Processor and Peripheral IP Cores for Microcontrollers in Embedded Space Applications

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A typical microcontroller consists of a processor core, on-chip memory and several communication interfaces in a design with emphasis on simplicity and determinism. The GRLIB IP library has several cores, including processors, memory controllers and communication interfaces, suitable for microcontroller designs.
The presentation will highlight the benefits of choosing a SPARC based processor core and will include examples of microcontroller systems using the LEON3 processor together with peripheral cores from Aeroflex Gaisler's GRLIB IP library.

1 ARCHITECTURE

1.1 Requirements

A microcontroller design should emphasize simplicity and determinism. Therefore a single processor system with one bus connecting the processor, memory and peripheral cores is proposed. Important parameters when selecting the processor core are; performance and clock efficiency, power consumption, suitability for space usage, and software support.

1.2 8- or 32-bit instruction set

In 1997, ESA initiated an activity in which a commercial 8032 core was purchased. The final product from that activity is a design featuring the 8032 core together with peripherals and functions for space applications. The 8032 core is an 8-bit microcontroller, compatible with the well-known 80C32/80C52 device and combines moderate execution speed with a moderate level of integration. The estimated size is 20 kgates according to the provider Dolphine. Comparable cores show an approximate size of 20 kgates. This can be compared with the LEON3 processor core including cache controllers that is about 20 kgates.
The performance claimed for the 8032 core is 2.4 DMI¬PS at 100 MHz system clock frequency (Dhrystone 1.1). Extrapolating from the figures presented in data sheets, the raw performance estimate is in average about 6.5 Clocks Per Instruction (CPI). This performance can be compared with the LEON3 core, which has an average CPI of 1. The LEON3 performs about 140 DMIPS at 100 MHz system clock frequency (Dhrystone 2.1, which is more demanding than Dhrystone 1.1).
The 8032 core implements its proprietary on-chip bus on which the peripherals are attached. The bus is based on 8-bit data width. One could wrap up the core with an AMBA interface, but since most existing AMBA modules are based on wider buses than 8 bits, the bus utilisation would suffer. Applications today often work with 32-bit data and engineers are accustomed to writing applications with the support of operating systems. A more powerful processor may be necessary in order to fit current development practices.
The main perceived disadvantage of using a 32-bit instruction set is the increased amount of memory required for program storage as compared to 8-bit instruction sets. However when processing data with higher accuracy than 8 bits the number of required instructions is larger for an 8-bit processor, which can offset the code size difference considerably.

1.3 SPARC architecture

The European space community has used SPARC based processors extensively and has substantial experience with developing software for the architecture. This means that there is a possibility for software re-use on a SPARC based microcontroller. The LEON3 and LEON4 SPARC V8 processors from Aeroflex Gaisler offer code compatibility with both LEON2 and ERC32.
A major advantage of the SPARC architecture is that it is completely open, well documented and under control of the non-profit organization SPARC International. Re-implementing proprietary architectures often brings legal problems in form of alleged patent or copyright violations. A well-known case is Intel vs. AMD regarding the x86 architecture, but other cases also exist.
A potential drawback of the SPARC architecture when building a microcontroller is that SPARC has a Harvard architecture. Harvard is a computer architecture where the buses and storage for instructions and data are separated. However, the SPARC architecture used in the LEON series is a modified Harvard architecture where the instruction and data caches are separated while both caches make use of the same bus system and memory.

1.4 Proposed architecture

The presentation will include examples of, and performance figures for, microcontroller designs using the fault-tolerant LEON3FT SPARC V8 processor together with currently available cores from the GRLIB IP library.

2 AVAILABLE IP CORES

2.1 Processor

The LEON3FT is a synthesisable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The model is highly configurable, and particularly suitable for system-on-a-chip (SoC) designs. The processor core is fault-tolerant and SEU-proof and is already used in a number of space applications. Some of the features of the LEON3 processor are:

- SPARC V8 instruction set with V8e extensions
- Advanced 7-stage pipeline
- Hardware multiply, divide and MAC units
- IEEE-754 FPU options available
- Configurable caches: 1 - 4 ways, 1 - 256 kB/way. Random, LRR or LRU replacement
- Advanced on-chip debug support with instruction and data trace buffer
- Power-down mode and clock gating
- Robust and synchronous single-edge clock design
- Up to 125 MHz in FPGA and 400 MHz on 0.13 um ASIC technologies
- Extensively configurable
- Large range of software tools: compilers, kernels, simulators and debug monitors
- High Performance: 1.4 DMIPS/MHz, 1.8 CoreMark/MHz (gcc -4.1.2)

The next generation processor in the LEON series, the LEON4 is also available. The LEON4 features a wider bus interface and is targeted toward applications with high processing requirements. The LEON3 can easily be replaced with LEON4, should the need for processing power warrant the use of LEON4.

2.2 Communication interfaces

The GRLIB IP Library contains a number of interface cores that are suitable for microcontroller designs. Examples of IP cores included in the library are:

- CAN controllers
- SPI master/slave controller
- I2C controllers
- PWM controller
- GPIO port
- USB controllers
- SpaceWire controller
- MIL-STD-1553B controller
- UART
- ADC/DAC interface controller
- Pulse generation core
- Time distribution core

2.3 Memory interfaces

Several different memory controllers are available and a selection will be included in the presentation. Since a microcontroller design needs to have a low pin count it may be difficult to dedicate pins to, or even have the possibility to use, external RAM/ROM.

Aeroflex Gaisler provides IP for implementing fault-tolerant on-chip RAM. The possibility to include on-chip PROM should be investigated for a microcontroller implementation. Another alternative is to use a serial interface for the boot PROM. The GRLIB IP library already includes a SPI memory controller that provides a boot PROM interface.

3 SINGLE EVENT HARDENING

The fault-tolerance in a microcontroller is foreseen to be aimed at detecting and correcting SEU errors in on-chip, and potentially off-chip, RAM. The caches and register files in the LEON3FT core are protected using parity and BCH coding, while the boot PROM will typically be protected with BCH. Any RAM blocks in on-chip IP cores are protected with BCH or TMR. Flip-flops are protected with SEU-hardened library cells if available, or TMR otherwise.

Many of the cores in the GRLIB IP library have been developed for use in harsh environments and can be instantiated with fault-tolerant configurations.

4 AVAILABILITY

All IP cores described in this abstract and in the presentation can be licensed from Aeroflex Gaisler. Design services of IP cores and complete system-on-a-chip designs are also available.
Microcontroller configurations can also be delivered on FPGA devices such as Actel RTAX and RT ProASIC3.

5 SOFTWARE SUPPORT

Software development targeting a LEON/GRLIB system is supported by a debug monitor, simulators, integrated development environments and toolchains maintained by Aeroflex Gaisler.
Most of the toolchains are GNU based and can be used with common development environments. Aeroflex Gaisler also offers LEON IDE, which is a plug-in for the Eclipse C Development Tooling (CDT), a C/C++ development environment for Eclipse. LEON IDE extends the CDT environment to include support for development and debugging using the tools provided by Aeroflex Gaisler.
For resource constrained targets like a microcontroller, and for applications that require low software overhead, the Bare-C Cross-compiler (BCC) may be an attractive option. BCC is based one the GNU compiler tools and the Newlib standalone C-library. The cross-compiler system allows compilation of both tasking and non-tasking C and C++ applications. BCC also includes the GDB debugger and a scheduling library (FreeRTOS).
Several alternatives are available if a project requires a full operating system. Alternatives include:

- RTEMS 4.8 and 4.10
- eCos
- VxWorks (WindRiver)
- LynxOs (LynuxWorks)
- ThreadX (Express Logic)
- Nucleus (Mentor Graphics)
- Linux 2.0/2.6

For debugging on hardware the GRMON debug monitor is available. GRMON is a general debug monitor for the LEON processor, and for SoC designs based on the GRLIB IP library. The features offered by GRMON include the following functions:

- Read/write access to all registers and memory
- Built-in disassembler and trace buffer management
- Downloading and execution of LEON applications
- Breakpoint and watchpoint management
- Remote connection to GNU debugger (GDB)

6 CONCLUSION

Aeroflex Gaisler can immediately provide IP cores and design services for a complete microcontroller design. The GRLIB IP library is today used to create designs targeted for space applications and include the flight proven LEON3 SPARC V8 processor. Software development for GRLIB/LEON is supported by development environments, a competent debug monitor, toolchains and operating systems.
A microcontroller design based on LEON/GRLIB will benefit from the IP library's heritage and will also be compatible with existing SPARC software used in the European space community.