

# *Toward generic OBC specifications*

*Roadmap and perspective for SCOC3 based computers & associated software*

**Astrium Satellites**

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ADCSS 2010 – GeSOR - 03-11-2010

All the space you need



# Contents

- Generic OBC specifications
- Building Blocks
- OSCAR computer

# Vision for a Generic OBC specification

## ■ Scope

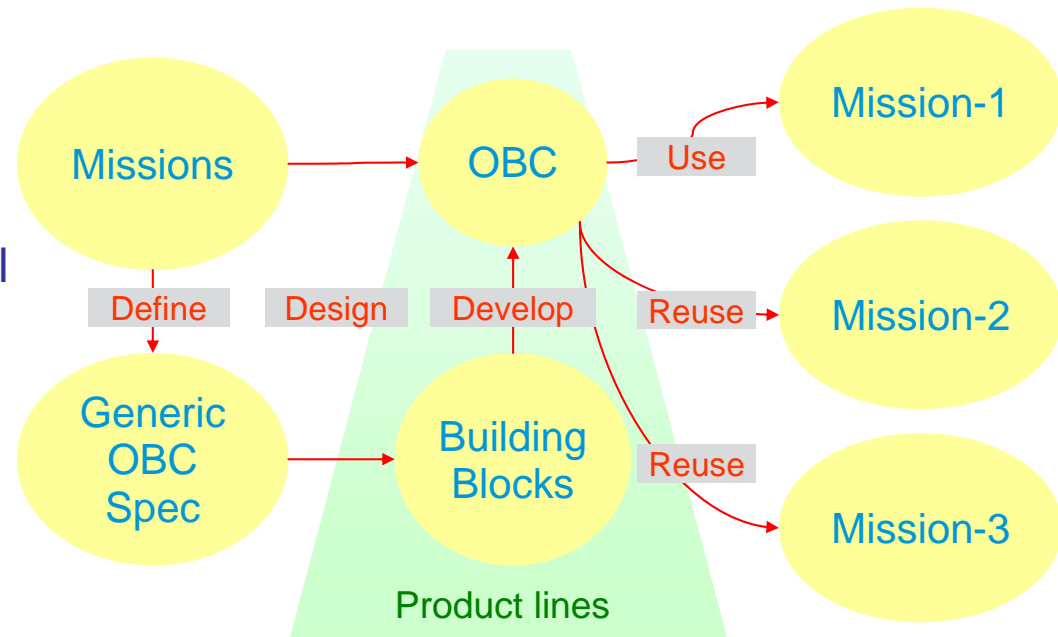
- Generic On Board Computer definition for EOS missions

## ■ Benefits

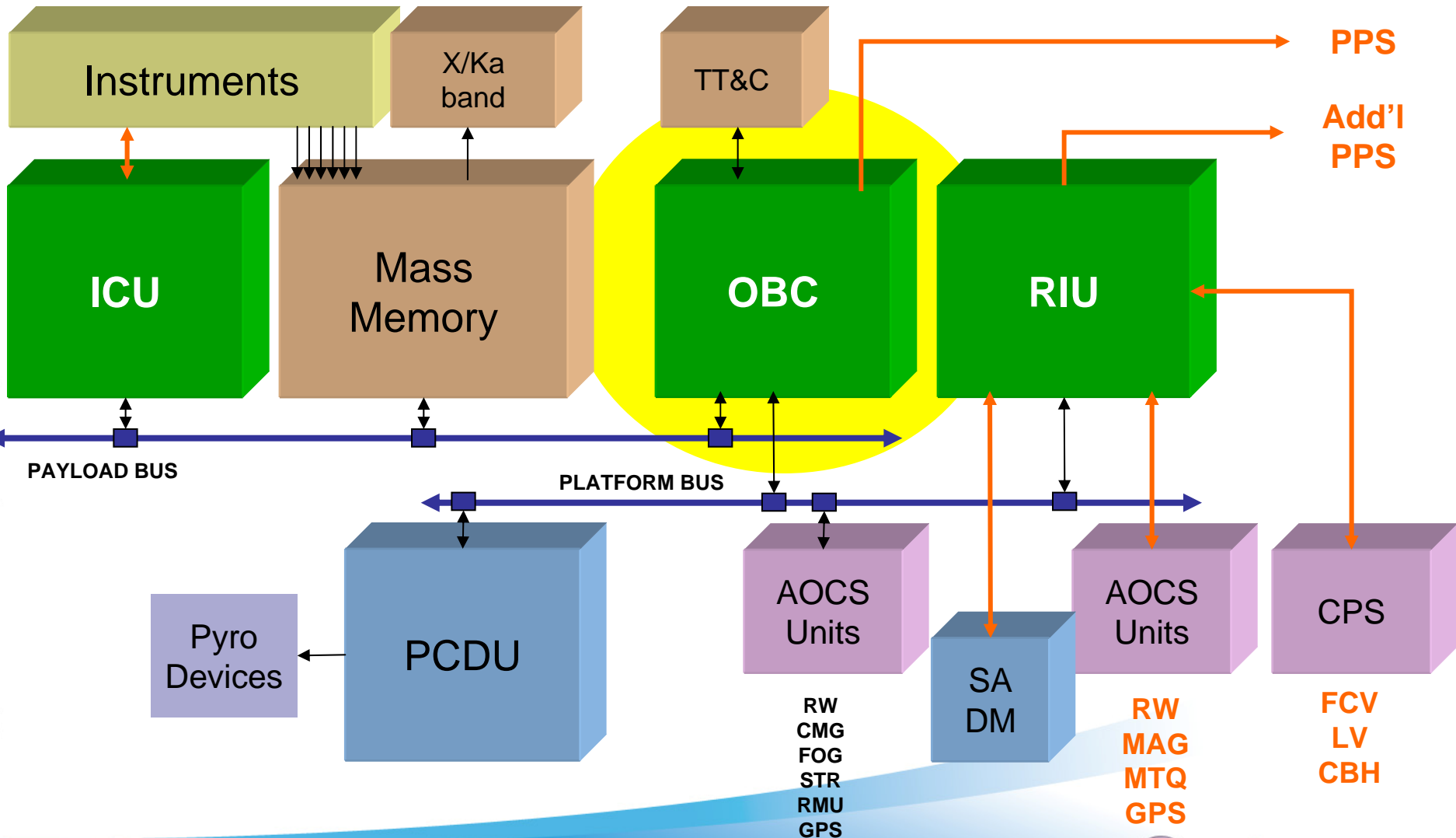
- Improve reusability
  - Across missions
  - At system and SW level
  - At equipment level
- Enables the development of industrial product lines

## ■ Keys for success

- Configurability
- Range of quality level and performance
- Business model



# Reference data handling architecture



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# Data Handling Functions

## ■ Generic Functions

- Real-Time Data handling
- Standard I/O's
- Spacecraft telemetry
- (Secured) Commanding
- Spacecraft operations

## ■ Mission dependant

- Direct TC's
- Direct I/O's
- Alarms
- Reconfiguration

## ■ Specific missions

## ⇒ Standard Building blocks

- ⇒ CPU, memory, clock, LLSW...
- ⇒ 1553, Can, SpW, ECSS protocols
- ⇒ CCSDS TM
- ⇒ TC + de-cyphering I/F
- ⇒ PUS library

## ⇒ Configurable modules

## ⇒ Specific modules

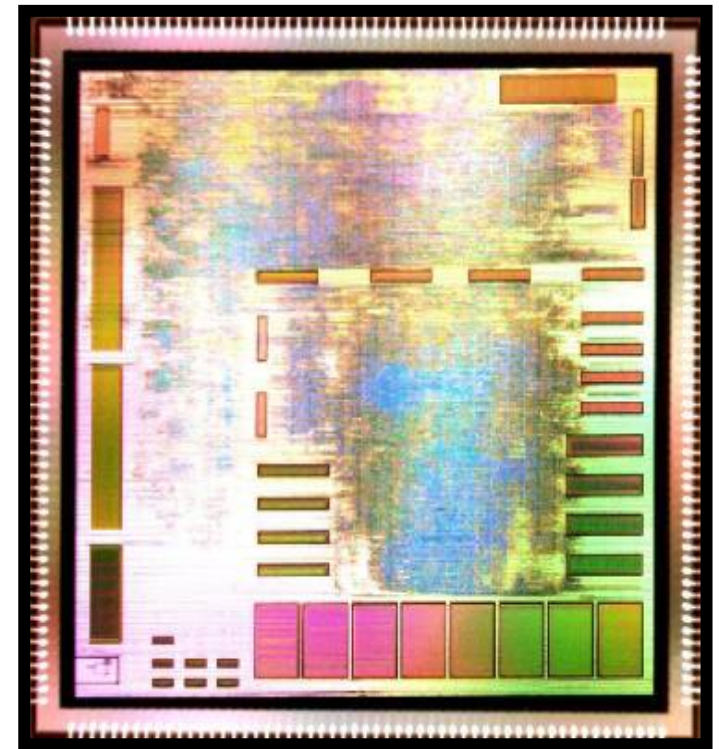
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# SCOC3 Key Features

*All the core functions of a platform computer on a single chip*

- **LEON3FT + GRFPU** (with caches and MMU) provide **68MIPS @ 80MHz**
- **CCSDS TM/TC interface + MAP interface** for **cross-strapping** of 2 SCOC3
- **7 x SpaceWire-RMAP**
- **2 x 1553, 2 x CAN**
- **4 x UART**
- **CCSDS Time Management**
- **Compatibility with both SDRAM and SRAM**
- **Power Management** (clock gating)
- **Security module** as an option (authentication, encryption)
- **Debug facilities** (IP Monitor, LEON DSU)



# SCOC3 ASIC

*Now available on the shelf*

- Fully characterized on OSCAR & KERTEL respectively with SDRAM & SRAM



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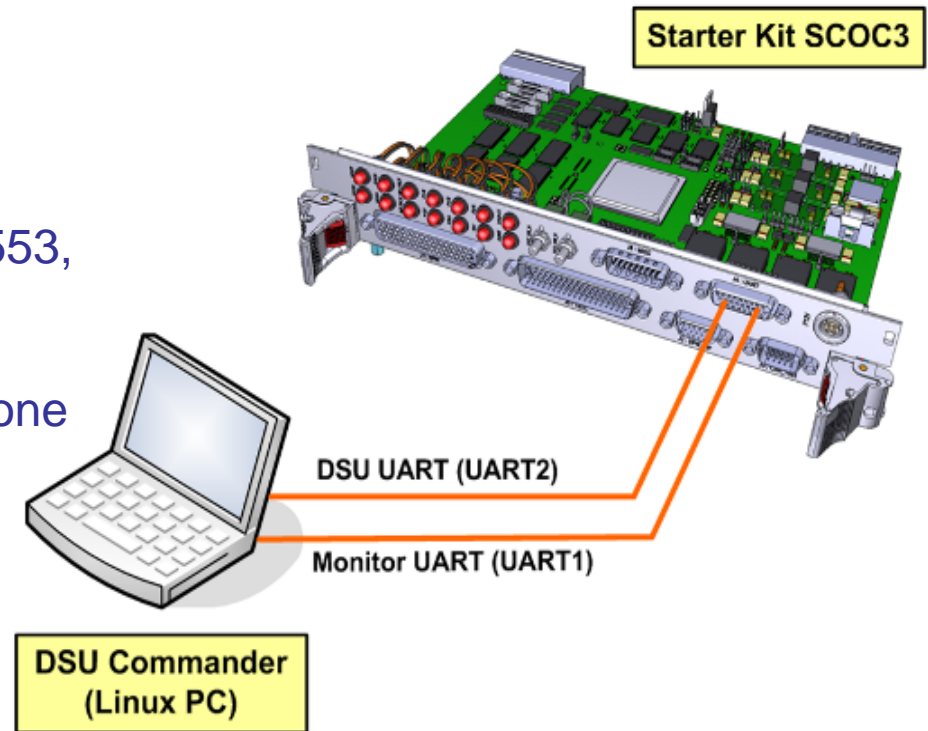


# SCOC3 STARKIT

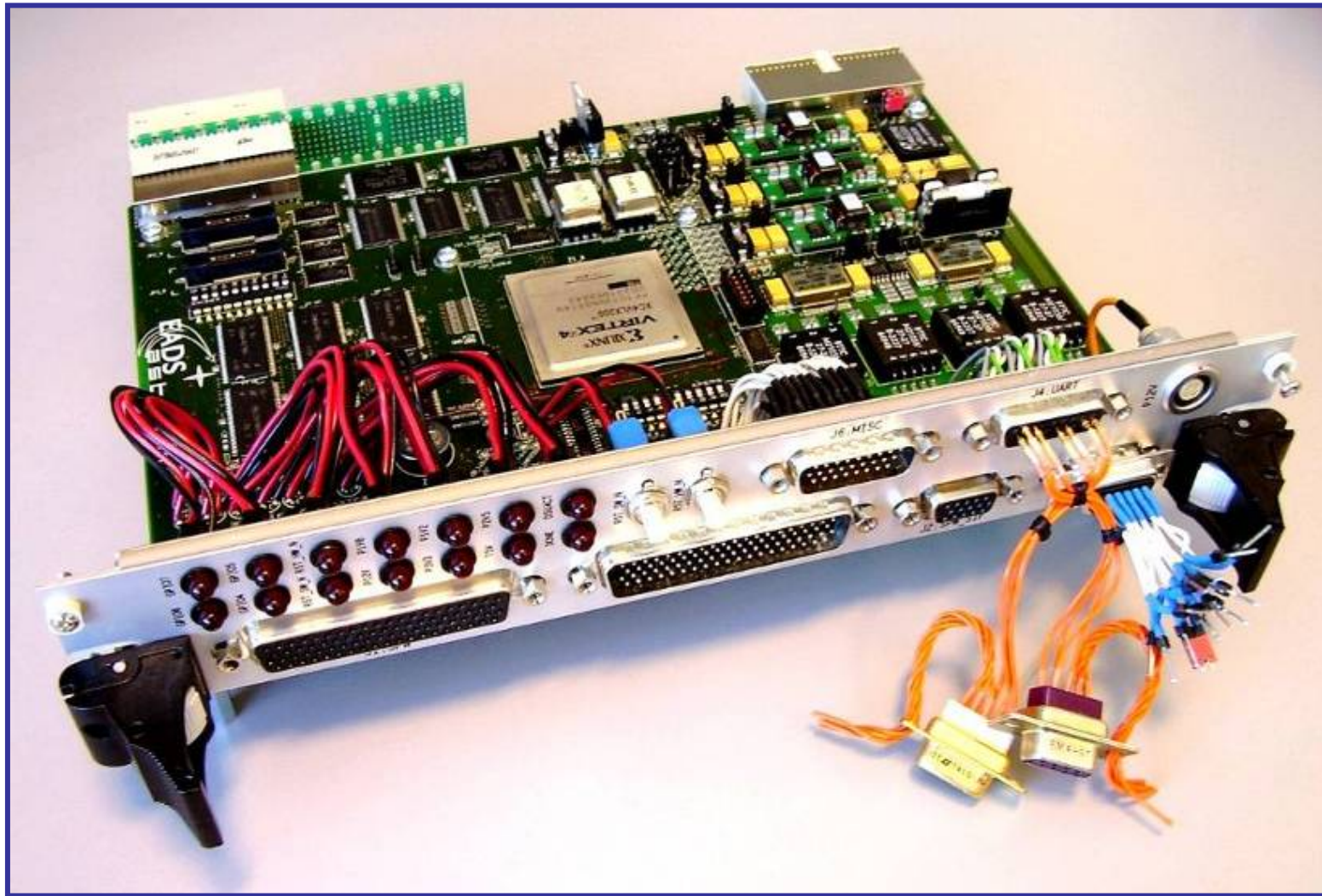


*SW R&D, performance evaluation, SW development*

- The **SCOC3 Starter Kit** evaluation board (**STARKIT**) provides a development platform for the early development and rapid prototyping of applications using the SCOC3 processor provided by EADS Astrium
- This 6U format board incorporates:
  - **SCOC3 VHDL** design in a fully representative Xilinx
  - **on board memory**
  - and all of **SCOC3 interfaces** (2x1553, 2xCAN, 4xUART, 7xSpW, TM/TC...)
- The STARKIT can be used in stand-alone or inserted into a cPCI rack
- A dedicated **expansion board** can be connected to the STARKIT if required



# STARKIT Status and Availability

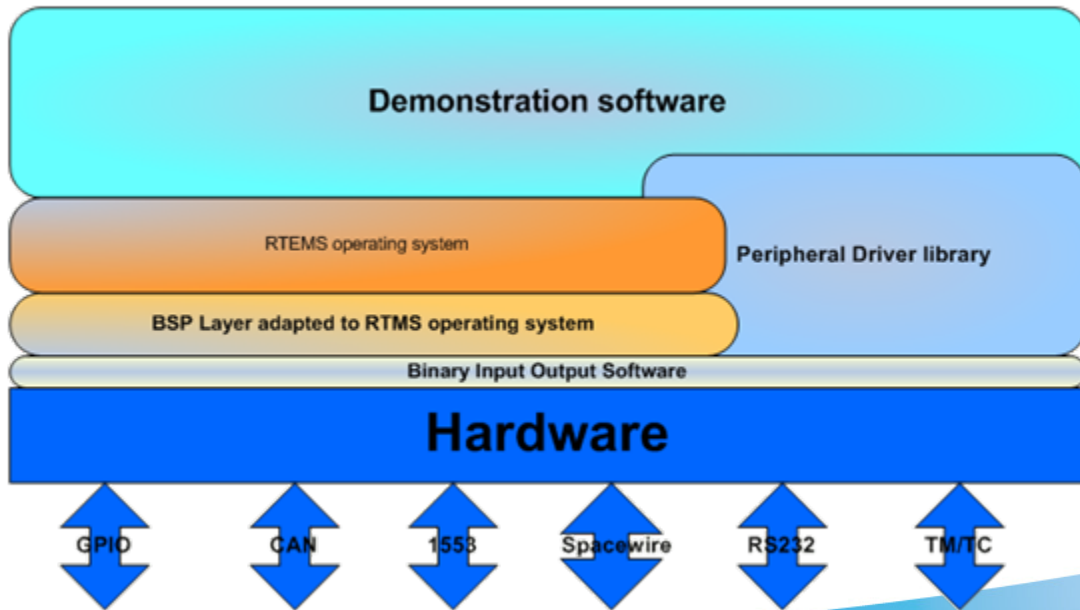


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# SCOC3 SW

*Can be provided with SCOC3 products*

- **Hardware Software** interface layer independent of the Real Time Operating System
- **Board Support Package** adapted to RTEMS Operating System
- **Drivers** for I/O's (SpW, 1553, CAN, UART, ...)



- **Demonstration SW** as test application example
- **SCOC3 software support** (planned ESA TRP)

# SCOC3 Simulator

- SCOC3 simulator executes as fast as real time
  - Using JIT technology
  - Calibrated with real HW
- Used for SW validation and operations
  - Ability to fully control execution time
  - Integrated with non intrusive debug functions
  - Failure injection capabilities to exercise SW error cases
- Test SW in Java
  - Eclipse plug-in

# SCOC3 Simulator

The screenshot shows the Eclipse IDE interface for the SCOC3 Simulator. The main editor displays the Java source code for `testMemAccessTime.java`. The code includes package declarations, imports, and a public class `testMemAccessTime` that extends `ARSATSimSequence`. The class contains a `sequence()` method that configures the simulation and runs it.

The left sidebar shows a project tree with various test files, including `testMemAccessTime.java`.

The right sidebar shows simulation parameters and data sources. The parameters include `simtg@local` with `State=STOPPED`, `SRT=0.250000`, and `Epoch=00:00:00`. The data sources include `SPW2`, `SPWCOMIA`, `SPWIntMul`, `SPWResp1`, and `SPWResp2`.

The bottom panel shows a simulation logbook with a table of messages:

Message	Sender	SRT	Epoch	Zulu
Sequencer RAM is now cleared	SPU.IOM_B.Control	0	00:00:00	16:05:42
Sequencer RAM is now cleared	SPU.IOM_A.Control	0	00:00:00	16:05:42
EEPROM write disabled set	SPU.PM_A.CPU	0	00:00:00	16:05:42
Initialising SimControl	simtg@local	0	00:00:00	16:05:42
Calling Initialisation entry points (if they exist)	simtg@local	0	00:00:00	16:05:42
Beginning Initialisation	simtg@local	0	00:00:00	16:05:42
Connecting models to Simulation environment	simtg@local	0	00:00:00	16:05:42
Configuring models	simtg@local	0	00:00:00	16:05:42
Starting Publication process for all Models in the Model Container	simtg@local	0	00:00:00	16:05:42
Created an object of class: LookbookCounter with name LookCounter	simtg@local	0	00:00:00	16:05:42

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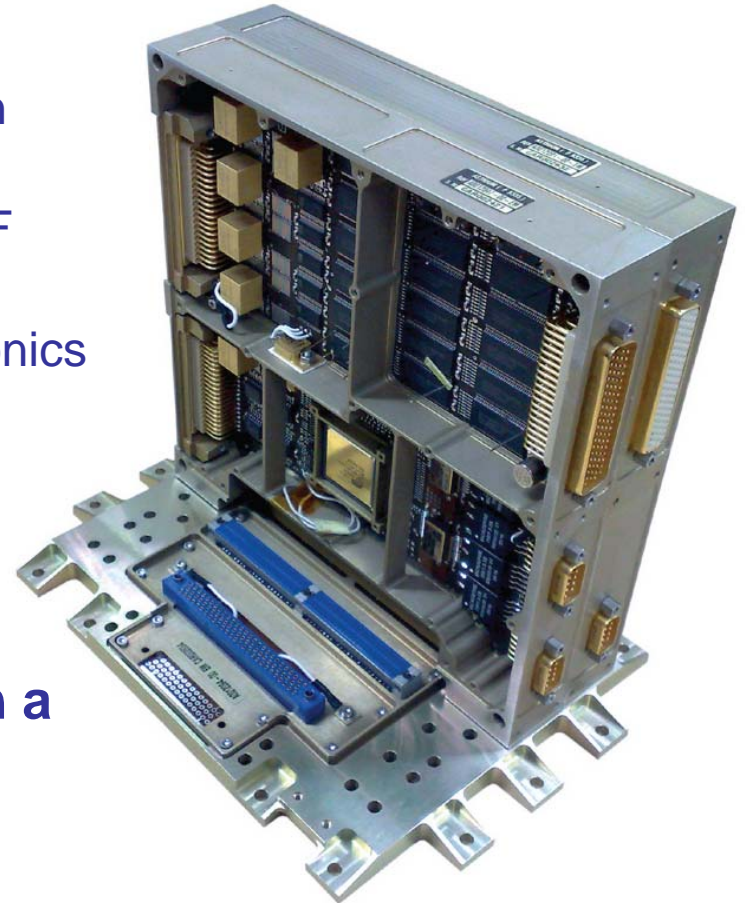
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# OSCAR

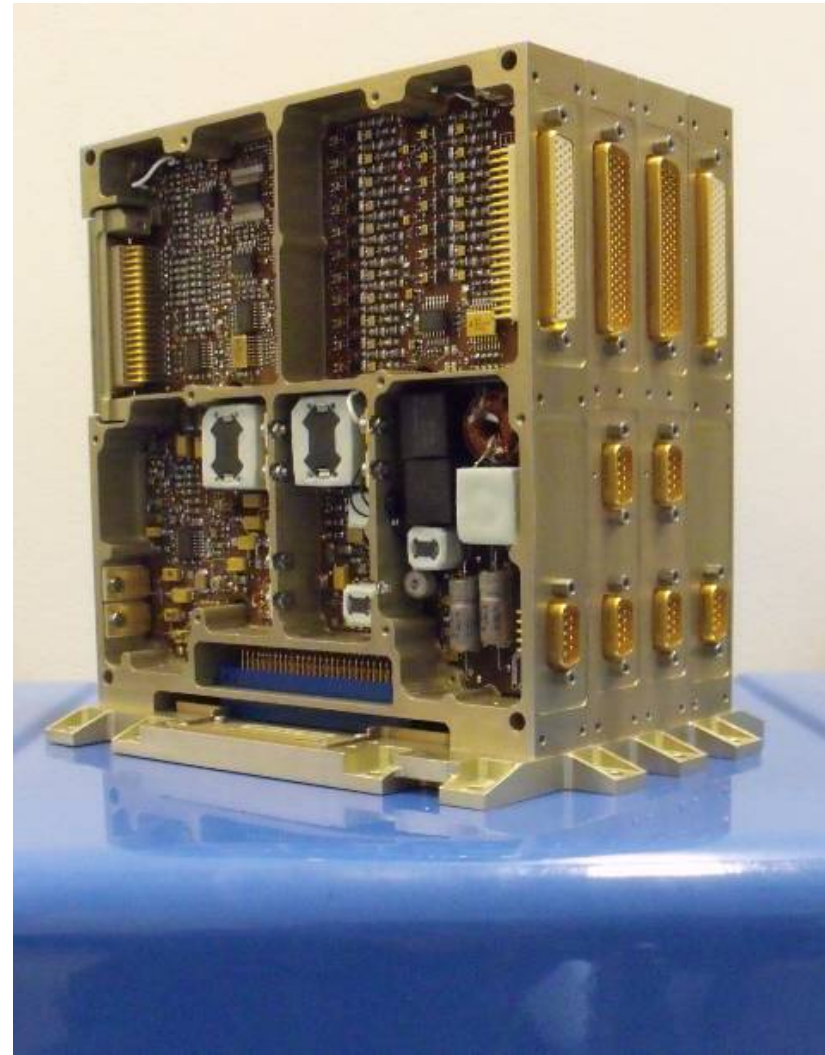
## *Generic OBC for any space quality program*

- **OSCAR provides the satellites with**
  - Processing resources for the flight mission software
  - TM/TC services and interfaces with the RF communication chain
  - General communication services with avionics and payload
  - Time synchronisation and distribution
  - Failure tolerant architecture based on redounded configuration
- **For genericity, I/O's are implemented in a separated box**
  - controlled via 1553 or SpaceWire



# OSCAR performances

- Up to **40 MIPS** for software execution
- **128 kbytes** EEPROM for boot SW
- **256 Mbytes** RAM for execution
- **512 Mbytes** RAM for mass memory
- 2 redounded **MIL-STD 1553B** for platform and payload management
- 2 **SpaceWire** links
- **CCSDS Telemetry and Telecommand** compliant with ESA standard
- 2 computer boards and 2 DC/DC converter boards **cross strapped for redundancy**
- UART and SPW links for SW development and debugging: **IP monitor and DSU**





# OSCAR characteristics

## ■ Budgets

- Mass 5.2 kg
- Volume 226 x 157 x 205 mm<sup>3</sup>
- Power 22 W

## ■ Environment Reliability

- Temperature -40°C to +85°C
- Vibration 20 g sine, 20 grms random
- Shock 1000 g @ 1000 Hz
- Radiation 15 krad total dose Si  
SEU tolerant (no fct impact)  
Latch-up immune
- EMC/EMI MIL-STD-461
- Reliability 3000 fits per channel



# OSCAR for any class quality program

- Based on the same ICD / SW & dev tools, OSCAR offers the same performances for any class quality program, with adapted EEE selection and manufacturing quality level
  - **OSCAR class 2** is the baseline for SEOSAT, SPOT6/SPOT7. This product is qualified, recurrent unit and can be proposed within roughly 12 months
  - **OSCAR class 1** has been derived from the class 2 version with the replacement of some EEE, and the upgrade of the justification file. It is the baseline for the CSO program
  - **OSCAR class 1 full hermetic** will be based on OSCAR class 1, with replacement of plastic part by MCM, for application for eg on SatCom market. The MCM necessary technologies have been validated, they are compatible with the MCM product line of Astrium France
  - **OSCAR class 3** version has been proposed for several customers and is ready to provide the market with a low cost version

# Conclusion

- **Reference DHS architecture enables generic OBC specifications**
  - Generic requirement for DHS standard functions
  - Configurable to fit different mission needs
- **Standard building blocks and tools are today available or in development**
  - SCoC3, Starter Kit, Basic SW, Simulator
- **OSCAR computer selected on future missions**
  - Available for any class quality program

**Thank you for your attention**

**Questions ?**