# Reference Architectures: status of the art and trends

## GeSOR- ADCSS 2010

Giorgio Magistrati TEC-EDD
ESA-ESTEC Data System Division

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European Space Agency

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# Agenda

- Drivers for OBCs and RTUs development,
- Trends: SoCs, Processors, Companion Chips, Modular RTU, uController,
- System Busses & Interfaces
- Generic Specification for OBCs and RTUs (GeSOR)

# Drivers - Future Reference Scenarios

- Future programs for **Science, Exploration, Earth Observation and Telecom** are the sources of high demanding requirements for the next generation of OBCs & RTUs:
  - increase of processing power,
  - reduction of mass, volume and power,
  - implementation of functional services linked to on-board communication (e.g. CCSDS SOIS, CFDP) and TM/TC handling (e.g. PUS and extensions),
  - rationalization of Interfaces (Mil1553 & CAN protocol extensions, SpaceWire networks, digital sensor buses, …),
  - new architectures for lower level and application SW,
  - enhanced modularity and multi-instruments support capability **(Science),**

# Drivers - Future Reference Scenarios

- **Earth Observation** missions share with **Telecom** projects architectures that implement **security solutions** to protect the P/L data and the S/C control and monitoring functions.

- Protection mechanisms for:
  - telecommand and telemetry space data links for the control of satellite platforms,
  - direct control and configuration management of payloads of communication satellites
  - Protection of P/L data that requires the development of elements/modules/equipment able to implementing fast and reliable on-board digital processing operations.

# Drivers- Additional Consideration

- Increase of integration with the ground infrastructure. The integration with Ground infrastructure and Ground services is also changing the definition process of the mission requirements,

- FDIR concept has to be developed accordingly to the complexity of the current and future architecture in order to maintain high figures of availability (e.g. figure less than one hard reset for a Telecom satellite over 15 years of life service) and reliability. Built In Test (BIT) with high and very high failure coverage (>95-99%) and special debugging modes are now part of the most recent FDIR philosophies,

- Reprogrammability on Flight of HW resources will complement the existing possibility on SW elements of a flight segment.

# Drivers - Additional Consideration

- Recent advances made in the field of Time and Space partitioning benefiting from sophisticated memory management functions implemented in CPUs must be supported as well.

- The increasing request of higher performance in term of MIPS/MFLOPS calls for the development of multi-core processors following a well consolidated trend that has started several years ago in the commercial/embedded markets. Clearly the operative system(s) and the SW development/implementation tools have to be accordingly improved.

- As alternative or also as complementary solution distributed processing power architectures calls for the development of uControllers that can offload the main processor from defined tasks

# Trends: Processors & SoCs

- **ATMEL 697F** (SPARC V8 32-bit Architecture, Performances: 1MIPS/MHz, 0-100 MHz, 10mW/MHz, TAS-I baseline for EXOMARS EDM Computer)
  - Fault Tolerance by Design, Full Triple Modular Redundancy (TMR), EDAC Protection, Parity Protection
- Astrium is currently developing a new generation of SoCs : **SCoC3** based on LEON3FT, dedicated to Platform applications and **MDPA** based on Leon2FT dedicated to Payload applications (both already selected for several satellite applications)
  - An evolution of SCoC3 has already started (improved Memory Controller, HSSL)
- **Next Generation Multi Purpose Processor** (Activity kicked off in 3Q2009 with Aeroflex Gaisler as prime). The NGMP is based on a SPARC compliant multi-core architecture.
  - The objective is to have a standard product implemented in DSM CMOS (65 nm is today's baseline).

# Trends: Companion Chips

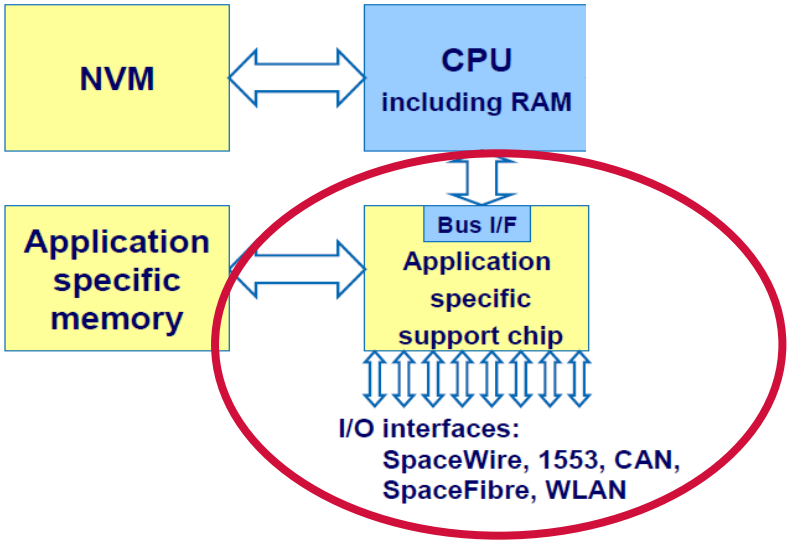
Functions as

- Fast I/Fs as SpW and Packet Wire,
- General Purposes I/Os,
- TM/TC I/F,
- Memory Management & Control Unit,
- Support for time/space partitioning

  can be implemented on a **Processor Companion Chip** as proposed for example by RUAG-S in Next Generation SMU Core Chip

- In this architecture the high performance core is decoupled from the interfaces of a specific application basically allowing an easier technology upgrade of the core itself.

- The proposed upgrade is intended for a design lifetime of at least 10 years, taking into account architectural changes of the spacecraft platform and aiming to be used also in instrument control units.

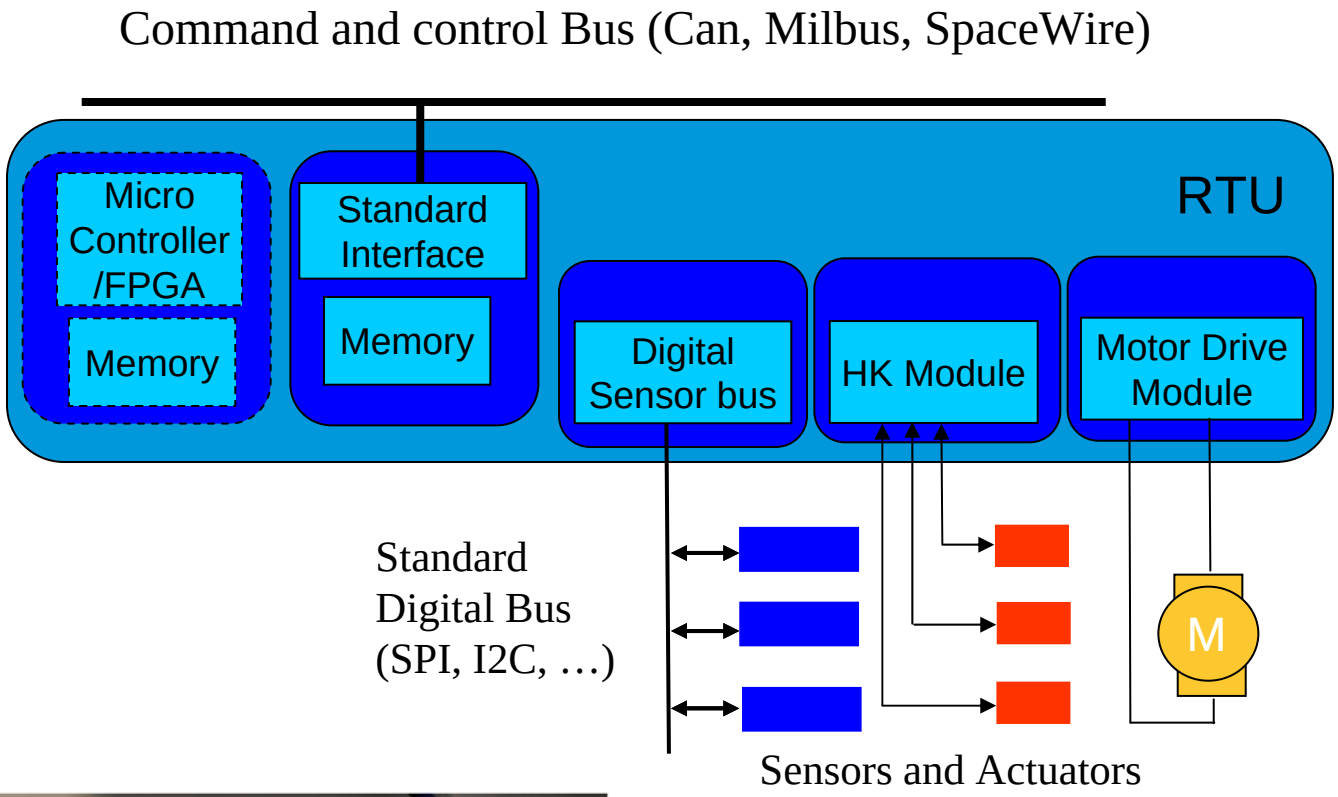


# Trends: Modular RTU

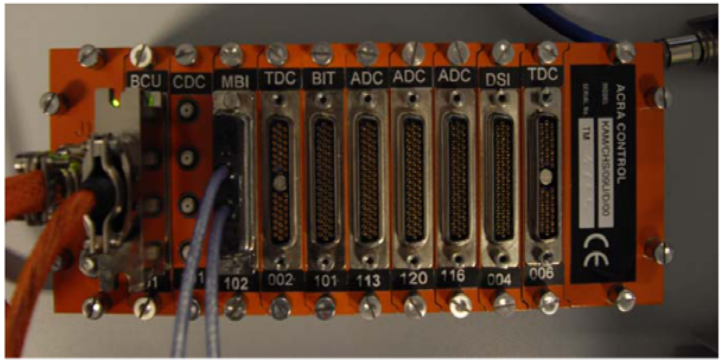
- The **modular RTU** has been identified in the Avionics Embedded Systems Dossier and Roadmap (recently updated in 2010) and by the SAG as a high priority building block.
- Modular RTU has been proposed as activity at the June 2010 Industrial Policy Committee (IPC) and several countries have confirmed their interest,
- Modularity and upgradeability are the key characteristics of the proposed unit to be developed; the unit has to be conceived as an assembly of different modules/slices with standardized mechanical and internal electrical interfaces.
- The main building blocks will be:
  - DC/DC power supply modules,
  - Controller Module
  - HK analogue & Digital I/O Modules
  - Serial digital Modules implementing serial digitized interfaces (I2C, RS422/485, SPI,...)
- Other modules can be conceived to be developed as well, among them:
  - uProcessor Module providing an autonomous capability to execute DAQ tasks
  - Wireless Module to be used as DAQ centre to distribute/convey wireless sensors network
- The interface with the OBC/SMU will be a MIL-STD-1553, CAN or SpaceWire.

# Modular RTU building blocks

- Remote terminal unit acts as a data concentrator
- Standard interface to OBC/CDMU
- Standard Serial bus to devices
- S/C may employ several miniaturised versions




Aeronautics/Embedded examples of RTUs




# Trends: Space Qualified uController

- As pointed out during the round table on Microprocessors for Space Applications (ADCSS09) the need for a reduced cost and highly integrated **microcontroller** for low-end space applications is strong. The obsolescence of the ATMEL 80c51 is creating a hole not filled by the available high-end microcontrollers like the AT7913E.

- The 2010 October IPC has approved the list of ESA basic Technology Research Programme (TRP) for the 2011-2013: among them an activity called *Microcontroller for embedded space applications: Specification and design verification* (**T701-317ED)** has been proposed

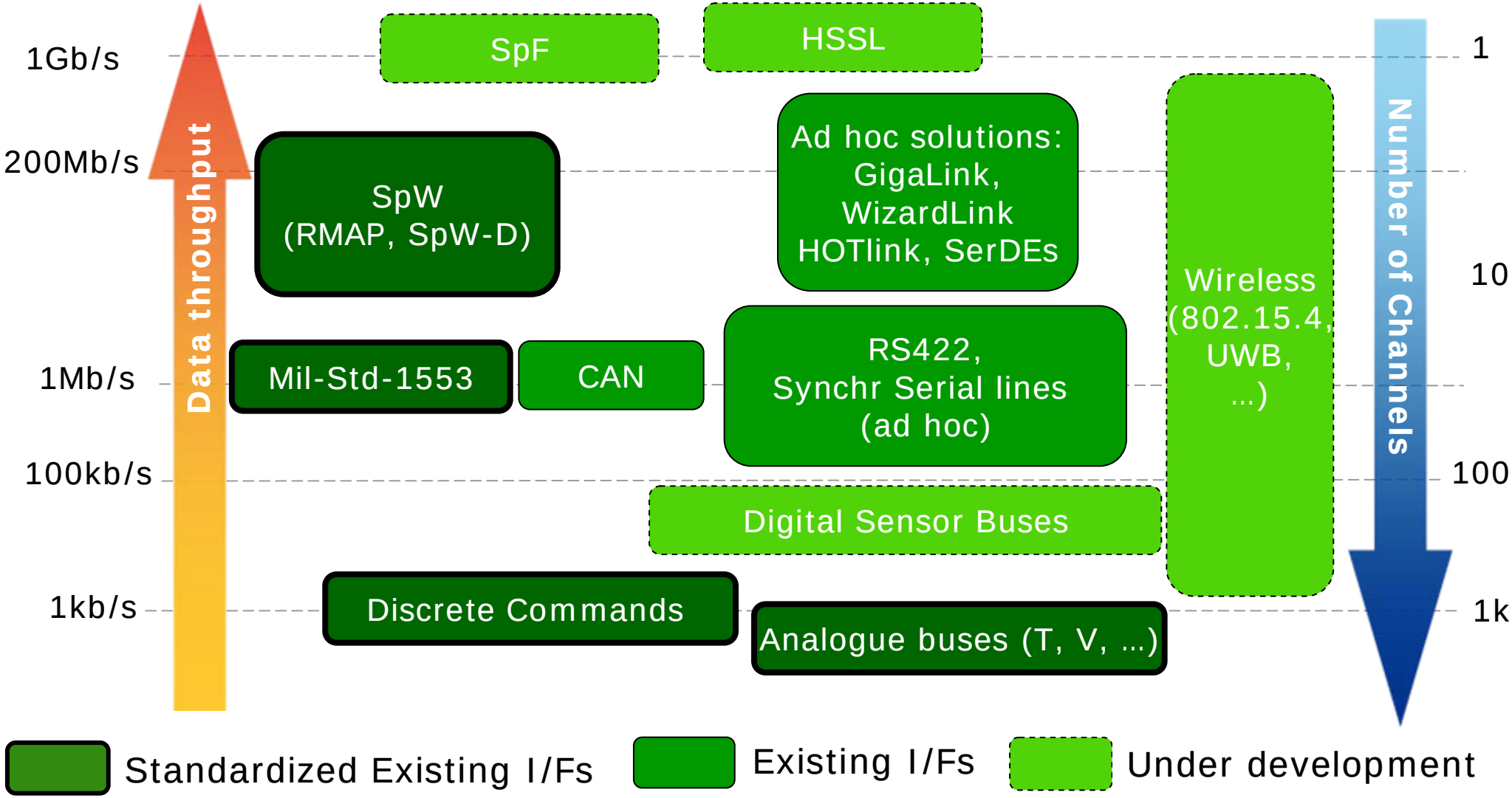
- This type of applications implies a reduced component price, a small and easy to be assembled low pin-count package (not BGA) and (monolithic) integration of essential system components (e.g. memory as RAM and (EE)PROM, serial I/Fs, GPIO's, PWM, ADC etc.) A low power consumption is a key point

- SW development and validation tools should be easily available (commercial?).

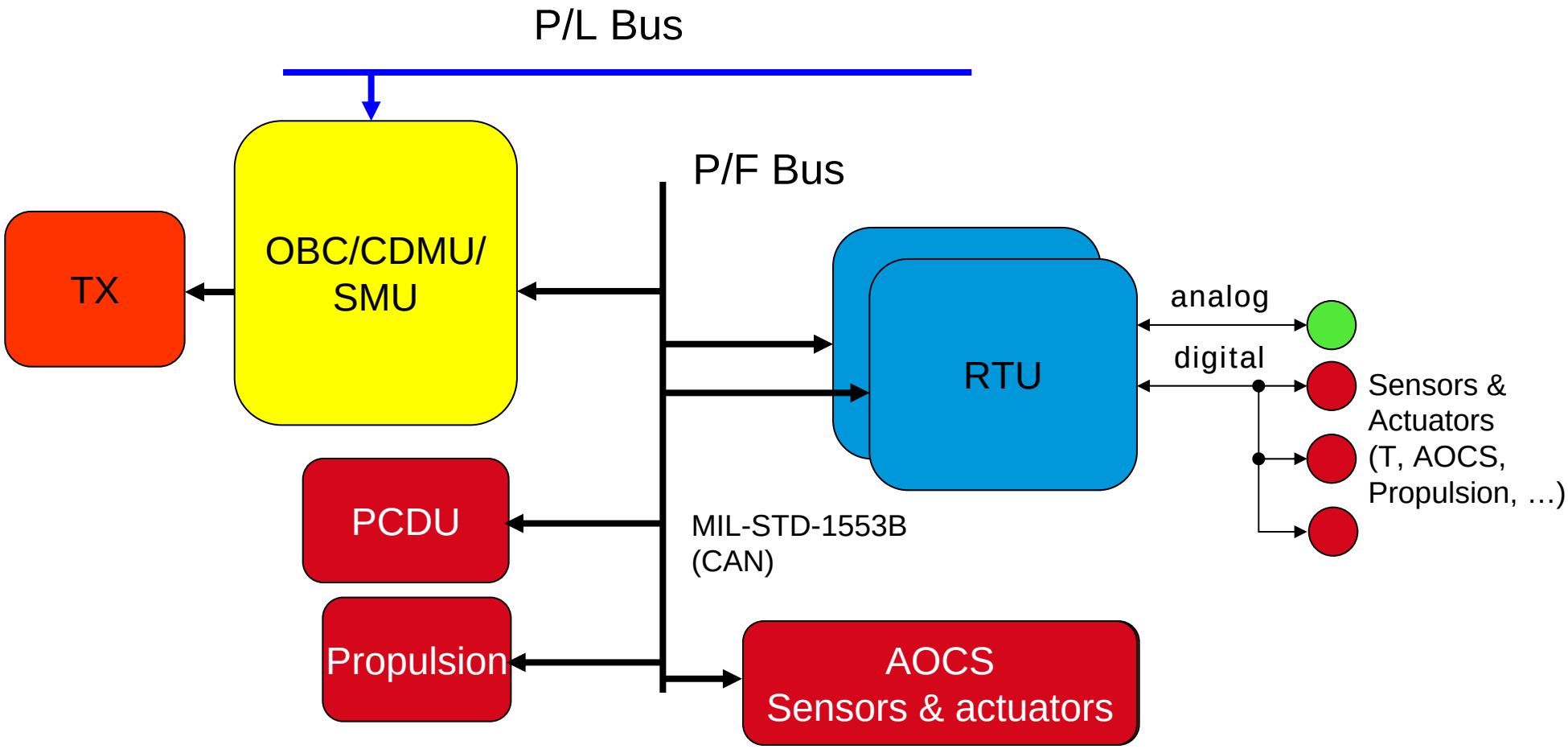
- Potential application areas are Power Distribution Systems, Motion Control, Sensors Acquisition, Sensor Wireless Networks, ….

- The Microcontroller can be the control core of a RTU in a decentralized architecture

# System Busses & I/Fs



# System Busses & I/Fs: Avionics System Topology – Platform Bus



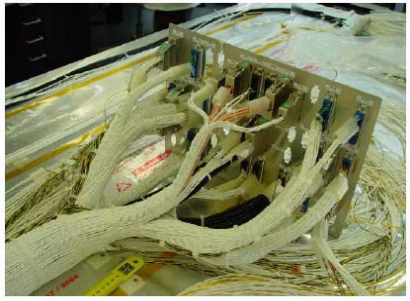
# **Digital Sensor Bus :** From ANALOG (ECSS-E-ST-50-14C) to DIGITAL (ECSS-E-ST-50-xx)

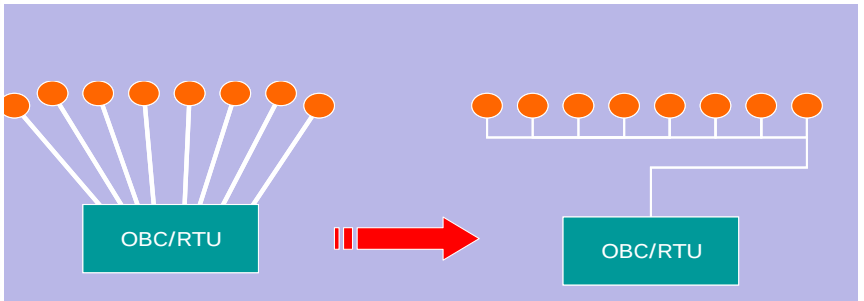
- Temperature Sensors, Pressure sensors , Position Sensors and Accelerometers used in space applications have been acquired as analogue signals up to now

- A natural evolution (higher resolution, better signal integrity and availability of miniaturised ASIC/sensors, harness reduction) requires the definition of standards for digital transmission of sensor data on a S/C

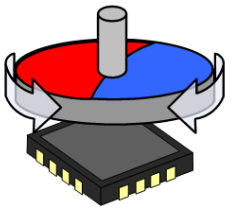
- Examples : SPI (Serial Peripheral Interface) implemented in the Contactless magnetic Angular Position Sensor (CAPS) developed by RUAG under a contract with ESTEC D/TEC/MMS, I2C investigated as digital sensor bus in the TEC-EDD TRP activity Sensor Bus #1

- Activity T701-314ED (Standardization of Digital Interfaces for Sensors) selected for the TRP 2011-2013 plan has as main goal a technical specification to be provided as an input to the new (to be created) corresponding ECSS working group.



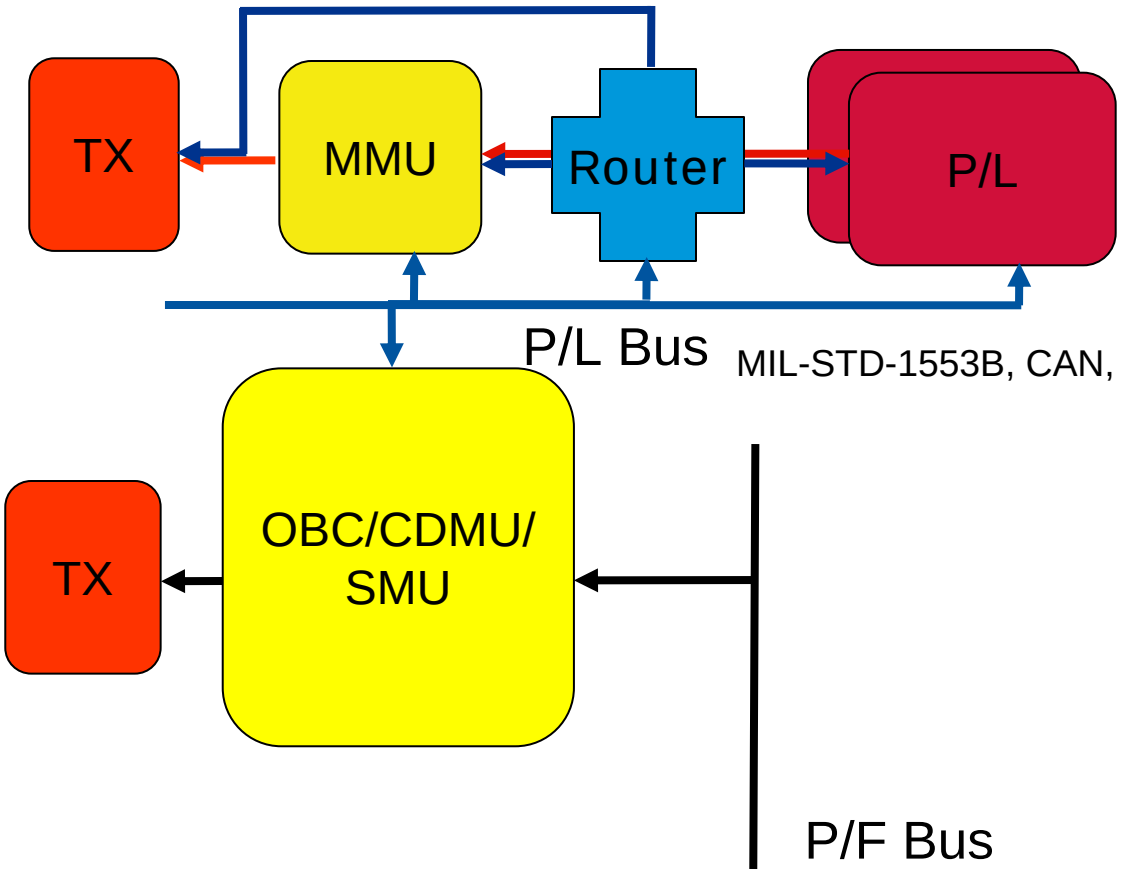



Sensor Bus (TRP)



CAPS (RUAG)

# System Busses & I/Fs: Avionics System Topology - Evolution of SpW

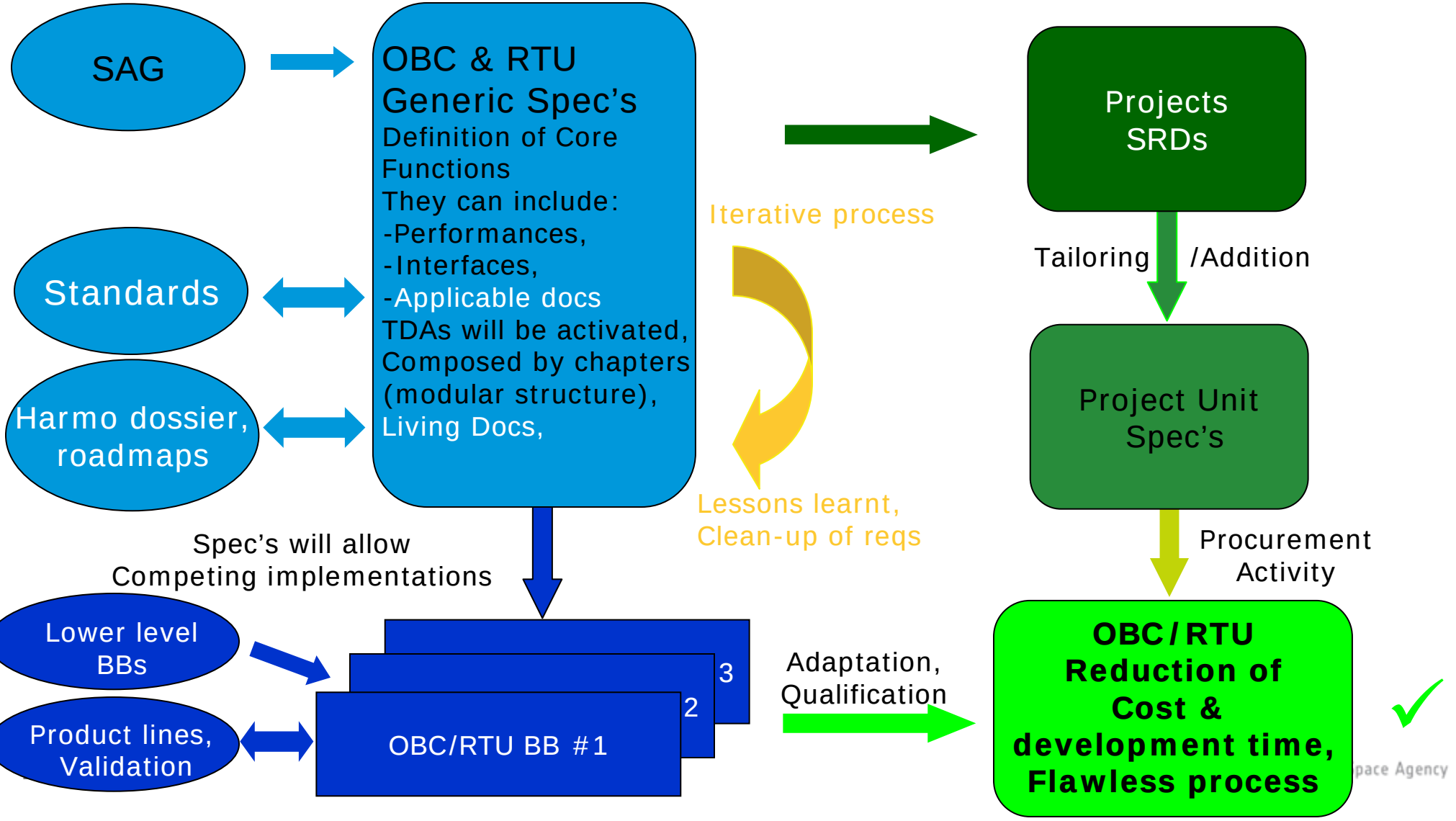



- Currently SpaceWire is typically used for high speed transmission of payload data, (multiple point to point configuration),
- Command & control data to P/Ls is transmitted on a separate interface,

➡ Impacts in terms of harness, mass and heterogeneous interface testing,

- SpaceWire-D (where D means deterministic) allows both command and control and high speed traffic to share the same interface,
- The protocol will be specified within the international SpaceWire Working Group before submission to an ECSS working group for development of the formal standard

# GeSOR: Generic Specification for OBCs and RTUs



# GeSOR: Q? for Round Table

- Open points:
  a. Generic Specification for Reference Architecture: a way to reach cost effectiveness and quality improvement . Do we all agree? Drawbacks?
  b. How to implement it ? Plan/Schedule definition
  c. Would a Modular Generic Specification be the correct approach ( where modular means composed of several sections addressing different functions)?
  d. How many Generic Spec's for an OBC? (Spacecraft, Launchers-Space Transportation,…)
  e. Should it be a minimum ( including only mandatory functions) or Maximum Spec (to be tailored to specific mission) that would be the best approach ?
  f. How will the generic spec's change the system engineering process of designing to requirements versus designing using products ?
  g. Is a requirement management tool (Doors, …) needed to generate the GeSOR?
  h. Requirements should be listed together with their justification, comments on this?
  i. Others?

# GeSOR Session: Agenda

| Time | Presentation |
|---|---|
| **GeSOR - *Generic Specifications for OBCs and RTUs*** | |
| 09:00-09:20 | Introduction Architectures: Status of the art and trends<br>*Giorgio Magistrati (ESA/ESTEC)* |
| 09:20-09:40 | Toward Generic OBC Specs – Roadmap and Perspective for SCoC3 based Computers<br>*Jean-Luc Poupat, Olivier Notebaert (Astrium-F)* |
| 09:40-10:00 | Next Generation Platform Input/Output Unit Roadmap and Standard Building Blocks<br>*Remi Roques (Astrium-F)* |
| 10:00-10:20 | RUAG View on Getting a Standard OBC and RTU Specification<br>*Torbjorn Hult (RUAG-S)* |
| 10:20-10:40 | Thales Alenia Space View on getting a Standard OBC and RTU Specification<br>*Gianluca Aranci, Livia Esposti* |
| 10:40-11:00 | ESA project perspective<br>*Damien Maeusli* |
| 11:00-11:15 | Coffee Break |
| 10:45-11:00 | Next Steps<br>*Kjeld Hjortnaes (ESA/ESTEC* |
| 11:00-11:30 | An Example of Spec (OBC Initialization)<br>*Felice Torelli (ESA/ESTEC)* |
| 11:30-13:00 | Round Table<br>*All* |
| 13:00-14:00 | Lunch Break |

**GeSOR Convenors:**
Torbjorn Hult (RUAG-S),
Kjeld Hjortnaes (ESA/ESTEC),
Giorgio Magistrati (ESA/ESTEC)