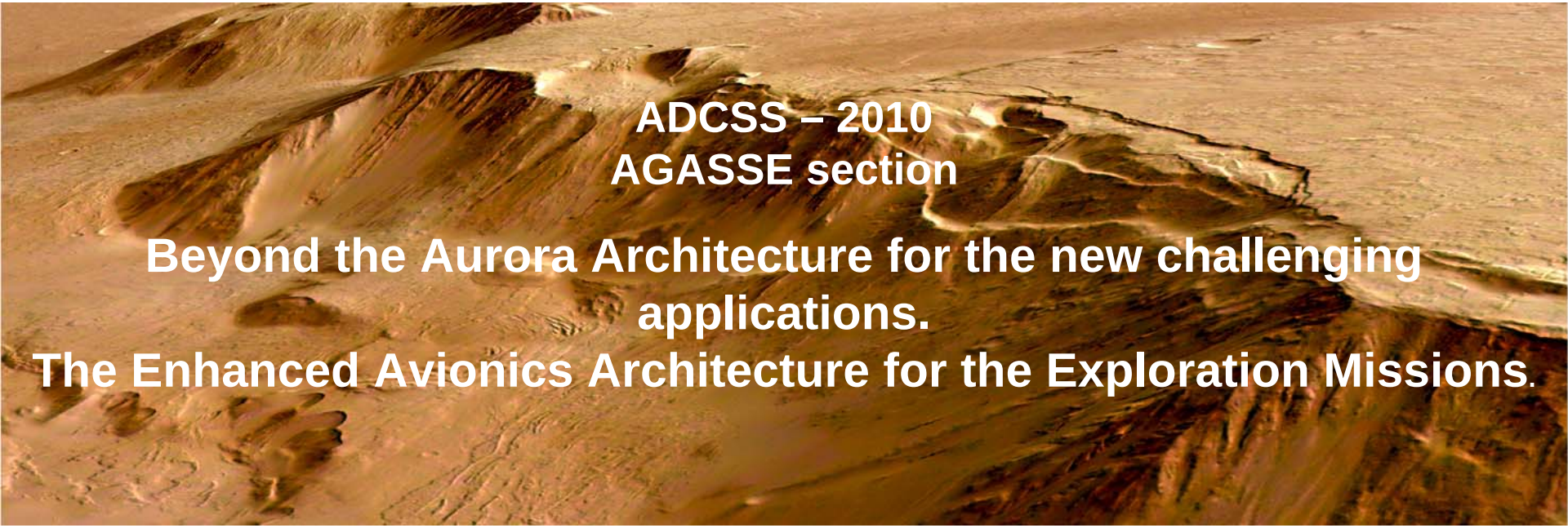

ADCSS – 2010
AGASSE section

Beyond the Aurora Architecture for the new challenging applications.
The Enhanced Avionics Architecture for the Exploration Missions.

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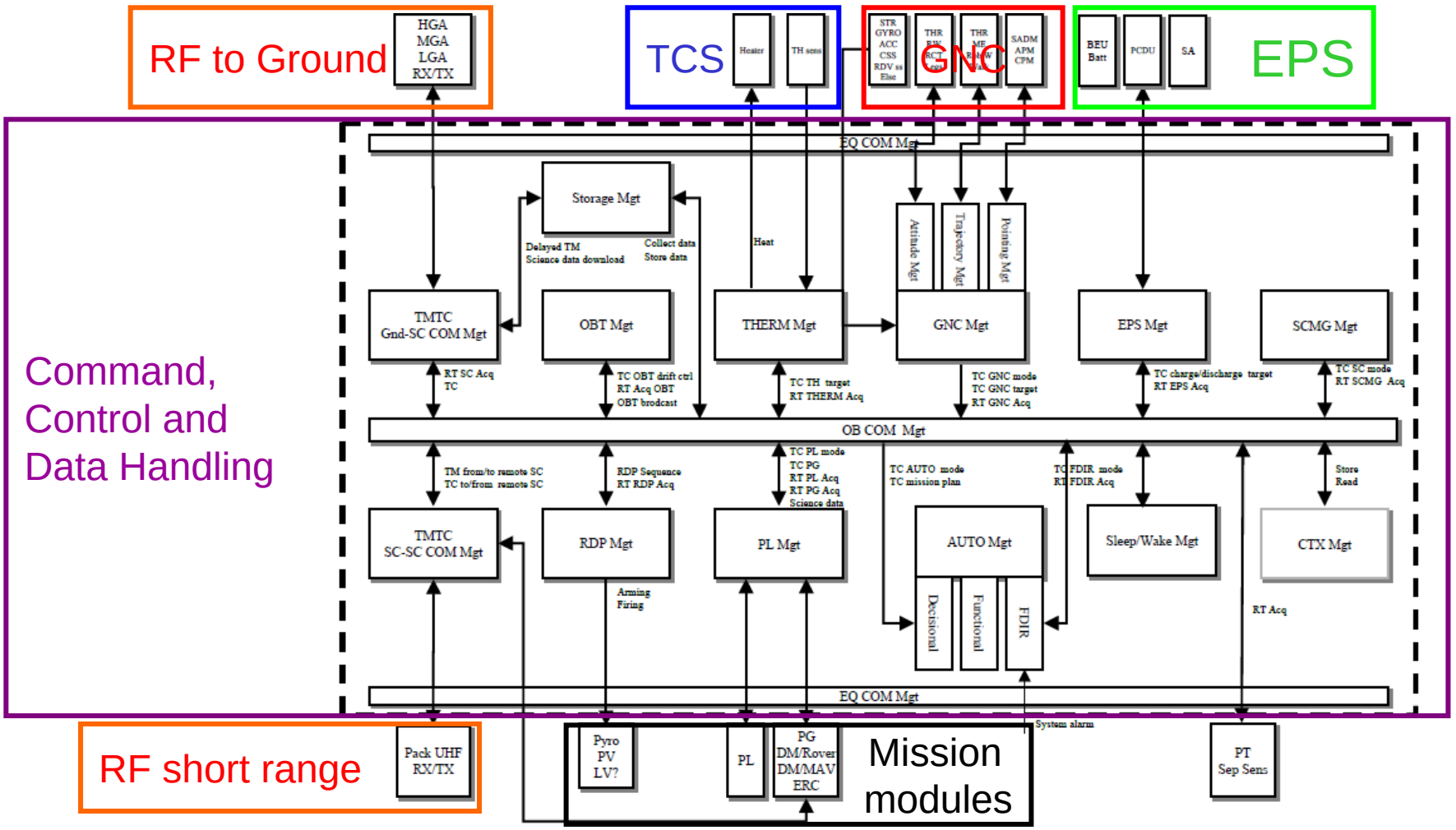
BSOOS Turin

Presentation contents

- Aurora Avionic Architecture as starting point
- EXOMARS : Aurora implementation
- Major requirements for exploration mission
- EDL, RVD and ROVER functional architecure
- Common elements : communication bus and CPU
- CDMU : processor – coprocessor configuration
- Avionic Test Bench to support avionic design
- Conclusion

Aurora Avionic Architecture as starting point



Aurora Avionic Architecture as starting point

Main functions implemented in the Aurora Architecture are :

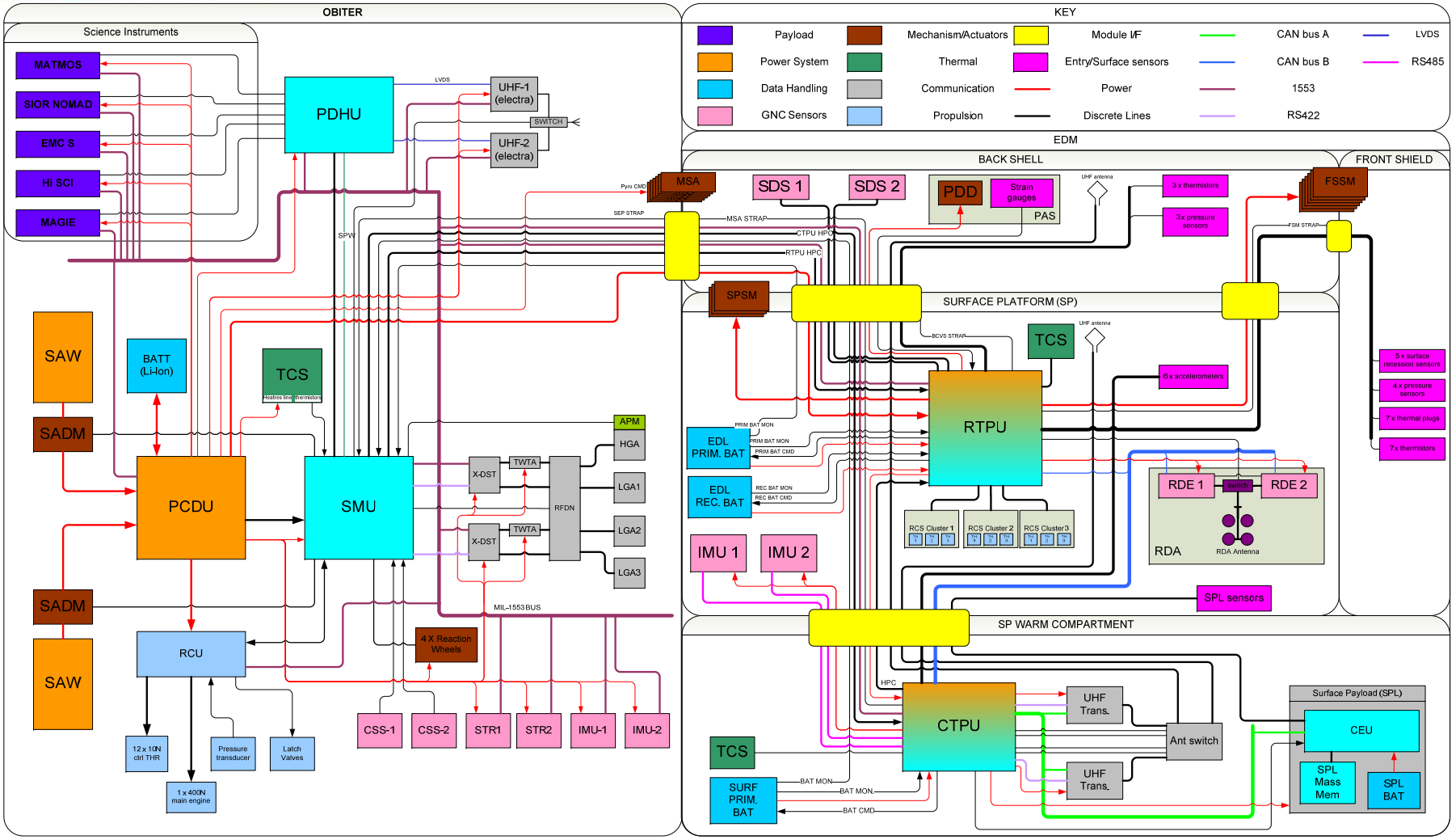
- TM/TC Management, Storage Management and On-Board Time (OBT) Management needed for interface with ground or with other spacecraft
- Thermal Management, Electrical Power Supply (EPS) Management for spacecraft TCS and EPS subsystem control
- Spacecraft Modes Management (SCMG), AMM/ FDIR Management, Equipment Management which are the principal Data Handling function. They handle the on-board system through the different mission phases, define the level of autonomy, execute the mission timeline, the detection of anomalies, and their recovery, maintain the equipment configuration following failure recovery execution
- GNC Management: computes the actuators commands from the sensors measurement in order to control the spacecraft attitude (and position) interfacing with GNC sensor and actuator units
- Payload Management: for scientific payload or additional units,
- Release, Deployment and Pyrotechnic (RDP) activation Management: for solar arrays/antenna deployment, for propulsion arming sequence before firing, or for specific needs like shield jettison or space-crafts composites dispatching
- Sleep/Wake-up Management: for the wake-up of a Descent Module near the atmosphere entry, or to make a Rover sleep during a Martian night,

EXOMARS: AURORA implementation

EXOMARS can be seen as the first implementation of the AURORA avionic architecture

- **Mission architecture require a composite S/C consisting of Carrier Module, Entry Descent Module, Rover Module. Release Deployment and Pyrotechnic mangement is needed**
- **Each module implements an Aurora architecture because TT&C, TCS, EPS, GNC subsystems are managed in each module**
- **Central Processing units in which SW functionalites are executed are embedded in each module of the composite spacecraft**

EXOMARS avionic architecture: OM and DM



Major requirements for exploration

Perform safe, soft and precise landing

- Safe site identification means capability to identify areas with minimal slope, acceptable hazards and taking into account illumination and environment constraints for power generation
- Soft and precise landing means capability to perform accurate absolute and relative navigation toward the target site and capability to plan a correction manoeuvre at very low altitude
- LIDAR, Camera, Altimeter become mandatory sensors to be added in the avionic architecture

Release and control rover modules for surface exploration

- Localization, navigation and experiments (i.e. terrain samples collection and analysis) require computational performance, high rate data bus link and data storage capability
- Significant data volume have to be transmitted towards orbiter, data relay spacecraft needed for communication with ground
- Autonomy in decision to be taken depending on contingency

Recovery and re-entry on ground of samples

- Rendezvous and docking or capture is a function needed to recovery samples
- Avionic has to be improved including dedicated sensors (NAC, WAC, LIDAR, RFsensor) and specific functionalities needed to optimise the propellant consumption in the different rendezvous phases.
- Significant computation power is required to solve on line optimization problems

EDL functional architecture

In SAGE study (EDL on Mars and Moon) required landing accuracy is 200m(Moon).

Guided entry is needed (Mars) and stringent requirements on vision based navigation are applicable

Absolute position estimation (Moon)

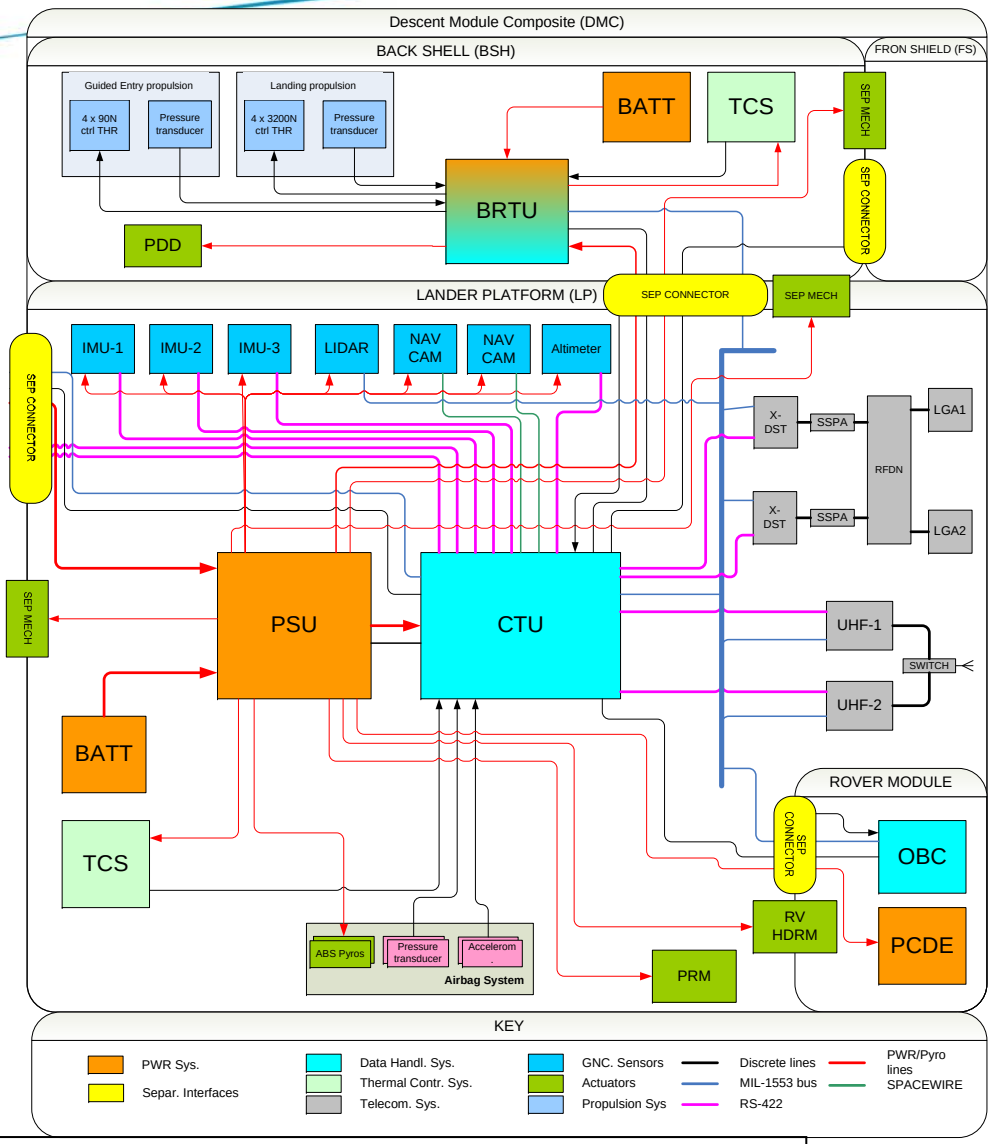
- from 50Km to 10 Km altitude
- 100 m accuracy each coordinate at 10Km altitude (eq. to 1% of altitude)

Relative position estimation

- from 10Km to 10 m altitude (Moon scenario)
- from 5Km (front shield jettison) to 10m (Mars scenario)
- 5% of slant range in the whole operative range
- 1m accuracy each coordinate at 10m of altitude

HDA design => Hazard Maps

- from about 1Km to 200 m altitude
- Roughness map
- Illumination map (Moon)
- Detect slopes higher than 10deg
- Detect rock higher than 0.5 m



Mars Precision Lander: EDM functional avionic architeture

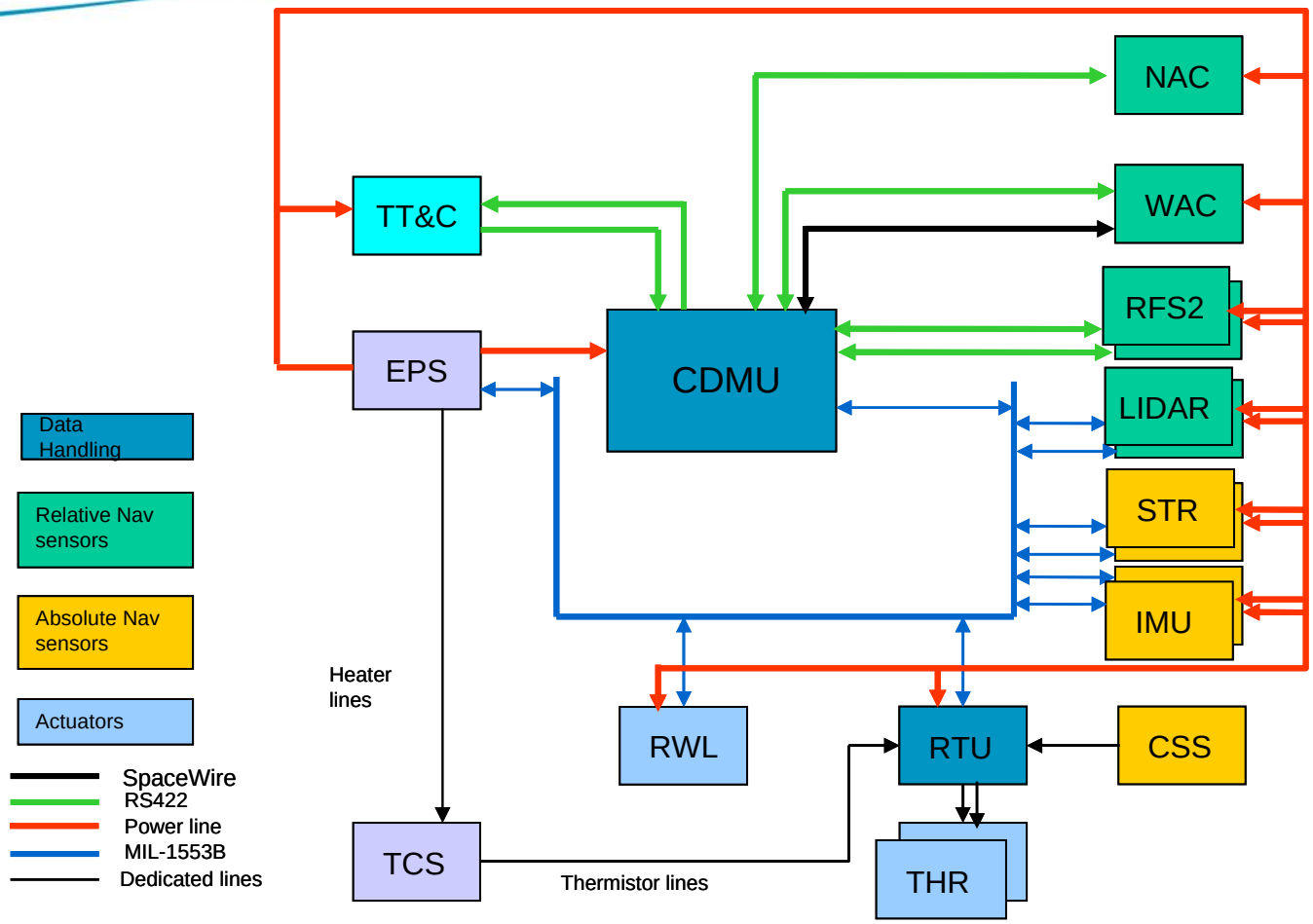
Rendezvous and Capture architecture

In ORCSAT study focus is on propellant saving in the different RDV phases

Model Predictive Controller Algorithms are used in all RDV phases (long range, intermediate range and short range) to solve on line optimization problems mainly related to the navigation function

Significant computational capability (MFLOPS) are required to the CDMU. Each 900 seconds no more that 30 second can be allocated to the MPC computation

Image Processing algorithms are used for the target detection (NAC) and for the terminal RDV phase (WAC)



ORCSAT : RDV and Capture functional avionic architeture

Rover Module Avionic architecture

The EXOMARS Rover Vehicle is required to survive and drive autonomously on the Mars Surface (100m every Sol)

Autonomous Navigation is based on Stereo Vision (3D Map Generation and Visual Localisation), thus high data rates for images acquisition (SpaceWire) and significant computational power are required

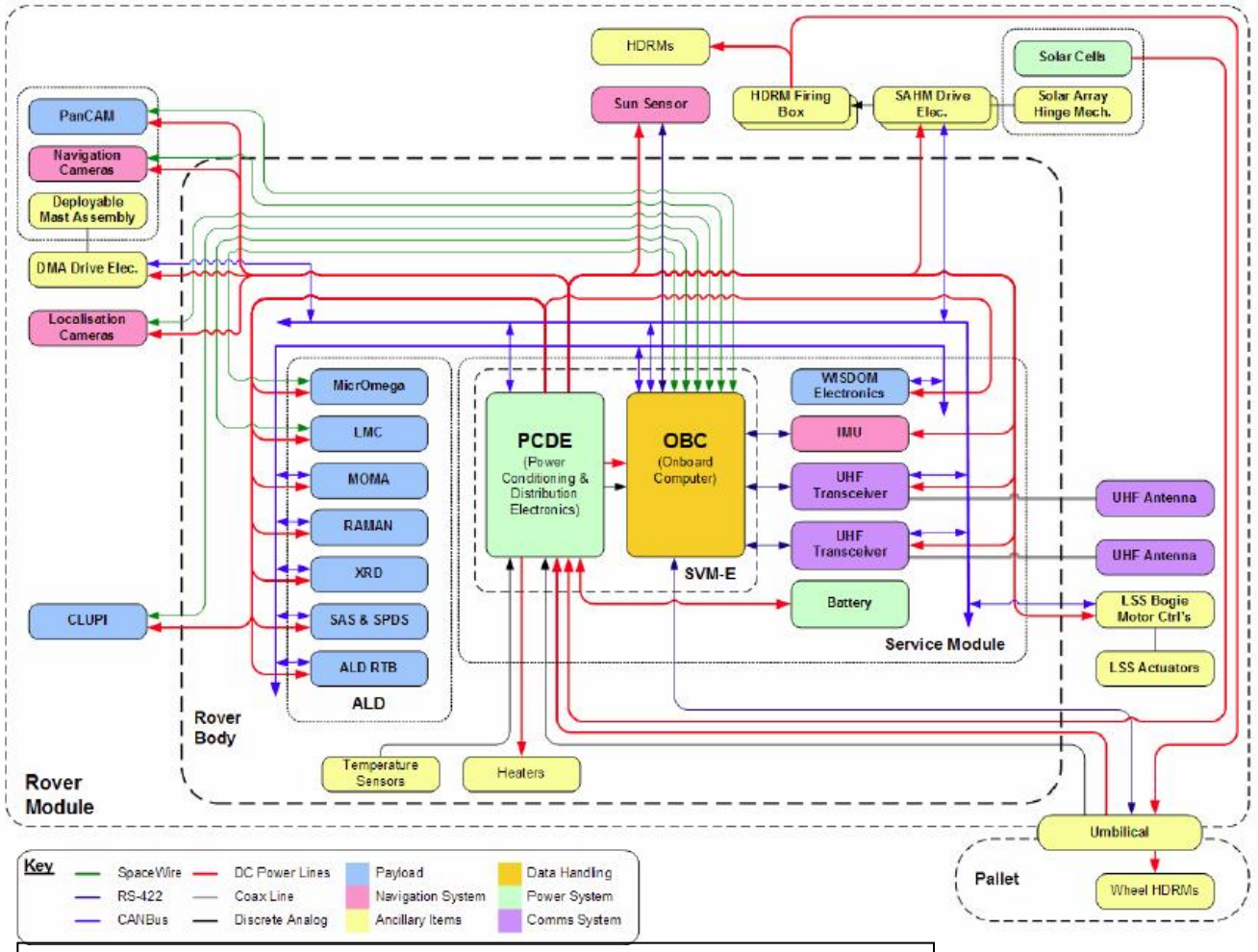
Required Performances:

Visual Odometry >0.1Hz

3D Map Generation (16m^2, grid size <4cm) in less than 120s

Precision after 100m travel +/- 6.8m and +/-5deg in heading

Upload to Earth of the needed information to select a new target (10x compression)



EXOMARS : Rover Module functional avionic architetcure

Common elements

Exploration avionics needs:

- **specific sensors (Cameras, Lidar, Altimeters (Radar or Laser)) to be tailored to the specific mission scenario**
- **specific algorithms (Image Processing, MPC controllers, Navigation filters) to be also tailored to specific mission scenario**

Common elements in all the architecture are:

- **CDMU with high computational performance (IP requires at least 1000 MIPS)**
- **and fast communication links with units generating significant data volume (LIDAR, Cameras)**

In the frame of ORCSAT, SAGE, VISNAV ESA studies the trade-off based on FPGA capability and available space qualified microprocessor has identified as the more powerful configuration:

- **processor-coprocessor configuration**
- **PCI and SpaceWire bus as the most suitable parallel and serial communication link for both inter-processor link and unit I/F link**

Common elements

PROCESSOR

In charge of all main functionalites (DH, Thermal, Electrical, TM/TC)

- **Currently space qualified processing units are based on LEON2 FT, its VHDL IP core can be included in dedicated SoC.**
- **Comparison between AT697F, SCOC3(LEON3 based), COLE(LEON2 FT based) is in favour of AT697F**
  - 86MIPS & 23MFLOPS @100Mhz
  - I/O I/F (DSU,2UART, GPIO, PCI) to be improved with dedicated FPGA

COPROCESSOR

In charge of specific algorithms computationally demanding (IP, MPC, GNC)

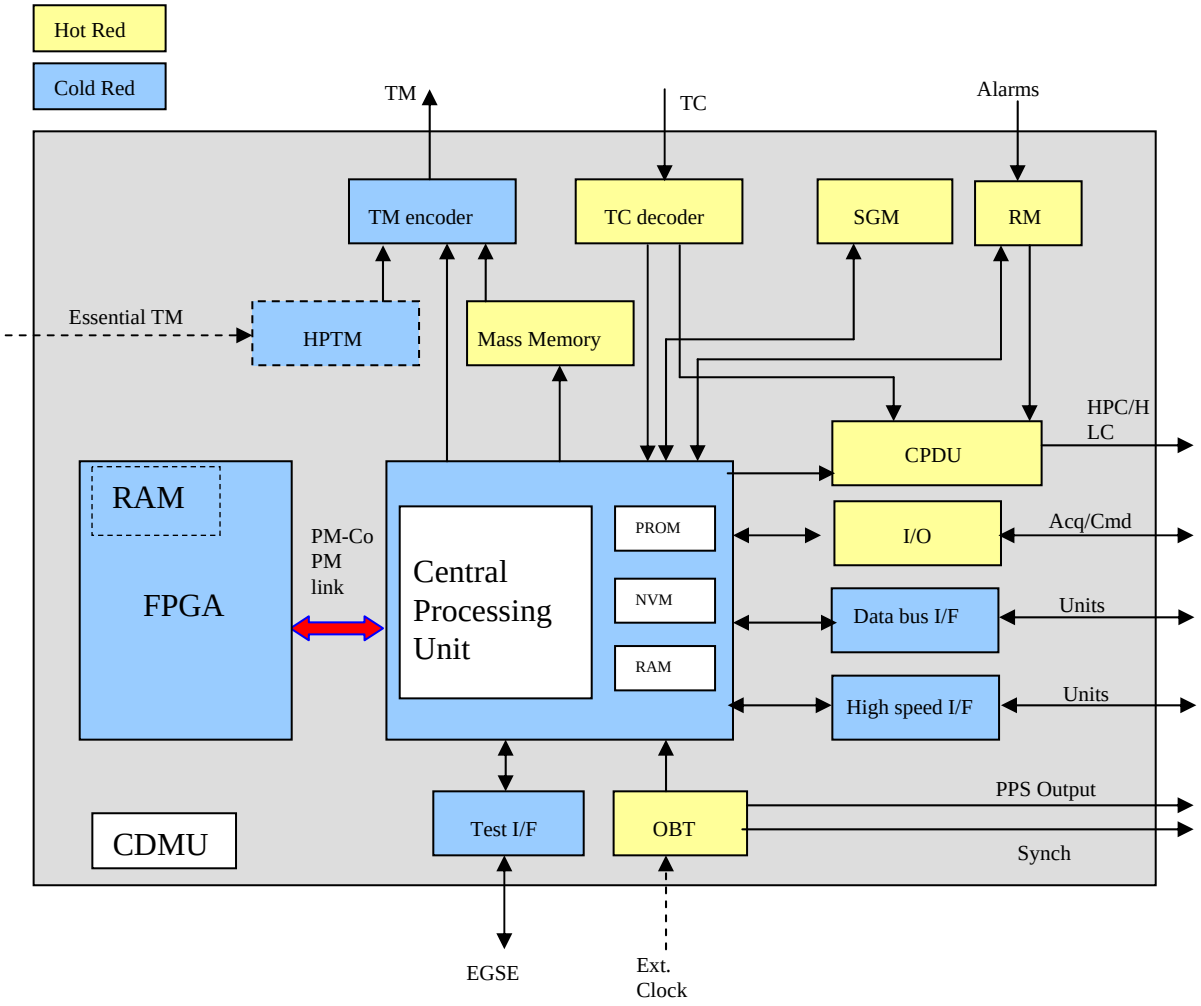
- **FPGA coprocessor**
  - Space qualified FPGA are available from Actel and Xilinx (Virtex4 and Virtex5). Both tolerate up to 300Krad (Si) of TID and declare a Single-Event Latch-Up Immunity (SEL) to LETTH > 117 (125 Virtex) MeVcm2/mg.
- **PowerPC coprocessor**
  - A flight qualified PowerPC is the RAD750 from BAE systems (Total dose: 1Mrad (Si), SEU: <1.6 E-10 errors/bit-day, Latchup-immune) with performance of 400 MIPS (Dhrystone 2.1) at 200 MHz. A more performing processor is the PowerPC750FX which has been used to design space qualified computer boards (Maxwell SCS750, MDA ESP750) with high computational performance (1650MIPS @ 733MHz).
  - A more powerful processor based on RISC technology is the PowerPC7448. It is manufactured on a 90nm SOI process and features 3000 MIPS (Drystone 2.1) at 1.3GHz (2.3MIPS/MHz). It has exhibited good behaviour under radiation and there is availability of up-screened versions from an European supplier: **e2v**

COMMUNICATION BUS

- Low speed communication link are MIL-1553B-STB and CAN bus (1Mbps). CAN bus can replace the MIL bus solving the relevant ITAR problems. TAS-I for the EXOMARS project is developing the CANOPEN protocol implementing the slaves in HW (IP core on FPGA) and Masters in SW.
- RS422 and RS485 are medium speed bus and can be used to set up a point to point full duplex link (up to 10Mbps)
- PCI parallel bus reaches 1 Gbps (32bit @33Mhz) therefore it is a candidate as inter-processor link
- SpaceWire (up to 200MBps) can be used to link LIDAR or Cameras to the CDMU

CDMU functional architecture: FPGA

- Specific algorithms of the GNC (MPC controllers or MPC solver for ORSAT) or IP algorithms (camera pose estimation for SAGE) could be implemented as HW solution programming a dedicated FPGA.
- FPGA can interface directly the central Processing unit via a dedicated co-processor link while all the other units are directly managed by the central processor. PCI is proposed as suitable interprocessor link.
- FPGA internal clock can reach a frequency of about 200MH nevertheless the achievable improvement in terms of computational throughput is strongly dependent from the implementation of the algorithms, in particular from the parallelism that can be obtained.

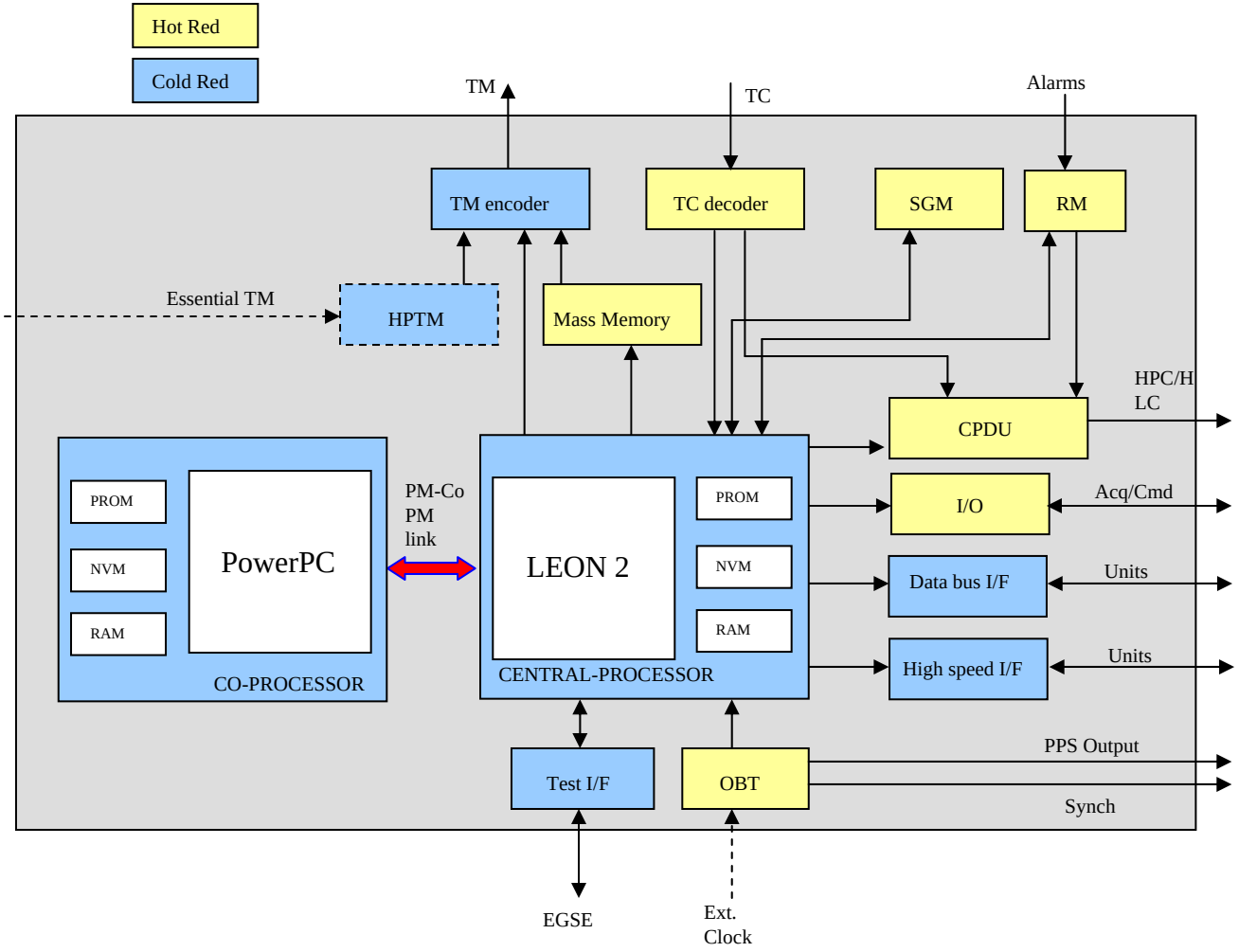


CDMU functional architecture : PPC

A more powerful configuration of the CDMU is based on a second processor directly linked to the central processor.

The on-board SW can be distributed on the two microprocessors leaving to the main processor the handling of the system units and to the coprocessor the execution of the algorithms requiring significant computational throughput (GNC or IP)

The selection of a general-purpose microprocessor gives less constraint to the SW development. A PowerPC RISC architecture is a suitable candidate



CDMU functional architecture: PPC+FPGA

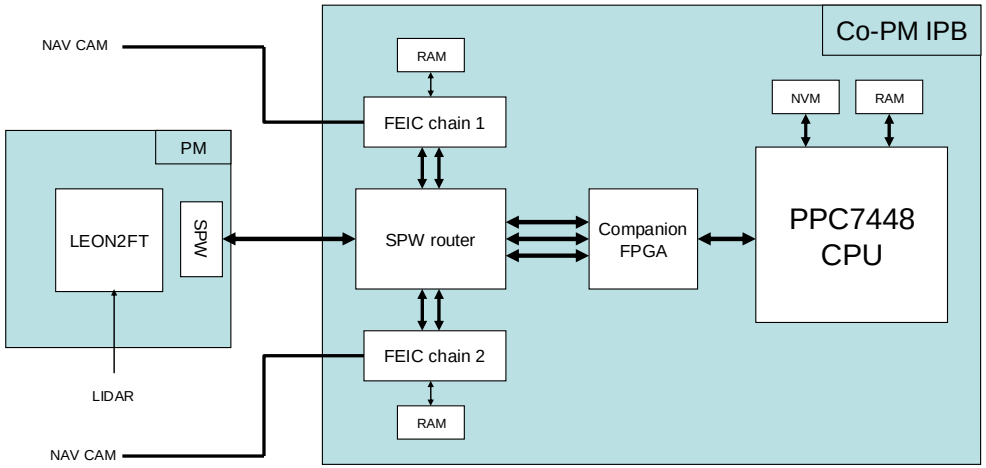
IP algorithms require the most powerful architecture. Coprocessor consists in FPGA and PPC integrated in a dedicated IP Board interfacing the central computer (LEON2FT) via SpaceWire router

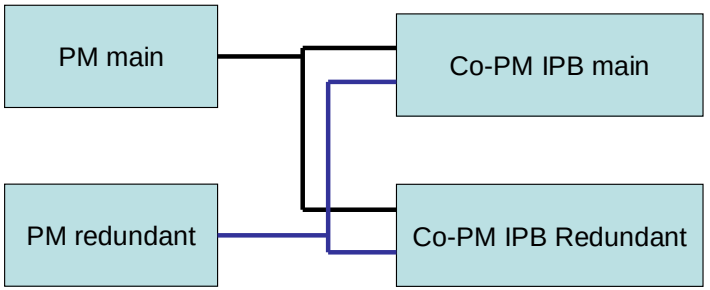
VISNAV architecture implements in FPGA part of the IP algorithms (FEIC) allocating to PPC processor (PPC7448) algorithms which cannot be efficiently implemented in the FPGA.

Navigation cameras are acquired and commanded by the IPB via SpaceWire while main processor (LEON2 FT) acquire final product of the IP algorithms needed by the GNC function and manage all the other GNC units. Central computer is also in charge of all the other system functions (DH, Thermal, Power, TM/TC)

Redundancy concept that can be applied to this architecture can consider PM main and redundant interfacing with both IPB co-processors.

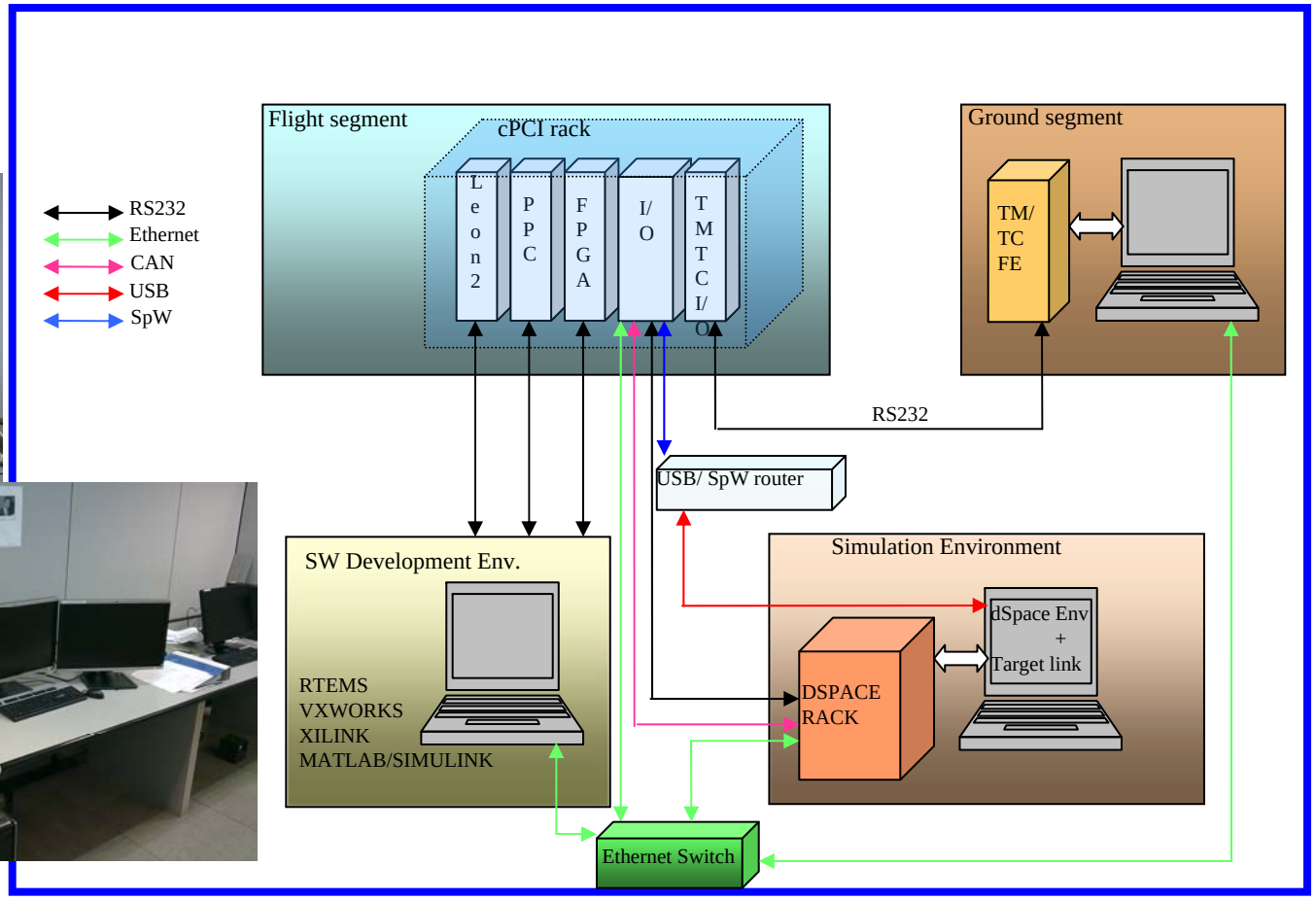
This architecture is applicable to different mission scenarios (EDL, ROVER, RDV)





Avionic Test Bench to support design

Trade-off between different configurations are feasible if flexible RT test bench is available in which communication bus, processor boards and SW algorithms can be integrated



Conclusion

TAS-I objectives to enhance the Avionics Architecture for the Exploration Missions are:

- **definition of a scalable avionic architecture adequate to the new demanding requirements of the exploration based on computer vision**
- **improvement of navigation algorithms using also on line optimization techniques which reduce the propellant budget needed to accomplisch the mission**
- **set up of a configurable and representative development and verification environment supporting trade-off and design of this scalable avionic architecture**