BUILDING BLOCKS OF NEXT GENERATION SPACECRAFT AVIONICS

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The proposed presentation treats the hardware architecture of the core functions and interfaces (TC, TM, processing, monitoring and reconfiguration) of a typical Spacecraft Management system, and how the main development steps have been taken for the past 10 years and a prediction for what seems to be happening for the next 5 – 10 years. Special focus will be put on the evolution of the main devices, from separate TM, TC, CPU, mass memory and I/O chips to today's System-on-chip versions and what can be expected from next generation System-on-chip. The most important aspect here is which functions and performances to include in a standard core and how to obtain a standard specification for these functions.

Performance Improvements

The performance improvement mainly deals with increased processing performance and increased memory size. For the future missions the LEON processor will be the most likely choice, possibly in some multi-core version. How can this increase in performance be used? Which is the best hardware architecture to support the Integrated Modular Avionics concept?

Communication links is another area where increased performance requirements are expected. For serial point-to-point links a performance of 100 – 200 Mbps can be assumed (in the payload even higher) while there is a problem with the performance of ordinary data buses (1553 and CAN) unless the space industry start to look at some of the new buses appearing in for instance the automotive industry.

Increased integration

The main way to reduce mass and power consumption is to improve the hardware integration level. Today the European space community is developing chips with most of the data handling functions integrated with the processor. With this high level of integration, questions like redundancy management and functional grouping on fault containment regions need to be solved and agreed between primes and equipment suppliers, and in close cooperation with ESA for operational aspects. A typical question here is: how much do we allow the TC Decoder and the Reconfiguration function to share resources with other parts of the Spacecraft Management core?

What are the other functions that may be integrated within the core? The available technology easily allows functions like uplink receivers, GPS/Galileo receivers and Star Tracker processors to be integrated within the core.

Mapping functions on physical units

The increased integration level also results in a need to reconsider the classical ways spacecraft are built with separate boxes that are delivered by different equipment suppliers. What was 10 years ago a box is now a single board or even just a part of a large chip. At the same time complex functions require large development resources and we still need to distribute the workload over the ESA member states. Thus, one might imagine that the boxes are becoming fewer but containing contributions from several companies. To ease this development some kind of standardised mechanical concept would be valuable, allowing smaller companies to maintain a product line of boards that can be supplied to several equipment suppliers.

For the functions not naturally part of the core, like various kinds of actuators and sensors with their electrical signal conditioning, the interface (both hardware and software) towards the core should be standardised. These functions may be integrated with the main avionics box or located in separate boxes, depending on physical accommodation capabilities, logistics and schedule as well as need for a good geo-return balance.