A Montium® Based Dynamically Reconfigurable Multi-Core for High Performance DSP Applications

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I. INTRODUCTION

Next generation digital signal processors must be flexible, energy-efficient, high performance and low cost. These conflicting requirements require a platform based design approach. Recore Systems provides semiconductor IP solutions for programmable systems-on-chip. The coarse-grained reconfigurable technology of Recore promises to satisfy all the conflicting requirements. The Montium® is a dynamically reconfigurable DSP core for programmable platform chips.

DSP applications require increasing processing power and are subject to ever changing standards. Application Specific Integrated Circuits (ASICs) for these applications are efficient, but inflexible and costly. Programmable architectures like General Purpose Processors (GPPs) or Digital Signal Processors (DSPs) do not have enough processing power for these demanding applications and are extremely power hungry. Field Programmable Gate Arrays (FPGAs) often perform better, but suffer from large configuration overhead and are still too power hungry and expensive for many applications.

The Montium is a domain specific coarse-grained reconfigurable architecture, which is both efficient and flexible within the DSP algorithm domain.

II. PROGRAMMABLE PLATFORM CHIPS

Tomorrow's multi-cores for (streaming) DSP applications will be interconnected by a network-on-chip (NoC) instead of a bus. Currently, most multi-core architectures rely on a central bus for interconnecting the (digital signal) processor cores. Such a central bus creates a major bottleneck and impedes performance, scalability and composability of such systems. A NoC approach does not suffer from these limitations. A NoC scales with the number of cores in the design. The more cores there are, the larger the network, and, hence, the more bandwidth available in the system-on-chip. Other advantages include that a NoC inherently supports short and structured wires, enabling increased clock rates and easier link optimization. NoCs allow disabling inactive parts of the network, which is essential for energy-efficiency and dependability. Finally, a key feature of NoCs is their predictable performance.

III. MONTIUM® TECHNOLOGY

Recore's Montium is a dynamically reconfigurable IP core for computational intensive DSP algorithms. The Montium can be used as an accelerator to offload DSP tasks from a GPP or in a heterogeneous multiprocessor system. ASIC-like performance and energy-efficiency is obtained by configuring the Montium with the functionality required by the algorithm at hand. The Montium can be reconfigured virtually instantly, as the size of the configuration binaries is very small. Yet, it has a low silicon cost, as the core is very small.

Next generation (reconfigurable) processors require a solid program development environment in order to be successful. Good tools enable swift development of new applications. Recore develops program development tools in synergy with its hardware cores. The integrated development environment (IDE) for Montium based platforms is called the Montium Sensation Suite. This comprehensive IDE includes compilers, simulators and the editors.

The Montium TP is a flexible core that can be used for digital signal processing applications. Typical target applications include communication systems (UMTS, WiMAX) and digital broadcasting systems (DAB, DVB).

IV. CONCLUSION

The Montium offers much more flexibility than an ASIC, while being much more energy-efficient than a conventional DSP. The Montium is almost as energy-efficient as an ASIC. However, the Montium can be dynamically reconfigured and different functions can be time-multiplexed on the same hardware. The Montium outperforms conventional DSP solutions in terms of energy-efficiency and performance. Recore's coarse-grained reconfigurable computing technology combines high performance, programmability, low power, and a small silicon footprint.