**Dynamically reconfigurable processor for space applications**

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During this session we introduce the XPP-III Signal Processor Architecture for space applications. The proposed processor is built from several building blocks which are glued with an on-chip communication framework. Data-flow based algorithms are processed by a reconfigurable coarse grained array of fixed-point ALUs and RAMs. Dynamic reconfiguration of the array allows on-the-fly change of the algorithm or sequencing of tasks. Most applications require also to deal with sequential code sections such as house-keeping tasks, protocol parsing, data compression or encryption. Those tasks are handled by specialized VLIW-like sequential processing cores. Each core features 2x4 16-bit ALUs and small local instruction and data caches The communication framework uses hardware dataflow protocols which automatically synchronize on-chip and off-chip communication channels. The progamming paradigm is completely based on C and APIs. Dataflow code sections can either automatically be vectorized or are coded using a descriptive language. All building blocks are available as cycle accurate simulation models. The combination of the coarse grained reconfigurable array, sequential processing cores and self synchonizing communication channels provides full programability, scalability and low power consumption for all on-board signal processing needs. All processor building blocks are built from standard cells and memories. Thus, porting to radiation hard processes is straight forward. The physical design can use an hierarchical approach. Finally, a high performance XPP-III processor for media server accelerators which is currently built is outlined. Based on this example an outlook about possible implementations for a future general purpose space processor is given.