RadSafe™ ASSP

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"Ramon Chips has developed the RadSafe™ technology for radiation hardened space ASICs, and has implemented a JPEG2000 image compression application-specific signal processor (ASSP), named JPIC, using that technology. RadSafe™ is a rad-hard-by-design technology. The chips are fabricated using a standard commercial 0.18u CMOS technology. Radiation hardness is achieved by layout, circuit and logic design methodologies. The technology has been shown to achieve hardness to TID above 300 KRad, no latch-up at above 100 MeV-cm2/mg and high SEU tolerance, yielding effective SEU rate of less than one event in hundreds of years in relatively large ASICs. EDAC is applied to on-chip Rad-Hard SRAM blocks to provide similar SEU hardness to memories. A Rad-Hard all-digital DLL is used for frequency multiplication and de-skewing, eliminating the high sensitivity to SET in analog PLLs. A library containing logic standard cells, memories, I/O (including 5V tolerance, Cold-sparing, LVDS and SSTL) and special cells has been developed and verified in radiation and qualification tests. The JPIC ASSP is based on a JPEG2000 IP core from Alma Technologies of Greece, and on additional logic for custom high speed interfaces. It is capable of image compression at close to 50 Mpixel/second, 12 bits/pixel, and dynamic reconfiguration. It operates at close to 100MHz and interfaces two SDRAM components for temporary data storage. JPIC includes more than 4Mbit SRAM bits in about 150 embedded cores, and optimized data-path logic. The ASSP is presently being validated at full speed on a Stratix II FPGA in a full system, and is expected to be fabricated in early 2008. Future generations of the ASSP will incorporate Tier-2 of the JPEG2000 standard, as well as offer JPEG-LS compression. Ramon Chips is also applying the same RadSafe™ technology to other ASICs, both programmable processors and custom ASSPs."