**High perf. ASIC platform approach for next satellite telecom processors possible application to other processors**

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Digital Processing functions implementation needs very high integration silicon technology to handle multi-Gbit/s data streams processors of millions gate complexity. For terrestrial applications, such devices are today produced in 90nm and developed in 65nm CMOS for production in 2008. Next Generation Space Processor could take benefit of such advanced technology if Radiation, Reliability and Cost issues specific to Space environment are solved. From many discussions and round table with agency and Industrial Space primes, ST is now in position to propose a 65nm CMOS ASIC technology which brings solutions to the identified issues specific to next space telecom applications. The purpose of the talk is to summarize ST development plans submitted to ESA and EC approval. First the needs in terms of processing capability, memories and very high speed interfacing will be discussed as well as space constraints of reliability and radiation robustness. Then those targets will be analyzed versus Deep Sub Micron 90nm and 65nm generation technologies. Specific emphasis will be given to the recent 65nm node with its intrinsic performance overhead. Reliability and radiation robustness capabilities of ST 65nm CMOS will be discussed with the associated Design for Reliability methodology. The ASIC development cost in such advanced technology is a severe issue that will be completely discussed. ST proposal of ASIC-platform development with Metal customizable logic arrays and fixed high performances IP blocks will be presented. Significant cost reduction at development, test and qualification level will be demonstrated with such fixed “structured ASIC” approach. Several tens of State of the art 7.5Gbit/s ST proprietary High Speed Serial Links, HSLL blocks will also be implemented inside the IC-platform to allow backplane and cable high speed interconnectivity of Asics or very high speed data-converters. The first 65nm ASIC platform foreseen development will target Next generation telecommunication satellite payloads processor with high level of parallelism and throughput optimized distributed processing. Nevertheless other applications could be addressed with the integration of robust multi DSP cores and different usage of the HSSLs with the obvious benefit of reuse of a space qualified process, test and packaging solution. Some experienced DSP IP core embedding will be shown to illustrate this possibility. With such space matched technology, High performance IP portfolio and partnering willingness, ST can also be an important partner in the field of Digital processors for space applications.