LEON COPROCESSOR FOR PAYLOAD DATA PROCESSING

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Past and present missions as well as trend analyses clearly show the constant increase of the needs in term of on-board data processing. The spacecraft payloads have to execute more and more operations on-board while coping with limited resources as the bandwidth to the Ground. Moreover, these data processing operations tend to be specific to each mission. The Leon processor in its different versions aims to become the standard in space applications. Its characteristics make it configurable and versatile. Nevertheless, if its performance regularly increases, the Leon processor is not sufficiently powerful to match real-time constraints of the most demanding data processing operations. On the other hand, the implementation of data processing operations fully in hardware can be difficult, consume many resources and is expensive. The development of Leon coprocessors is guided by the objectives to take benefits of the versatility of the Software and the performance of the Hardware. By implementing critical data processing in Hardware and less critical and generic parts in Software, it becomes possible to match the performance and the flexibility requirements while ensuring a control of the costs.

Strong of its experience in space systems, Astrium Satellites has initiated an internal project to study the feasibility and interest of developing co-processors for the Leon with the support of the AED SME. The first phase of this project focused on the coupling of a DSP processor to the Leon. However, the versatility and performance of existing flight DSP processors clearly appear very limited when compared to modern FPGA components. As a result, a second phase has been recently initiated and aims to define, to characterize and to experiment different interfaces between a Leon processor and one or several dedicated hardwired functions for internal (Leon and dedicated functions in a same component) and external (Leon and dedicated functions in distinct components) connections. A versatile interface module is being developed and characterized on a FPGA in which a Leon3 processor interfaces a generic configurable numerical operation (convolution).

The interface module will later be included in an experimentation case study representative of on-board advanced processing. The hardware software partitioning of a complex hardwired function already developed for a space mission. This function will be re-visited in order to optimise the data processing budgets. Indeed a major objective is the reduction of the complexity of the Hardware design in order to make it compatible with a flight technology while ensuring the correct level of performance and reduced costs. A key to success is the performance of the interface between the Leon executing the software and the hardwired function.