use of Texas Instruments' DSP in Space Programs

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CGS has designed several boards and units based on DSPs for space applications:

Ø MITA P/L Computer (ASI mission, launched June 2000)
Ø SarLUPE SMU (Spacecraft Management Unit for SarLUPE constellation of satellites, two satellites already launched)
Ø Herschel DPUs/ICU (Data Processing Unit/Instrument control Unit for the ESA Herschel Mission)

The central core of all the mentioned units is the DSP TSC21020 manufactured by ATMEL-TEMIC. This DSP provides a theoretical performance of 60 MFLOPS (Peak) /40 MFLOPS (Sustained) when clocked at 20 MHz.
The DSP from ATMEL represents the state of the art of the available space qualified DSPs and it has also the feature to be ITAR free (ATMEL is an European manufacturer) but nevertheless its performances are clearly undersized if compared with the ones required by the future space missions. For example this is the case of the GAIA Video Processing Unit (ESA ITT AO70059 February '07) where the processing capability, required by the mathematical algorithms to be executed on the data generated by GAIA Telescopes CCDs, is well above the performance reachable using the TSC21020 or a Leon 2 processor (at least in a single-core implementation).
The baseline reference computer suggested by the customer in GAIA was the Maxwell SCS750TM CPU board designed and developed by Maxwell Inc and based on a PowerPC-750F processor that is a General Purpose Processor (GPP) able to provide up to 1800 MIPS. CGS has proposed a different solution based on the SpaceMicro Inc. (SMI) Proton200K™ board, a 3U cPCI board built around the Texas Instrument TMS320C6415T Digital Signal Processor, with Time Triple Modular Redundancy (TTMR) and H-Core technology for the mitigation of radiation effects. The TMS320C6415T is able to provide up to 4000 MIPS at the maximum clock frequency with a power consumption of only 8 W. CGS is firmly convinced that DSPs are characterized by a proven superiority w.r.t the GPP in signal-processing applications (as stated also by benchmarking from independent authority like EEMBC' TelemarkTM). The DSP's design is optimized more for the execution of instructions and data-handling operations and in general algorithms that are used more frequently when manipulating large amounts of data in repetitive and analytical ways (such as that used by the VPU for GAIA), hereafter a brief summary of the high-enabling technologies implemented into the DSP is listed:

• Single-cycle Multiply/Accumulate (MAC)
• Deep pipelines
• Parallel processing
• Multiple memory access with Harvard architecture
• Zero overhead looping
• Hardware circular addressing for circular buffers

CGS has analyzed the last 320C6xxx generation of DSPs from Texas Instruments (TI) as a possible processor solution for the future space P/L computers but also as a processing platform for OBDH where the AOCS SW tasks requires a significant floating point calculation capability. The 320C64xx part number defines the fixed point digital signal processor sub-family of TI, while the 320C67xx code defines the floating point digital signal processors.
In particular the TMS320C67x™ floating-point DSP thanks to its high performance in term of MFLOPS, memory access speed and low figure of power consumption appears to be the best candidate for a CGS custom made CPU board. Details and an architectural block diagram of the CGS custom made CPU board will be presented. The SM320C6701 family's component is available also as MIL-PRF-38535 QML-V version in a ceramic package, 5962-9866101VXA. Data related to the radiation hardness of this device are available on the TI website *, where the declared minimum Total Dose for Gamma rays is 100krad (Si). The component is also not susceptible to SEL up to tested LET of 89 MeV-cm2/mg. For the SEU a rate of 7.6E-03 upsets/device-day in GEO Orbit has been measured.