Memory Technology Trends and Qualification Aspects

ESA Workshop on Avionics Data, Control and Software Systems (ADCSS)
23-25 October 2012, ESA/ESTEC, Noordwijk, The Netherlands

Institut für Datentechnik und Kommunikationsnetze, TU Braunschweig

Addressed Topics

F. Gliem, D. Walter, K. Grürmann, M. Herrmann
Memory Technology Trends and Qualification Aspects

Addressed topics

- Memory technology selection,
  current situation and outlook
- Characterization of the radiation sensitivity,
  some specific aspects of 16/32-Gbit SLC NAND-Flash and
  4-Gbit DDR3 SDRAM
- Test challenges,
  some examples
- References

Technologies for Space Memories

Technology			Die Density bit/cm²	R/W ns	Non-volatile	TID krad	SEE	Gbit Main Memory	Gbit Safeguard Memory	Tbit Mass Memory
Standard	SRAM	comm.	256M	2	no	> 30	!			
		hard	64M	15		200		X		(X)
	SDRAM	DDR3	4G	2		> 200 [3]	m.b. EC			X
		LP-DDR2	4G	3		> 200				X
	Flash	NOR	1G	10 / 10^4		70			X	
		NAND SLC	16G	15 / 80	yes	70 [1,2]	m.b. EC		X	X
		NAND MLC	128G	20 / 200		70 [1,2]			(X) 3000 program cycles	
Advanced	MRAM S.T.T	comm.	64M	35	yes	30?	1)			
		hard	32M	50		100 [4]		(X)	X	(X)
	PCM	comm.	512	2 / 200		30				
		hard	4M	70 / 1000		500			(X)	

m.b.EC: manageable by Error Correction

1) no SEE generation if non-powered, storage cell is SEE immune, only peripheral circuitry is prone to SEU / SEFI

D > 100 krad: LP-DDR SDRAM, DDR SDRAM

D < 100 krad: NAND-Flash ↔ LP-DDR SDRAM, SRAM?, hard MRAM?

SDRAM / Flash Array Power Consumption versus Data Rate (1)

NAND-Flash ↔ LP-DDR SDRAM

The power consumption of the memory array is a very basic criterion

Main assumptions for a strongly simplified model:

(i) $C_{net,\ nom}$ = 1 Tbit

(ii) Contribution of the additional capacity for EC is not taken into account

(iii) Contribution of I/O power is not taken into account

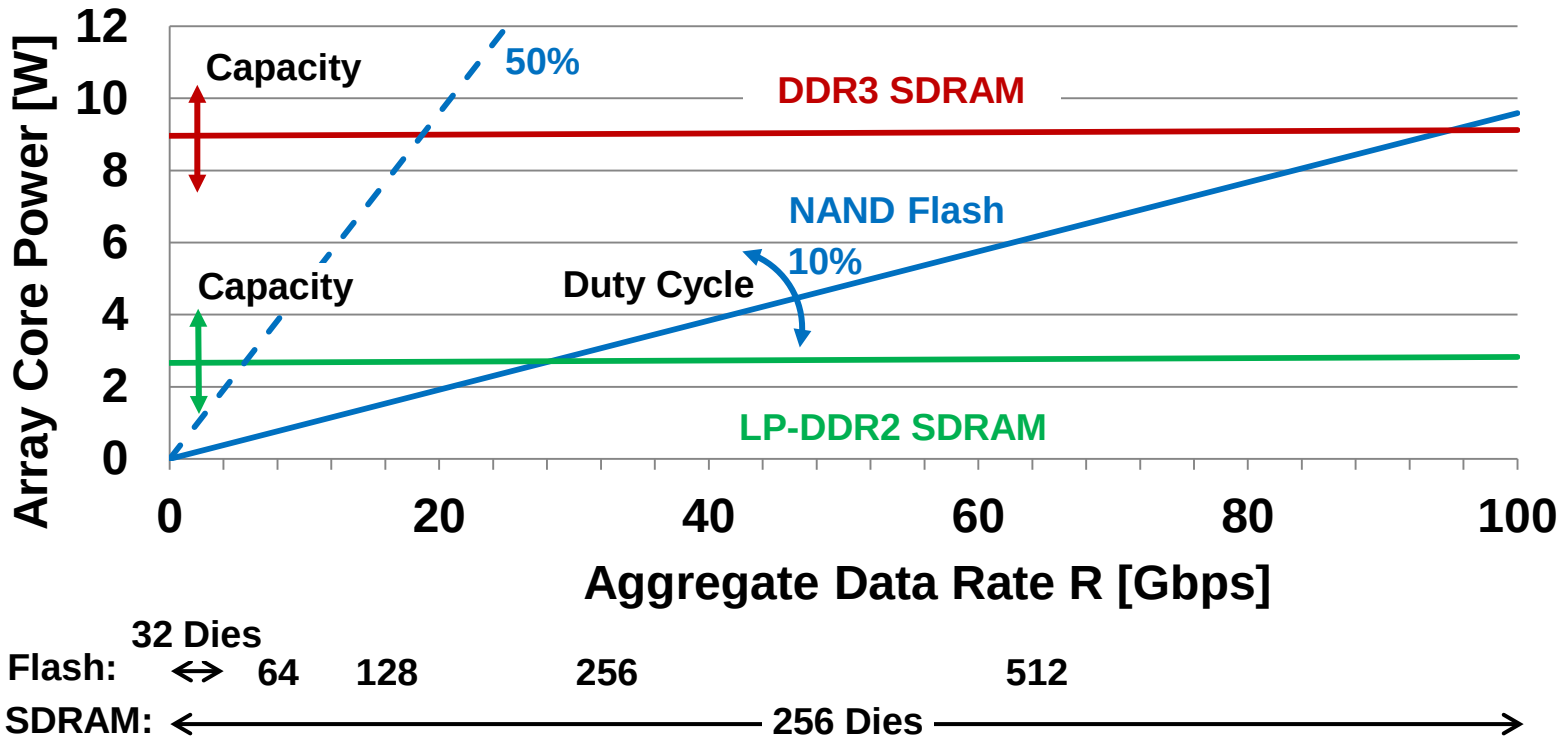
(iv) Same data rate for quasi-simultaneous Data Record and Data Replay

(v) Activity duty cycle: 10 % or 50 %

(vi) For high data rates the net capacity of the Flash-array is expanded so that in round robin operation with 10% duty cycle the cells exercise 60,000 write operations within 10 years → 32 dies @ < 3.9 Gbps aggregate data rate,
64 dies @ < 7.8 Gbps, a.s.o.

(vii) Until 5.4 Gbps 32 Flash dies are operated in parallel, for higher data rates the respective multiple of dies.

SDRAM / Flash Array Power Consumption versus Data Rate (2)



The power consumption of the 256 SDRAMs is determined by their consumption in idle state. Only few of the 256 dies are active at a time → only weak power increase with the data rate on top of the quiescent power of 256 dies.

The power consumption of idle Flash devices is zero. The average array power increases in proportion to both, the data rate R and the activity duty cycle dc.

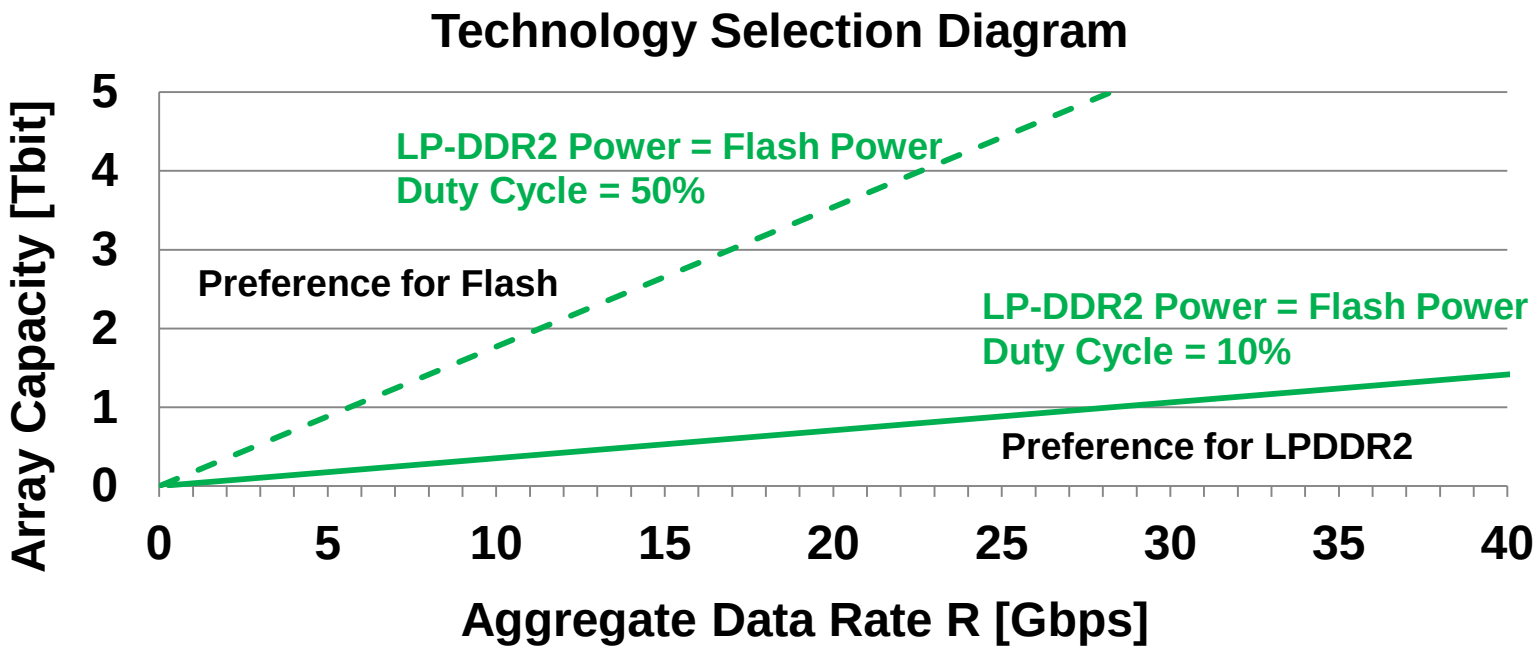
SDRAM / Flash Array Power Consumption versus Data Rate (3)

DDR3 SDRAM beats NAND-Flash only at excessively high data rates:
C_{net} = 1 Tbit : R > 90 Gbps @ dc = 10% activity, R > 18 Gbps @ dc = 50%

LP-DDR2 SDRAM delivers a significantly lower power consumption.

It beats NAND-Flash for $R * dc > 2.8\ Gbps * C_{net}[Tbit]$; $C_{net}[Tbit] = R * dc / 2.8\ Gbits$

Most applications: $R * dc < 2.8\ Gbps * C_{net}[Tbit] \rightarrow$ NAND-Flash



Recommendations for memory technology selection

Recommendations:

Based on the current situation, and anticipated that LP-DDR SDRAM show a tolerance dose and SEE characteristics comparable to DDR SDRAM, we see the following trends:

i. LP-DDR provides a significant advantage compared to DDR.

ii. For memories of D > 100 krad LP-DDR SDRAM is the first choice and DDR SDRAM the background solution.

iii. For the majority of mass memory applications (D < 100 krad and R * dc < 1.8 Gbps・C [Tbit]) NAND-Flash is the first choice.

For low capacity memories SRAM or hard MRAM might be an alternative.

Outlook

Will an Advanced Technology become of relevance for mass memories?

Very likely not within the next four years.

Will the density of NAND-Flash increase furthermore?

Some indications that topological shrinking comes to its end, because the Si-layer below the FG can not be thinned even more.

But, stacking of these low frequency planar structures is rather easy, either by conventional stacking of separate dies or monolithically by stacking of several functional layers on top of a single substrate.

We expect an increase of the SLC NAND-Flash device capacity in pace with DDR SDRAM, roughly doubling every 2 – 3 years.

Radiation Sensitivity

Radiation Testing of Memory Devices

SDRAM and Flash are available only as commercial parts, which have to be qualified for space use.
Radiation sensitivity imposes the most prominent restrictions for the use of commercial parts in space.

TID imposes an absolute limit. In contrast to SEE it can not be mitigated by structural means such as redundancy applied in the manifold methods of EC.

TID, DDR3 SDRAM

In general, TID improves with scaling,
because the thickness of the charge collecting gate oxide decreases.

State of the art SDRAM showed very favorable tolerance doses.
Co-60 tests of non operated DDR2 SDRAM with pauses after the irradiation steps for device testing delivered tolerance doses of several 100 krad [3].

An in-situ high dose rate test (80 rad / min) of the Samsung 4-Gbit DDR3 SDRAM is under way at the ESTEC facility.

More then 200 krad have been reached already without severe error occurrences (one row error, few SEUs).

TID tests of LP-DDR devices are still missing.
Most likely the TID characteristic of DDR3 and LP-DDR2/3 is quite similar.

TID, NAND-Flash

NAND-Flash are more TID sensitive than SDRAM.

In high dose rate tests (140 rad / min) distributed SEUs start at about 50 krad. Between 100 and 200 krad the share of SEUs increases to about $1 \cdot 10^{-3}$.

At early SLC devices we observed that the erase operation failed in the dose range of 70 – 120 krad.
F. Irom found erase failures of 8-Gbit Samsung SLC not before 250 krad.

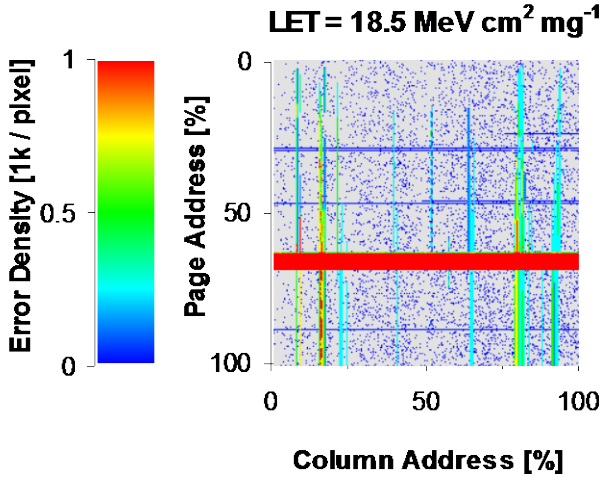
High dose rate TID tests of 16/32-Gbit Micron SLC NAND-Flash are planned for the first quarter of next year.

Possibly low dose rate tests could deliver results, which are even more favorable and more relevant for the space environment.

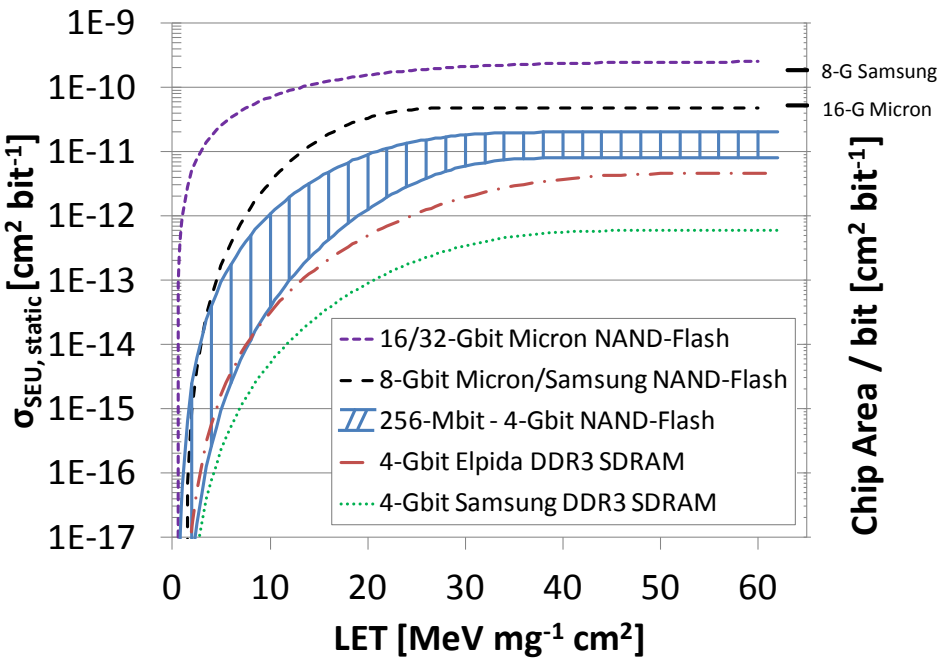
SEE Error Classification

SEE error pattern

- Class A
  - Random SEU
    - Single Bit Error
    - Multiple Bit Error
    - Single Symbol Error
    - Stuck bit, etc.
- Class B
  - Transient SEFI
    - Row
    - Column
    - Block, NAND-Flash only
- Class C
  - Persistent SEFI
    - Row
    - Column
    - Block, NAND-Flash only
    - Device
- Class D
  - Flash
    - Device Failure
      - SDRAM
        - C1; Removable without data loss
        - C2; Removable with potential data loss
        - C3; Removable only with data loss (PC)



SEE Sensitivity



ERROR RATES FOR 1 AU ORBIT

		GCR (ISO, quiet)	Solar Flare Worst Week
Micron 16-Gbit NAND-Flash			
Random SEU	[bit/day]	$1.7 \cdot 10^{-9}$	$3.8 \cdot 10^{-6}$
Word Error Rate[a]	[word/day]	$8.3 \cdot 10^{-15}$	$4.2 \cdot 10^{-8}$
SEFI	[dev/day]	$5.5 \cdot 10^{-3}$	$5.1 \cdot 10^{+0}$
Elpida 4-Gbit DDR3 SDRAM			
Random SEU	[bit/day]	$1.1 \cdot 10^{-11}$	$8.4 \cdot 10^{-10}$
Word Error Rate[a]	[word/day]	$3.4 \cdot 10^{-19}$	$2.0 \cdot 10^{-15}$
Class C, Device[b]	[dev/day]	$4.2 \cdot 10^{-5}$	$3.8 \cdot 10^{-2}$
Class C, Device[c]	[dev/day]	$2.2 \cdot 10^{-6}$	$2.5 \cdot 10^{-3}$
Samsung 4-Gbit DDR3 SDRAM			
Random SEU	[bit/day]	$1.6 \cdot 10^{-11}$	$1.4 \cdot 10^{-9}$
Word Error Rate[a]	[word/day]	$7.0 \cdot 10^{-19}$	$5.5 \cdot 10^{-15}$
Class C, Device[d]	[dev/day]	$4.0 \cdot 10^{-6}$	$7.3 \cdot 10^{-3}$

[a] post correction
[b] without periodic reinitialization
[c] with periodic reinitialization
[d] no change by reinitialization

4-Gbit DDR3 SDRAM is less SEU sensitive than 16/32-Gbit NAND-Flash. Using single symbol correcting RS EC the SEUs should be no matter of concern.

The average BER is determined not by SEU – SEU coincidences, but by uncorrectable coincidences between a rare, but extended SEFI error pattern in one device of the WG and SEUs in the other devices.

Word Group WG

What is a Word Group WG?

n 512M x 8 devices store 512 M code words of *n-2* data bytes.
Each code word comprises 2 parity bytes.

These *n* devices constitute a single WG.

The EC is performed on WG level.

The WG constitutes the smallest self-contained and reconfigurable portion of memory cells.

Device SEFI of DDR SDRAM

SEFIs produce extended error pattern.

Occasionally DDR3 SDRAM experience a persistent Device SEFI. The SDRAM function is locked and all addresses deliver erroneous data. Then each SEU within another device of the affected WG produces a non-correctable error.

Apparently the Device SEFI should be detected and removed by power cycling as early as possible, before SEUs in the other WG devices accumulate.

In the ideal case only the affected device would be power cycled. Then the EC would restore the data in the course of a scrubbing cycle.

In reality, a power switch serves one or even several WGs. Before power cycling all data of the commonly supplied WGs has to be swapped to empty WGs.

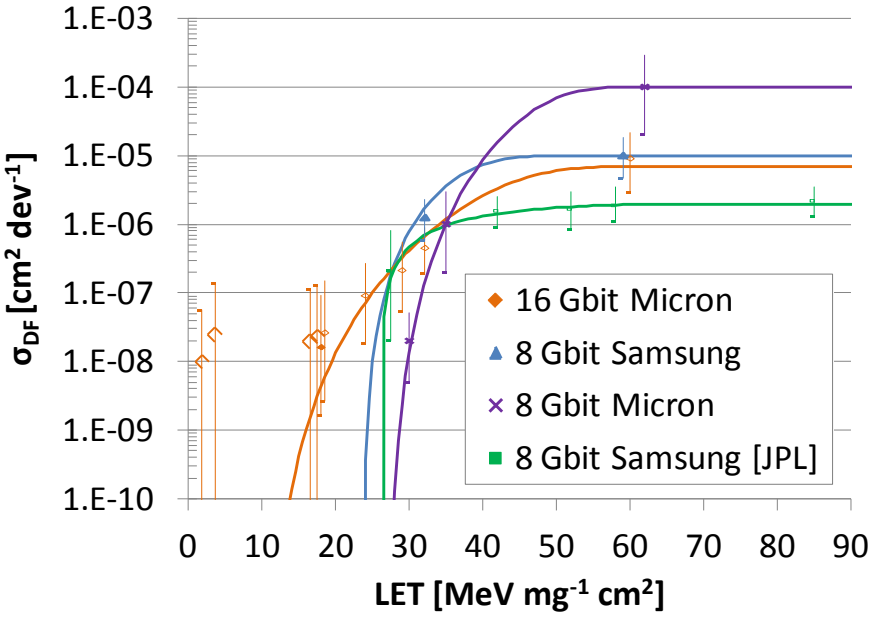
Destructive Failure of NAND-Flash

Flash devices suffer from rare Device Failures DF, which cause a permanent breakdown of the device.

Erase and Write is no more working, but often Read still works.

The failure originates from a gate rupture of a transistor in the high voltage generator / distribution, and is induced by a single high LET ion.

Data rescue is similar to the SDRAM Device SEFI situation.



1AU GCR
Average time
to 16-Gbit NAND-Flash DF: 1200 years/dev
to 4-Gbit DDR3 Device SEFI: 700 years/dev

100 devices / memory → 1 year / memory

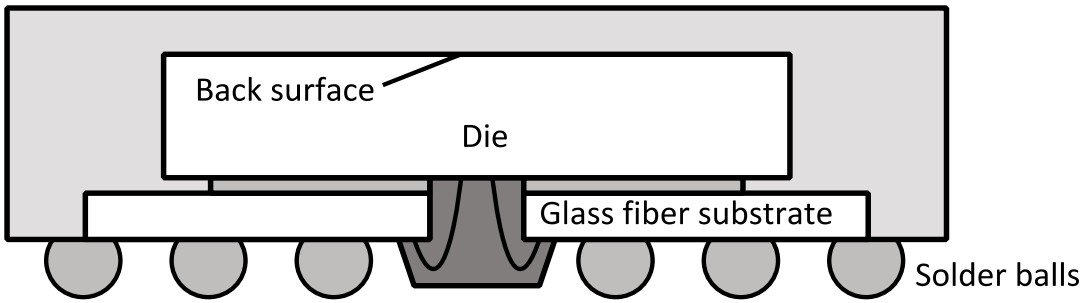
Test Challenges 1

Test Challenges

Some examples out of a large catalogue:

(i) Non-sufficient range (energy) of the heavier test ions necessitates die thinning.

Krypton range at RADEF 9.3 MeV/n: 94 µm,
at A&M 25 MeV/n: 250 µm.



DDR SDRAM dies are packed bottom-up in a BGA casing. The active surface is covered by the solder balls and the interfacing glass fiber substrate. Therefore the die has to be irradiated from its backside. The thickness of the die varies between 200 and 350 µm. To reach at RADEF the sensitive volumes in the active zone the die has to be thinned down to 60 ± 5 µm.

Test Challenges 2

The difficulty is that the die and the residual plastic casing warp by e.g. 30 µm as soon as the cover plastic is removed [9].

(ii) For the DDR3 SDRAM test with DLL ON at 330 MHz clock and 660 MHz data frequency a tailored memory controller and test board was designed and built. In particular it controls the periodic insertion of command sequences for DUT re-initializing in order to check whether the frequency of SEFIs can be reduced by the so-called „S/W Conditioning“. This effort took more than one man year. One test result was that „S/W Conditioning“ is effective for 4-Gbit Elpida devices, but not for 4-Gbit Samsung devices [10].

(iii) The in situ TID test of DDR3 SDRAM until 200 krad requires a shielding equivalent to 5 cm lead of the memory controller and test board, which has to be located as tight to the DUTs as possible to guarantee the fidelity of the high frequency signals.

Test Challenges 3

(iv) An in-situ low dose rate test of NAND-Flash the DDR3 SDRAMs is desirable. Personal attendance for test monitoring over weeks is not feasible. The test bench is prepared for unattended operation.

(v) The available beam time is never sufficient to investigate all relevant effects thoroughly.

Acknowledgment
We appreciate much the efficient and friendly support by Véronique Ferlet-Cavrois and her understanding of the difficulties of experimental work, and also the well-established cooperation with our friends at Astrium Friedrichshafen.

References and Recent IDA Test Results

[1] F. Irom et al., “Evaluation in Mechanisms in TID Degradation and SEE Susceptibility of Single- and Multi-Level High Density NAND Flash Memories”, IEEE Tr.Nucl. Sci.vol. 58, No.5, Oct. 2011

[2] F.Irom et al., “Scaling Effects in Highly Scaled Commercial Nonvolatile Flash Memories”, IEEE NSREC 2012, W-15

[3] R. Ladbury et al., “Effects of Bias, Electrical and Thermal Stress on DDR2 SDRAM Total Ionizing Dose Response”, IEEE NSREC 2012, PG-2

[4] C. Hafer et al.: “SEU, SET and SEFI Test Results of a Hardened 16Mbit MRAM Device”, IEEE NSREC 2012, W37L

[5] K. Grürmann et al., “SEU and MBU Angular Dependence of Samsung and Micron 8-Gbit SLC NAND-Flash Memories under Heavy-Ion Irradiation”, IEEE NSREC Data Workshop, W-24, 2011

[6] K. Grürmann et al. “MBU characterization of NAND-Flash Memories under Heavy-Ion Irradiation”, RADECS 2011

[7] M. Herrmann et al., “Heavy ion SEE test of 2 Gbit DDR3 SDRAM”, RADECS Data Workshop, 2011

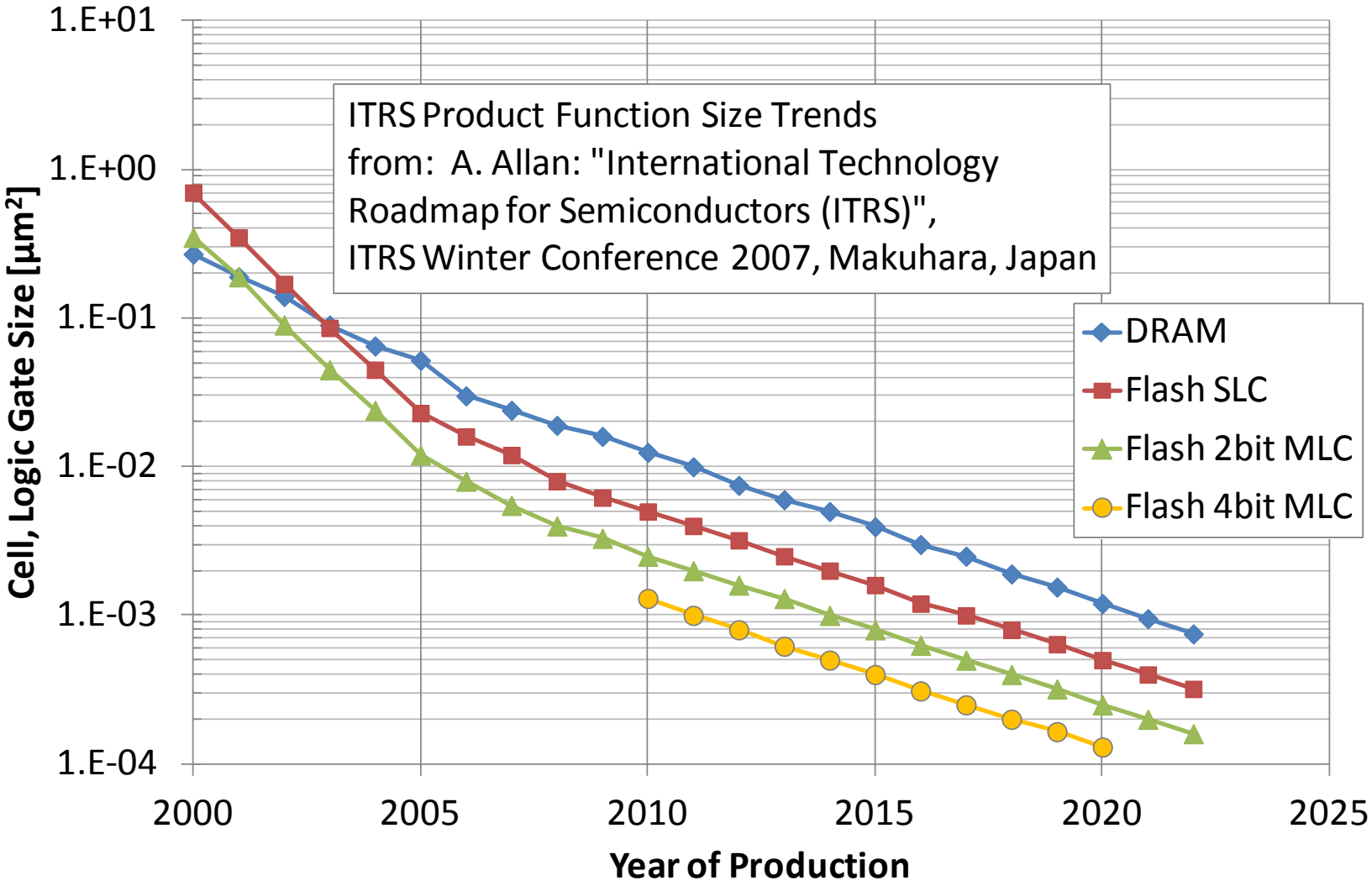
[8] K. Grürmann et al., “Studies of Radiation SEE Effects in NAND-Flash and DDR Types of memories”, ESA R&D Final Presentation Days, 2011

[9] K. Grürmann et al., “Heavy Ion sensitivity of 16/32-Gbit NAND-Flash and 4-Gbit DDR3 SDRAM”, NSREC 2012 Data Workshop

[10] M. Herrmann et al., “New SEE Test Results for 4 Gbit DDR3 SDRAM”, RADECS Data Workshop, DW-25L, 2012

[11] K. Grürmann et al., “New SEE Test Results of 16/32-Gbit SLC NAND-Flash”, RADECS Data Workshop, DW-23L, 2012

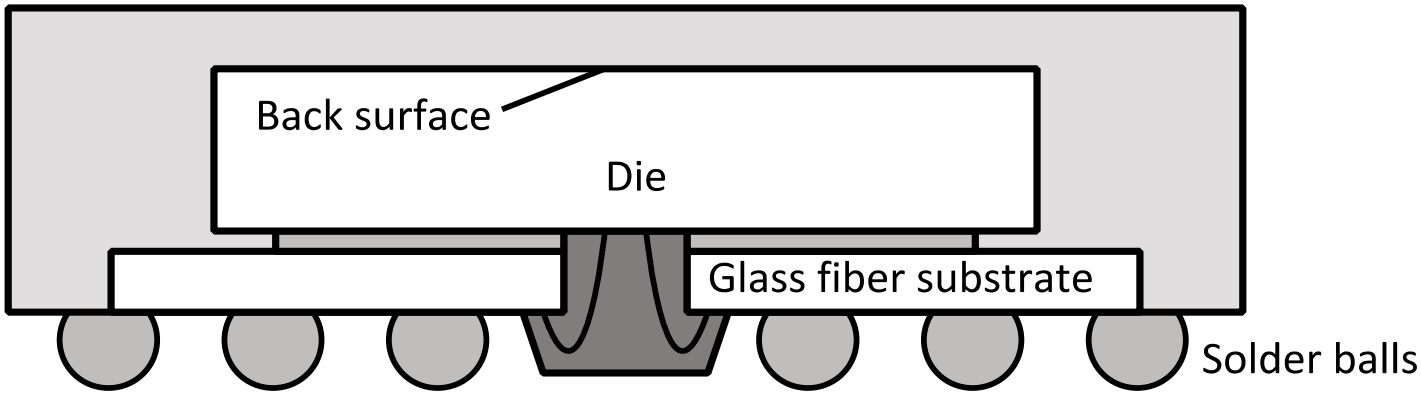
ITRS Product Function Size Trends



DDR3 SDRAM DUT Preparation

- DDR3-SDRAM in FBGA-Package
- die-thickness between 250 µm (Micron) and 350 µm (Elpida)
- penetration of ion beams is about 90 µm at LET = 30

→ **backside thinning down to 60 – 70 µm**



- NAND-Flash in TSOP-Package
- large die of the 32-Gbit parts results in incomplete plastic removal
- Micron NAND-Flash are sensitive to HNO3 etching

→ **only about 30% yield**

Some Challenges for High Speed Mass Memories

- Interfacing a large number of memory devices requires numerous signal drivers. Two basic approaches are:
  - Single memory controller + additional buffer devices
  - Multiple controllers

    Pros: No buffer devices, memory buses are kept local,

    Higher granularity of controller path can improve reliability and throughput

    Possible Cons: Higher costs and power consumption
- High speed memory signaling requires adequate controller technology
- Transport of high speed data streams requires adequate link technology
- Multiplexing of data streams requires additional buffer memory (in particular in case of NAND Flash)
- Power supply
  - Voltage levels can be rather low (e.g. 1.14V … 1.30V for LP-DDR2)
  - Load variation can be rather high (NAND Flash)

  → Dictates local power management

Calculation of Array Core Power

Memory Die Performance for selected parts and operating conditions:

			NAND Flash	DDR3 SDRAM	LP-DDR2 SDRAM
Manufacturer			Micron	Micron	Micron
Part			MT29F32G08ABCABH1-10	MT41J512M8RH-125:E	MT42L128M32D1LF-25 WT:A
Density	D	Gbit	32	4	4
Data Width, Clock Frequency			8 bit, 50 MHz	8 bit, 303 MHz	32 bit, 75 MHz
Write and Read Data Rates	R_W , R_R	Gbps	0.1 ; 0.56	2.4 ; 2.4	2.4 ; 2.4
Write, Read, Retention Power	P_W , P_R , P_{Ret}	mW	170 ; 122 ; 0	69 ; 78 ; 35	51 ; 49 ; 10.4
Write Endurance	N_{WE}		60000	∞	∞

Data Access Mode:	Flash: Random acces to rows, worst case program and read access times, DDR I/O
	SDRAM: Random access to 32 columns, 50% data I/O utilization, DLL-On (DDR3)
Data Retention Mode:	Flash: Standby or Power-off, SDRAM: Precharge Power Down
Aggregate Data Rate:	R = Record Data Rate + Replay Data Rate (both equal)
Duty Cycle:	dc = Activity Time / Total Time
Required Array Capacity:	C_{net}
Mission Time:	T_{Miss}
Minimum Die Count:	$N = \text{roundup}\{\max[C_{net}/D ; R/2 * (1/R_W + 1/R_R) ; R/2 * dc * T_{Miss}/(D * N_{WE})]\}$
Avg. Share of Dies Writing:	$sh_W = R/2 * dc / (R_W * N)$
Avg. Share of Dies Reading:	$sh_R = R/2 * dc / (R_R * N)$
Avg. Array Core Power:	$P = N * [sh_W * P_W + sh_R * P_R + (1 - sh_W - sh_R) * P_{Ret}]$