# ADCSS 2012 - Day 3 - Session Wrap-up

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# Introduction

- This summary provides a wrap-up of the sessions held on day 3 of the ADCSS:
  - Mission requirements and operational trends
  - Architectures and communication trends
  - Technology trends and challenges for future SSMM

- It is not intention to provide detailed analysis of all topics discussed, rather it attempts to capture the salient points of each paper and summarize the results of the discussion during the day

# Day 3 programme

| ADCSS-2012: 25 Oct 2012 Tennis Hall<br>Mass memories for payload applications and file based operations - J. Ilstad | | | |
|---|---|---|---|
| **Time** | **Presentation** | **Presenter** | **Company** |
| | ***Session 1: Mission requirements and operational trends*** | | |
| 09:00 | Welcome and Introduction | J.Ilstad | ESA/Estec |
| 09:10 | FTP for space - CFDP | C.Taylor | ESA/Estec |
| 09:35 | File Based Operations | M.Pecchioli | ESA |
| 09:55 | EUCLID Needs for space and ground segment | L.Stagnaro | ESA/Estec |
| 10:15 | OPS concept for EUCLID | F.Keck | ESA/Estec |
| 10:35 | JUICE mission – Mission overview and communcation aspects | C.Erd | ESA/Estec |
| 10:55 | Sentinel-2 Mass Memory and Formatting Unit and Future File Based Operations | G.Mandorlo | ESA/Estec |
| 11:15 | Session 1 discussions | | |
| 11:45 | *Coffee Break* | | |
| | ***Session 2: Architectures and communication aspects*** | | |
| 12:00 | Introduction | | ESA/Estec |
| 12:05 | A CFDP flight implementation | A.Bourdoux | Spacebel |
| 12:25 | Mass memory trend supporting file based operations | P.Lombardi | Syderal |
| 12:45 | Lunch | | |
| | ***Session 2: Continuation*** | | |
| 13:45 | Current and Future Mass Memory Products | M.Staehle, T.Pike | EADS Astrium |
| 14:10 | Advanced Mass Memory units and outlook on implementing CFDP | M.De Meo | Thales Alenia Space |
| 14:30 | Development of the CFDP IP core | N.Dankert | IDA Braunschweig |
| 14:50 | Session 2 discussions | | |
| 15:10 | Coffee Break | | |
| | ***Session 3 Technology Trends and challenges for future solid state mass memories*** | | |
| 15:30 | Introduction | | |
| 15:35 | Memory technology trends and qualification aspects | F.Gliem | IDA Braunschweig |
| 15:55 | ESA deep sub micron program - ST 65nm | L.Hili / D.Lehongre | ESA/ESTEC, ST Microelectronics |
| 16:15 | SpaceFiber IP core | S.Parkes | University of Dundee, Star Dundee |
| 16:35 | Improved Memory Module for COTS NAND FLASH devices | G.Tuccio | Sitael |
| 16:55 | Use of CFDP in NASA/GSFC's fligth SW architecture | J. Wilmot | NASA via Webex |
| 17:15 | Wrap-up and conclusions | | |
| 17:30 | End | | |

# Session 1 Wrap-up

- CFDP is an international standard with heritage and currently under review – inputs welcome
- The file based operations study led by ESOC has completed and concluded that file based operations will bring benefits and is the way forward; CDFP has been selected as the baseline for file transfer and will be made available in the ground segment as a standard service
- The use of K-Band infers that transmission will be subject to increased data loss such that retransmission may be required
- The study of Euclid requirements has led to the baselining of file based ops and CFDP, the actual implementation will be left to industry
- ESOC is investigating the basic concepts of file based operations in preparation for Euclid
- Earth ops may utilise optical communication in the future and such links may also incur data loss  requiring transmission
- Any move towards file based operations should involve all parties so that an end-to-end solution is developed
- Possibly too soon to determine if CFDP would bring big benefits to Juice but long delays on uplink may be assisted by file based checksum

# Session 2 – Wrap-up

1. Spacebel has developed and tested in a representative end-to-end scenario a software modular CFDP entity.
    a. The Test Infrastructure is based on the Proba2 OBSW and SVF.
    b. Class 1 (best effort) and Class 2 (reliable) transfers have been implemented.
    c. A File store operations and structure have been developed.
    d. Initiating file transfer are possible through PUS and through CFDP.

2. Syderal has presented its current development and R&D in Solid State Mass Memory.
    a. GAIA PDHU and EartCare MMFU.
    b. The Next Generation Solid State Mass Memory (NG-SSMM) will implement a CDFP class transfer.
    c. Hardware implementation of the downlink chain processing is considered necessary to cope with High Data Rate.

# Session 2 – Wrap-up

3. Astrium has presented its current development and R&D in Solid State Mass Memory.
    a. Astrium latest SSMM products with Flash NAND Flash technology provide savings of more than 50% in mass and power consumption over comparable SDR-SDRAM products.
    b. Flash SSMM units are fully qualified at component & unit level and successfully operating in space (Spot-6) since Sep 2012. S-2 will use a Flash SSMM
    c. The implementation of the CCSDS File Delivery Protocol is supported by the R&D Activity (NGMMA). A useful configuration in the frame of NGMMA needs HW support to cope with the high speed demands.

# Session 2 – Wrap-up

4. TAS-I has presented its current development and R&D in Solid State Mass Memory.
    a. A detailed description of the functionalities implemented in the Multi-user SSMM developed for Bepi Colombo and Solar Orbiter has been presented.
    b. The SSMM developed by TAS are implementing a file based storage and transfer engine based on adapted PUS13 Large Data Transfer and PUS15 On-board Storage and Retrieval services.
    c. HW technology trends (TAS) and SW architecture trends and challenges (INTECS) for Future SSMM have been presented

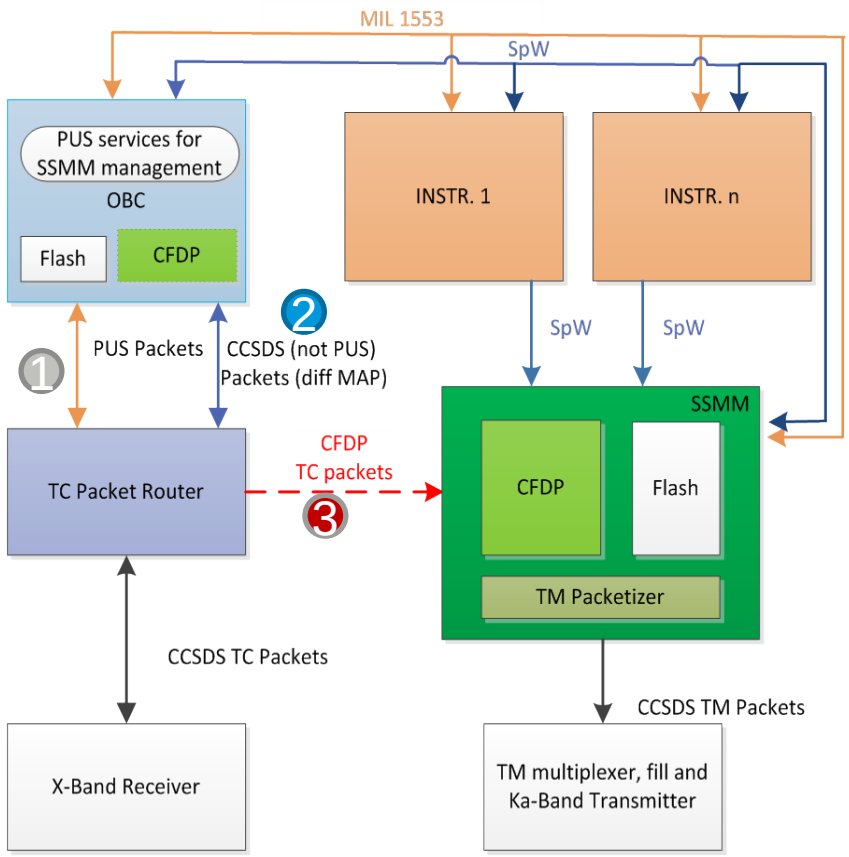
# Session 2 – Wrap-up

5. C3E of the Technische Universitat of Braunschweig has presented the on-going development of the CCSDS File Delivery Protocol IP Core
    a. Class 1 and Class 2 transfers
    b. Configurable (Size of Local and Remote Entity IDs, Size of Transaction IDs, Number of Remote Entities, Number of Outstanding Transactions,..,)
    c. The filestore is decoupled from CFDP IP using a generic interface
    d. Based on a HW & SW architecture

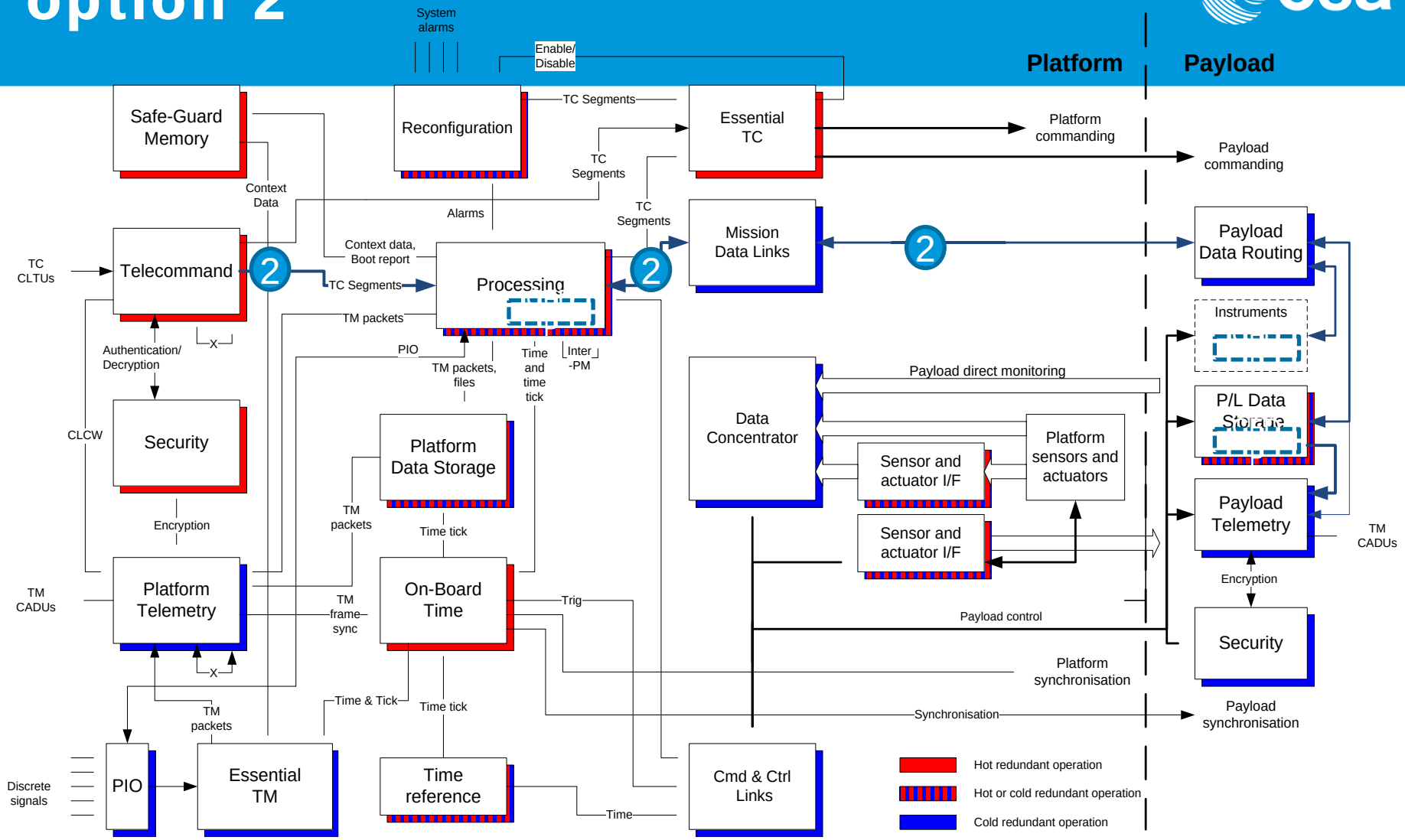
# Session 2 – Wrap-up

At the end of session 2 the various possible options for a CFPD implementation(s) on board have been presented and some of them mapped on the Savoir Functional Architecture:

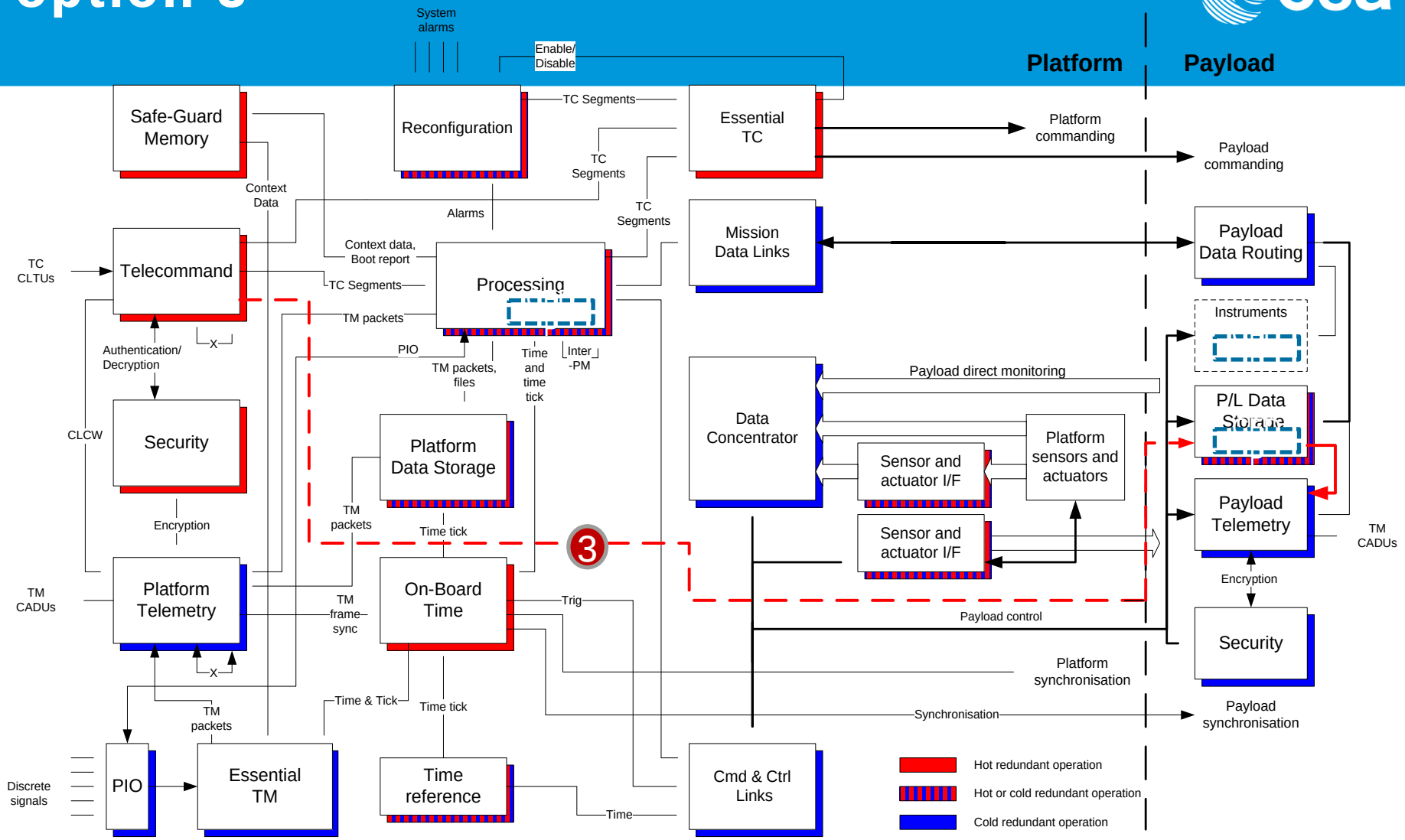
- CFDP entity is located in the SSMM (for P/L data) but could also be located in the OBC MM (ASW image,…)
- Direct link from the SSMM to the Transponder (X, Ka band)
- CFDP Metadata (CCSDS packet) for CFDP transactions to/from SSMM are routed directly to SSMM (3) or passed via the OBC (2), see next slides
- Implementation of large data transfer (TAS SSMM for BepiColombo) are using PUS packet (1)



# CFDP Metadata sent through the OBC option 2



# CFDP Metadata sent directly to the SSMM option 3



# Session 3 – Wrap-up

1. Memory storage technology is in continuous development. Testing of the devices is increasingly challenging, particularly multi-die devices.
    a. Thinning of die for HI testing is hampered by low yield
    b. Testing of LPDDR memory should be given priority.
    c. Do we need to change our strategy for device testing? i.e. putting in place means to quickly carry out SEE tests for devices.

2. ST microelectronics 65nm technology appears crucial to be able to exploit next generation memory devices both in terms of voltage level SSTL15 and SSTL18.
    a. Next generation high speed serial links operating at up to 6Gbps is facilitated with 65nm DSM technology
    b. Test vehicles of full commercial library has been characterised.
3. SpaceFiber standard and VHDL IP core has be presented, and beta testing among alpha customers is on-going.
    a. SpaceFiber provides built in QoS and FDIR.
    b. Alpha customers is testing
    c. SpFi link analyser for end-to-end communication verification is in development.
    d. SpFi is applied as internal communication backbone in Next Generation Mass Memory (AO/1-5975/08/NL/LvH)

# Session 3 – Wrap-up

4. Mitigation towards SEE in FLASH technology is challenging and requires adequate test platforms to allow for investigation of complex single event functional interrupt mechanisms.
    a. The Improved Memory Module IP core to become part of the ESA IP core library to facilitate test of fault mitigation techniques.
    b. Worst Case Uncorrectable BER Calculation shall be calculated from tested raw NAND bit error rate (BER),

$$BER_{worst\ case} = BER_{radiation} + BER_{cycling} + BER_{disturb}$$

    c. Error Correction Codes (ECC) are always required with NAND Flash and shall be dimensioned in *test as you fly, fly as you test* way.
5. CFDP experiences in LRO have been positive and have given mission operation center and science operations centers a greater degree for flexibility.
    a. High data rates needs dedicated hardware processing functions.
    b. Commercial file systems such as the ones provided in e.g. RTEMS or VxWorks have high overhead. Simpler versions required.

# Day 3 - Summary

- The three sessions were all related to future requirements and trends in relation to mission requirements, operations and technology for what concerns mass memory, data transfer requirements and the use of files
- Representatives from many interested areas (projects, operations avionics and industrial suppliers) all presented their specific views and this provided for a lively forum
- From the project viewpoint, the main message was that the use of Ka-band in news mission will require the retransmission of missing data due to atmospheric induced outages, other inputs included:
    - Continuously increasing data rates and the use of optical links
    - The need for fast data turn around
    - The need to involve all parties, including ESRIN, to optimise the end-to-end system
- Some concern was expressed on the need for files versus existing packets with an overall consensus that both have their place to play in future systems
- All in all the use of files and a standard file protocol was promoted as a way forward especially for Euclid where CFDP is now baseline for the ITT
- The presentation from NASA on LRO and the successful use of files/CFDP added to the confidence that file based operations is a solid way forward

# Day 3 - Summary

- From an ops viewpoint a strong belief in the use of files was expressed on the premise that it will simplify and stream-line operations
- The use of CFDP on the downlink was fully supported but added to this was the use of CFDP on the uplink
- Effort still needs to be expended on defining the way in which the content of files are used onboard and this will eventually require updates to PUS
- From an implementation aspect there are many on-going developments which will support the use of Files and file transfer and no particular concern was expressed on the difficulties to implement files or CFDP
- There are options on the way in which CFDP is implemented in the flight avionics and how access is provided to the Mass memory and these need to be traded, some updates to Savoir documentation to reflect this will be required (see figures)

# Day 3 Summary

On-going ESA funded activities applicable to mass memories, Page 1/2

| Activity Title | Scope | End Date | ESA Program | Status |
|---|---|---|---|---|
| Next Generation Solid State Mass Memory (EADS Astrium,IDA,Star Dundee) | - 6 Gbits record, 2 Gbits replay, 2Tbit capacity.<br>- DDR-3 DRAM memory for mass storage<br>- SpFi based architecture<br>- CFDP Class 2 implementation | Q4 2013 | TRP | Detailed Design phase |
| Very High Speed Link Demonstrator – SpaceFiber (University of Dundee) | - Demonstrator<br>- IP core development<br>- Inputs to ECSS standard | 2013 | TRP | Beta Codec (VHDL) available. Alpha users are testing |
| Technology Assessment of DRAM and Advanced Memory Products (Astrium SAS Satellites, Thales Security Solutions & Services, IDA, Astrium ST, EADS Innovation Works) | - Assess commercial state-of-the-art DRAM memories and their robustness for space applications.<br>- Conduct radiation assessment and technology evaluation of state of the art advanced memory technologies for space applications like FeRAM, MRAM, PCRAM. | 2014 | TRP | Early stage |
| Radiation Hard Memory; Radiation Testing Of Candidate Memory Devices For Laplace Mission (EADS Astrium, IDA) | - Identify suitable candidate memory for Laplace<br>- Evaluation Program of state of the art COTS memory<br>- Assessment of emerging memory technologies (e.g. MRAM, FeRAM, PCRAM) | 2013 | TRP | |
| CFDP IP core development ( TU Braunschweig) | - VHDL IP core development<br>- Technology mapping to e.g. DARE library | 2014 | TRP | Preliminary design phase |

# Day 3 Summary

## On-going ESA funded activities applicable to mass memories, Page 2/2

| Activity Title | Scope | End Date | ESA Program | Status |
|---|---|---|---|---|
| Next Generation – Mass Memory Architecture (Syderal SA) | * 3Tbit Flash Based memory modules<br>* CFDP - class 1<br>* 6Gbps record, 2 Gbps record. | 2014 | STRIN | Detailed Design Phase |