PMD, rationalisation and interface standardisation

Agenda

TEC-EPM
ESA-ESTEC

Workshop at ESTEC, 3 and 4 October 2012, Escape Tennis Hall

PMD rationalisation and interface standardisation

Workshop objectives

a. Identification of “items” of rationalisation within PMD domain, fulfilling a minimum set of qualifying features*

b. Agreement on a logical path towards standardisation, where possible and convenient, of (power) electrical interfaces, functions and units for space applications in Europe, to be achieved with the cooperation of all main actors**

* wide use, flexibility, recurrent utilisation, non-exclusive exploitation

** unit/equipment manufacturers, Primes, ESA and possibly other European Agencies

Applicability: institutional markets, but could be used for commercial space market too.

Agenda, day 1, Oct 3rd 2012, PMD rationalisation opportunities

1. 13:30-13:40 **Welcome** – H. Barde

2. 13:40-14:00 **Introduction -** F. Tonicello

3. 14:00-16:45 **Presentations & discussion (20'+10') –** moderators: M.M. Alfonso / F. Tonicello

   a. 14:00-14:30 Thales Alenia Space & CNES – ***Modular PCDU***
   b. 14:30-15:00 STM – ***Integrated Current Limiter as a key example of rationalisation***
   c. 15:00-15:30 Thales Alenia Space ETCA – ***Digital Power Control as a potential aid to achieve better rationalisation of interfaces?***

   d. 15:30-15:45 Coffee break

   e. 15:45-16:15 3D-Plus - ***Building blocks for secondary power distribution and conversion units***
   f. 16:15-16:45 ESA on Eads Astrium and other inputs – ***Key areas and opportunities for PMD rationalisation***

4. 16:45-17:45 **Roundtable on rationalisation opportunities –** moderator: H. Barde; presenter: F. Tonicello
   a. Key factors
   b. Opportunities
   c. Challenges
   d. Mapping on landscape architectures

5. 17:45-18:00 **Wrap-up** – F. Tonicello

Agenda, day 2, Oct 4th 2012, PMD interface standardisation opportunities

1. 9:00-9:15 **Introduction -** F. Tonicello

2. 9:15-12:00 **Presentations and discussions (20' + 10')** – moderator: F. Tonicello

   a. 9:15- 9:45 CNES – ***ISIS initiative***
   b. 9:45-10:15 TERMA ***– Key areas of LCL interface standardisation***
   c. 10:15-10:45 ASP – ***Proposed standardisation of Solar Array Regulator interfaces***

   d. 10:45-11:00 Coffee break

   e. 11:00-11:30 OHB - ***Opportunities on standardisation from system level perspective***
   f. 11:30-12:00 SG - ***SELEX Galileo approach for (power) electrical interfaces standardisation***

3. 12:00-13:00 **Roundtable on interface standardisation opportunities** (part 1) – see next chart

4. 13:00-13:45 Lunch

5. 13:45-15:30 **Roundtable on interface standardisation opportunities** (part 2) – see next chart

6. 15:30-15:40 **Wrap-up -** F. Tonicello

7. 15:40-16:00 **Summary of workshop and way forward** – H. Barde

Agenda, day 2, roundtable on PMD interface standardisation opportunities

1. 12:00-13:00 **Roundtable on interface standardisation opportunities** (part 1) – details – moderator: H. Barde; presenters: various
   a. Objectives
   b. Constraints
   c. Specific issues & examples
      - Power system distribution, we are almost ready for I/F standardisation
      - S/C with unregulated bus, is an additional regulated bus interface convenient for platform items?
2. 13:45-15:30 **Roundtable on interface standardisation opportunities** (part 2) – details – moderator: H. Barde; presenters: various
   a. Specific issues & examples (continued)
      - Battery switch: single or double barrier? Relay, arm plug or other?
      - Contingency cases: standardisation of DNEL interface?
      - Diodes in series to all SA sections for centralised Solar Array Regulators with MPPT , or reliable S3R Shunt Stage
      - Umbilical battery conditioning & power bus supply series diodes
      - Interfaces between Battery and PCDU Battery Management (Power & Sensing)
   b. What standardisation of (power) interfaces could bring
      - Specific example: CII interface
   c. Which are the possible impacts and the risks involved
   d. Possible workplan and frame
   e. Is there consensus to start working on interface standardisation?

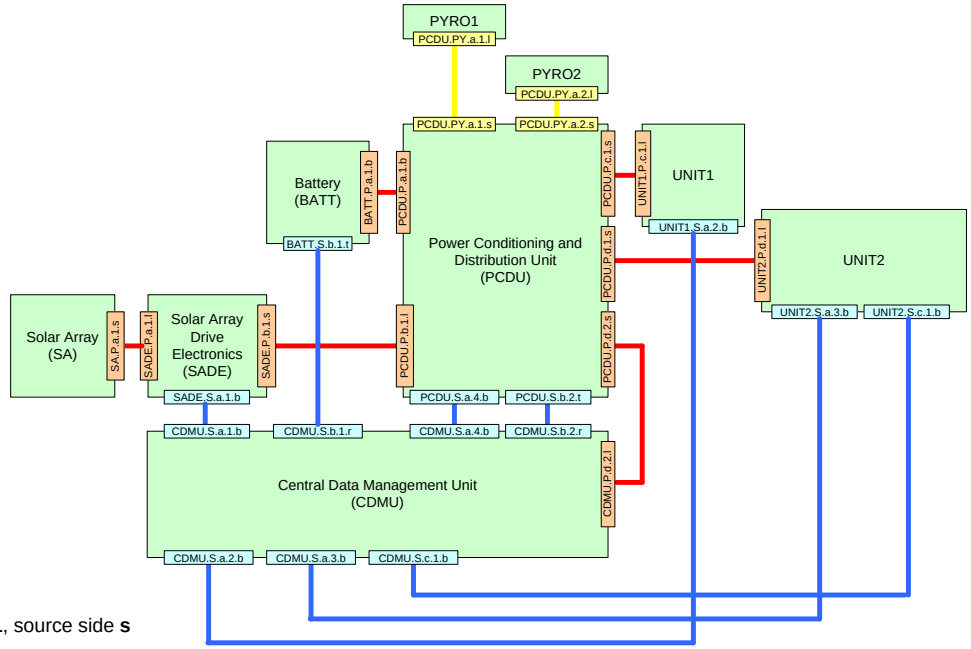
PMD I/F standardisation – Possible workplan and frame

1. Proposed work plan: small steps, incremental approach as described in the TN you received in the invitation to this workshop

   a. **Define** reference architecture
   b. **Collect**…
   c. **Compare**…
   d. **Assess**…
   e. **Minimise**… I/F datasheets

PMD I/F standardisation – Possible workplan and frame

a. Define reference architecture:
establish the "borderlines" of the interfaces to be evaluated (it is sensible to take the most generic cases, widely applicable to all satellites)



Element1 (E1) — Element1 (abbreviated E1) – it can be a unit, function or subfunction

Power line

Signal line

Pyro line

APS.P.a.1.s — **APS** element, Interface **P** (power), interface type **a**, interface instance **1**, source side **s**

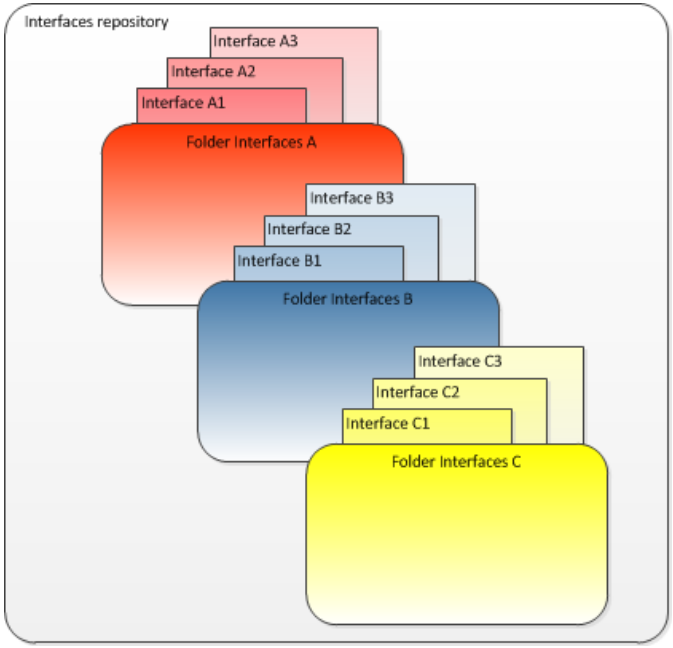
TMTC.S.b.2.r — **TMTC** element, Interface S (signal), interface type **b**, interface instance **2**, receiver side **r**

PCDU.PY.g.3.l — **PCDU** element, Interface **PY** (pyro), interface type **g**, interface instance **3**, load side **l**

PMD I/F standardisation – Possible workplan and frame

b. Collect:

after defining a common datasheet format, collect the most updated and complete interfaces datasheets available in your company (mostly a work to be done by procurement agents – Primes, Platform or Payload responsible).

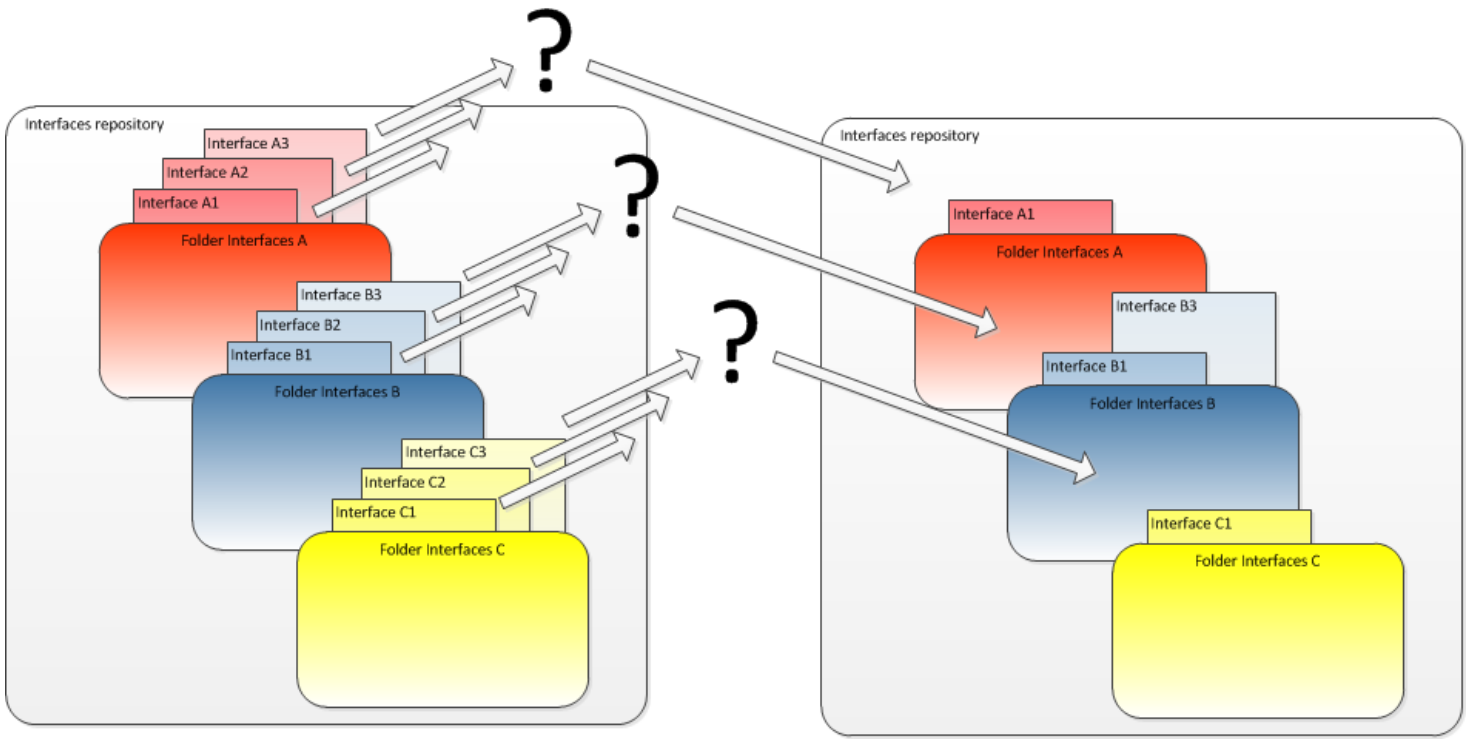


The vehicle might be a common repository that can *immediately* be used as a reference document for new projects

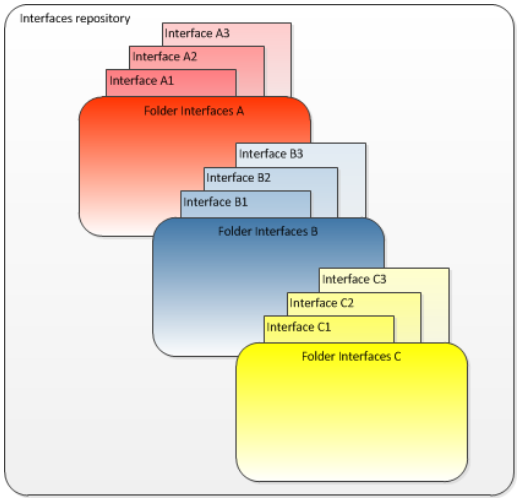
PMD I/F standardisation – Possible workplan and frame

c. **Assess** differences

d. **Minimise** as far as practical and possible interfaces of the same type



PMD I/F standardisation – Possible workplan and frame



DEFINE

COLLECT

COMPARE

ASSESS

MINIMISE

Process to be elaborated and proposed as a new ECSS work item

PMD I/F standardisation – Workshop statistics

Participants	**61**	
External	36	
Internal	25	

Questionnaire response (external participants only)

	Yes...	Partially...	Not...	... in line with my expectations	
Did the workshop meet your expectations?	78%	22%	0%		
Are you satisfied with the workshop?	Very satisfied	Satisfied	Neutral	Not satisfied	Completely dissatisfied
	7.4%	85.2%	7.4%	0%	0%
Would you take part to European Work Group for (power) interfaces standardisation?	Yes	No			
	93%	7%			

Especially if the answer is negative, which are the relevant reasons?

The negative answers (two) come respectively from a university representative and from a Si foundry representative.
It is clear that those two entities are not interested in the standardisation of (power) interfaces.

Do you think that your company would adhere to a European Initiative for (power) interfaces standardisation?	Yes	No	There is one missing reply, neither option was selected.
	89%	7%	