Improved Memory Module for COTS NAND FLASH devices

ADCSS2012

ESTEC, October 25th, 2012

Project Overview

- **Context**
  - “Digital Latch Up and functional protection for COTS memories in space “ ITT of European Space Agency’s Directorate of Technical and Quality Management (ref. TEC-EDD-20009,42-T201-002ED, 25/11/2009)
  - ESA Contract N. 4000102926/11/NL/AF based project
- **Aim**
  - Development of an Improved Memory Module IP Core to mitigate the radiation effects caused by heavy ions, neutrons and protons impact on a COTS based mass memory modules, making use of digital techniques
- **Outputs**
  - Configurable Improved Memory Module IP Core (IMMIPC)
  - IMM Breadboard (IMMB) to test and verify the core functionality

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Improved Memory Module Interface

- **IMM is a black-box module embodying a reliable low-power mass-memory module**

- **Write-Read operations are controlled with a DMA like interface accessed via SpW-RMAP**
  - Fixed data size 2 (4) Kbyte Page access
  - Write operation:
    - **`Wait for IMM not busy`**
    - **`Write Page at logical address`**
  - Read Operation:
    - **`Request page read-DMA on R-Control register`**
    - **`Wait for end of DMA`**
    - **`Read Page Data from output buffer`**

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What is in the Box

- **Nand Flash Address Translation Layer.**
- **Error Correction Code and control for Nand Flash errors and SEU/SEFI effect .**
- **Communication stack up to the Transport Layer: end-to-end reliable connection with (support to) flow control**
- **Test Utilities:**
  - Fault Injector on the Nand Flash Interface
  - HK circuit for current/temperature monitoring

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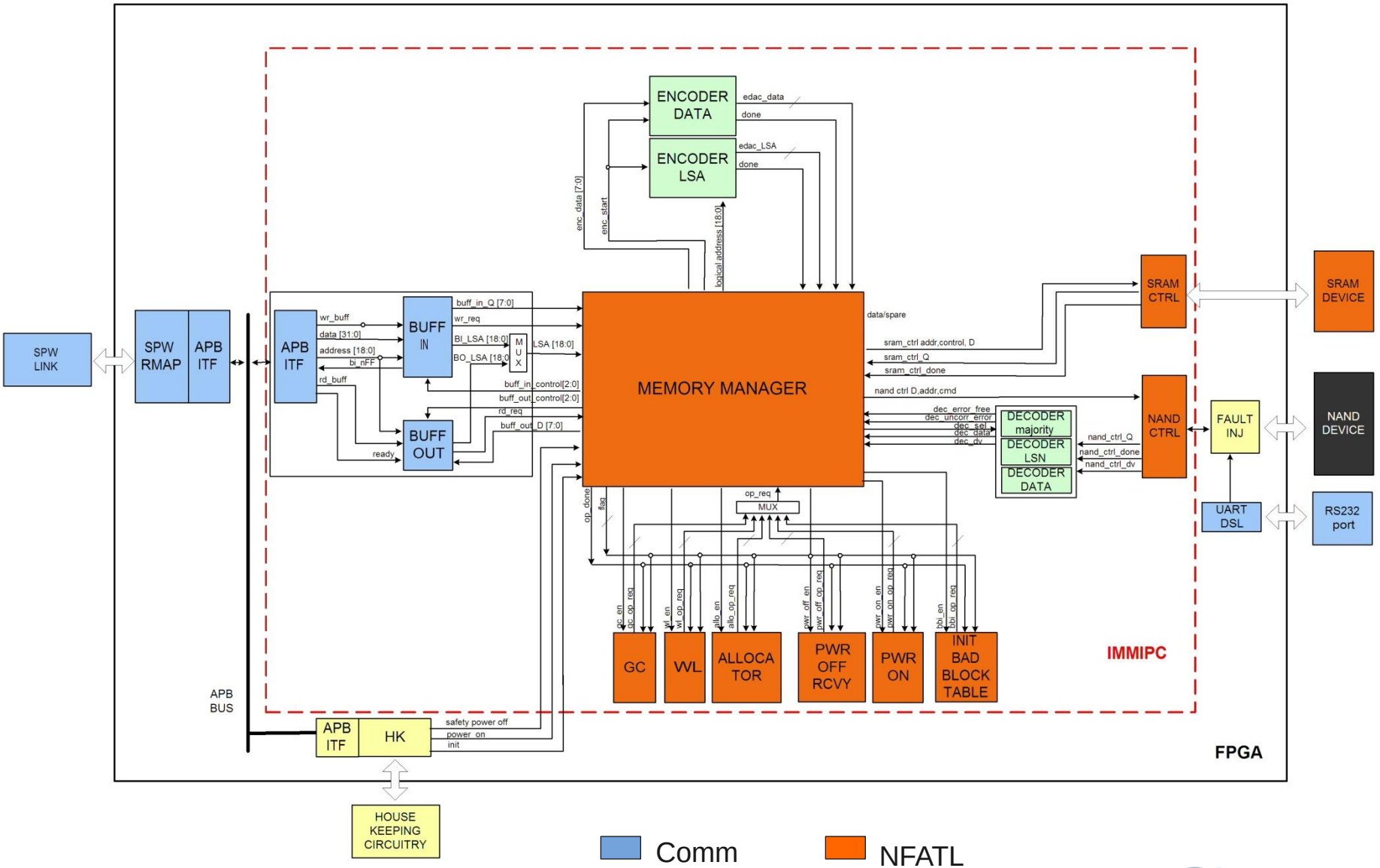
IMM Block Diagram



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Nand Flash Address Translation (1)

- **NAND FLASH MEMORIES**
  - Flash Memory array is composed of blocks, and each block is made up of pages (1 block == 128 page == 512 Kbyte + Spare)
  - Minimum erasable unit is a block
  - Erase operation is time consuming (700 us)
  - Some blocks are bad at shipping time
  - Each block can be written only a limited number of times (100,000)
  - Program page is possible only on erased paged, i.e. write–once
  - Within a block, pages must be programmed in sequential order
  - Each page is provided with additional storage called spare area to store metadata (ECC and additional information)

- **NAND FLASH ADDRESS TRANSLATION LAYER**

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Nand Flash Address Translation (2)

- **NAND FLASH ADDRESS TRANSLATION LAYER Building Blocks:**
  - Allocator
  - Bad blocks Manager
  - Wear leveler
  - Garbage Collector
  - Power off
  - Power on

- **Resource Budget on ProASIC3E A3PE3000 FPGA :**
  - Core cells : 10%
  - Block rams: 15%

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Nand Flash Address Translation (3)

- **ALLOCATOR**
  - It manages 2(4)K byte page write and read request from Spw link
  - Logical to physical address translation is implemented to manage overwrite requests of the same physical page
  - Logical address is written into spare area of NAND physical page because random page programming within a block is prohibited (pages have to be written sequentially !)
  - ECC is written into spare area of NAND page to protect both data and metadata
  - A Hybrid-mapping Translation Layer based on LOG buffer is used to defer the time-consuming block erase operations.
  - Block Mapping Table (BMT) for data blocks and Sector Mapping Table (SMT) for log blocks are stored in SRAM memory.
  - Log blocks are used to handle page overwrites.

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Nand Flash Address Translation (4)

- **BAD BLOCKS MANAGEMENT**
  - NAND Flash are shipped with some bad blocks marked as invalid by vendor
  - A bad block table all invalid blocks addresses
  - Bad block table is updated with blocks that worn out during device life time
- **WEAR LEVELER**
  - Evenly distribute the number of erasures of each block to improve device endurance
  - Static wear leveling method is implemented
  - SRAM tables are used to keep number of erasures of each block and to select victim block

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Nand Flash Address Translation (5)

- **GARBAGE COLLECTOR**
  - NAND FLASH device accumulates obsolete pages and the number of free available pages decrease: GC is used to recycle the blocks occupied by the obsolete pages and reclaims free space
  - On-demand: GC reclaims free blocks when the number of free blocks is under a certain threshold
  - Background: GC cleans obsolete blocks by performing block erase operations and puts them into free blocks pool
  - SRAM tables are used to read/mark the status of each block(free/data/log/dirty/bad/mem)

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Nand Flash Address Translation (6)

- **POWER OFF**
  - A block of NAND FLASH is used to store the copy of the SRAM tables into a non-volatile memory in order to save address mapping tables and other vital info
  - Standard power off: SRAM tables are saved to NAND FLASH when a power off request occurs
  - Recovery Power off: copy of the SRAM table is done periodically to work as back up copy in case of sudden power off

- **POWER ON**
  - First power on: SRAM tables are initialized and later saved into a NAND FLASH block
  - Power on: SRAM tables are loaded retrieving the last copy saved in NAND FLASH

Error Correction Code (1)

All data and metadata in NAND Flash and in off-chip \ on-chip RAMs are protected with a specific ECC

The IMMIPC is equipped with 4 distinct codec engines

- BCH code protecting 2 (4)KB Nand FLASH data page;
- A SEC-DED code protecting the Logical Sector Address;
- A repetition code protecting the binary information of the RAM-table copy in a NAND block;
- SEC-DED codes to protect data stored in external SRAM and internal Block-RAMs.

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Error Correction Code (2)

BCH (Bose Chaudhuri Hocquenghem) codec

- length of the code : 2048+29 bytes
- length of info. word : 2048 bytes
- number of parity bits : 225 bits (stored in the spare sector)
- Random error-correcting capability : 15 bits
- Coding rate 2048/(2048+29) : 0.986
- Fast decoding process\low latency: byte-oriented solution, 15 Galois-Multipliers working in parallel → code size + 71 cycles latency between the first byte provided by the Flash memory and the first decoded byte.
- BCH codec area occupation on Actel ProAsic3 A3PE3000 @ 25MHz : 30% logic resources \ 6% Block-RAMs

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Error Correction Code (3)

LSA codec

- SEC-DED code protecting the LSA (Logical Sector Address)
- length of codeword : 21 bits (LSA) + 7 bits (parity bits)
- Stored into spare sector of the NAND Flash

Majority decoder

- Repetition decoding is done using majority logic detection
- The code chosen is a repetition of ‘1’ or ‘0’ 7 times, in a single byte into spare area. All zero word identifies a RAM Table - copy block
- Random error-correcting capability: 3.

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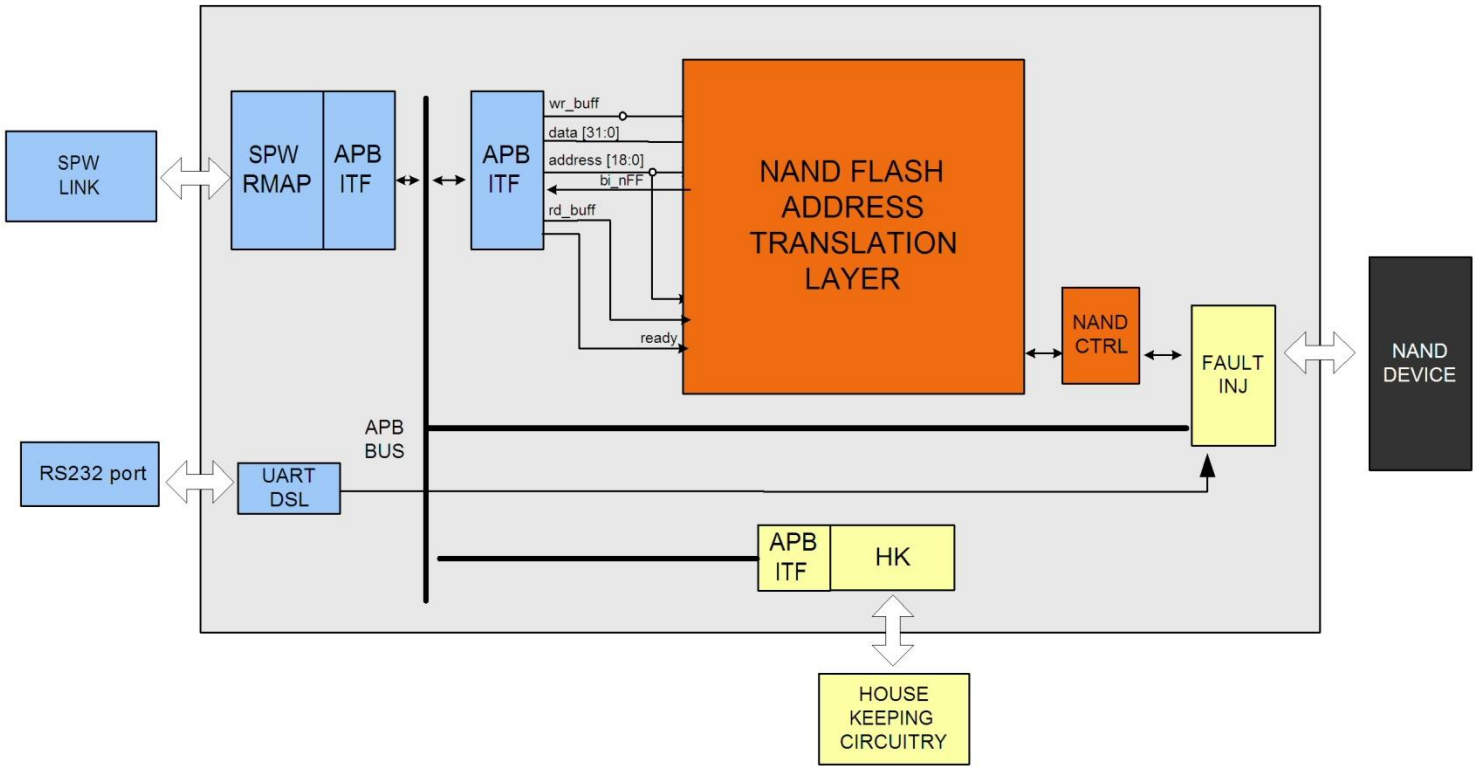
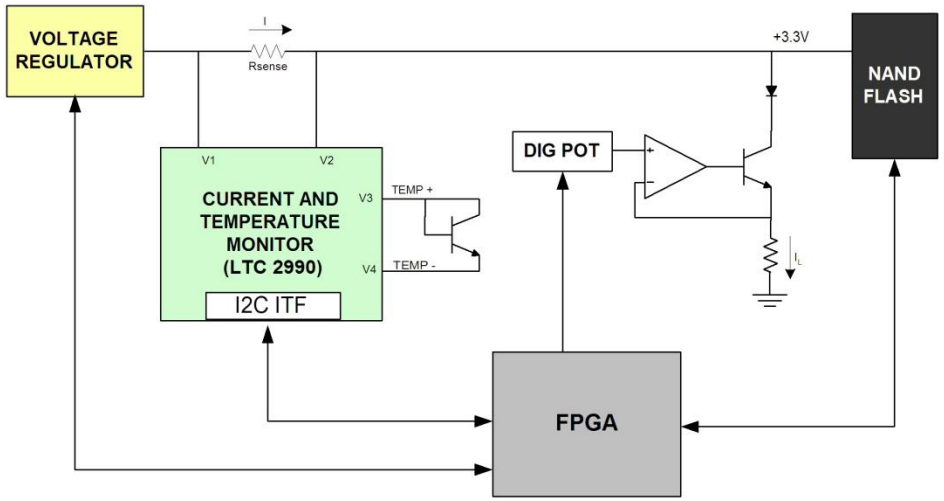
Communication Stack

- SpW-RMAP as host interface
- DSU like protocol on serial RS232 for test (Fault Injection)
- APB bus for Control and Test.



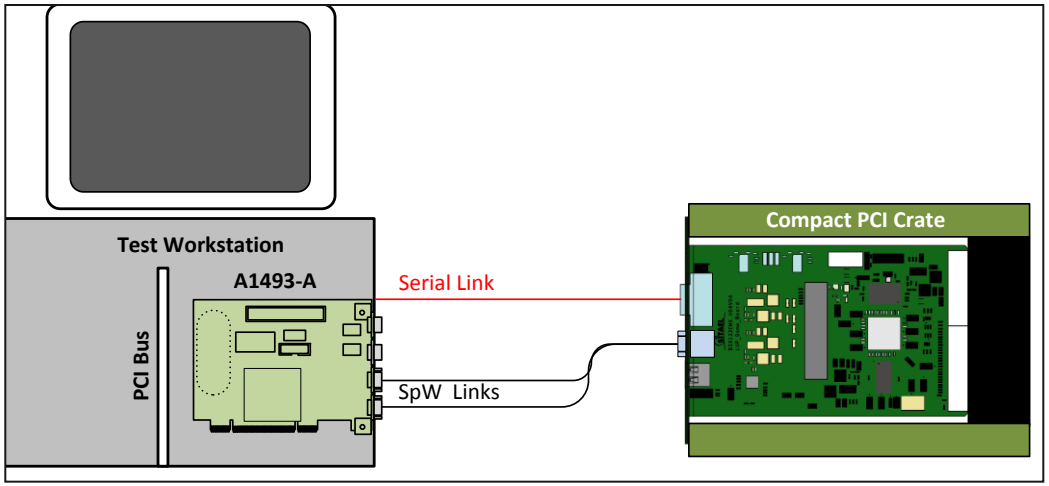
Test Utilities

- **Fault Injector on the Nand Flash interface**
  - Programmable for errors number, error rate or pseudo-random function
  - Controllable via RS232 or APB
- **HK circuit**
  - Nand FLASH Current and Board Temperature monitoring with the LTC 2990 IC (I2C interface, 14 bit ADC)
  - Programmable threshold for auto power-off request
  - Latch-up emulator based on a voltage controlled current sink

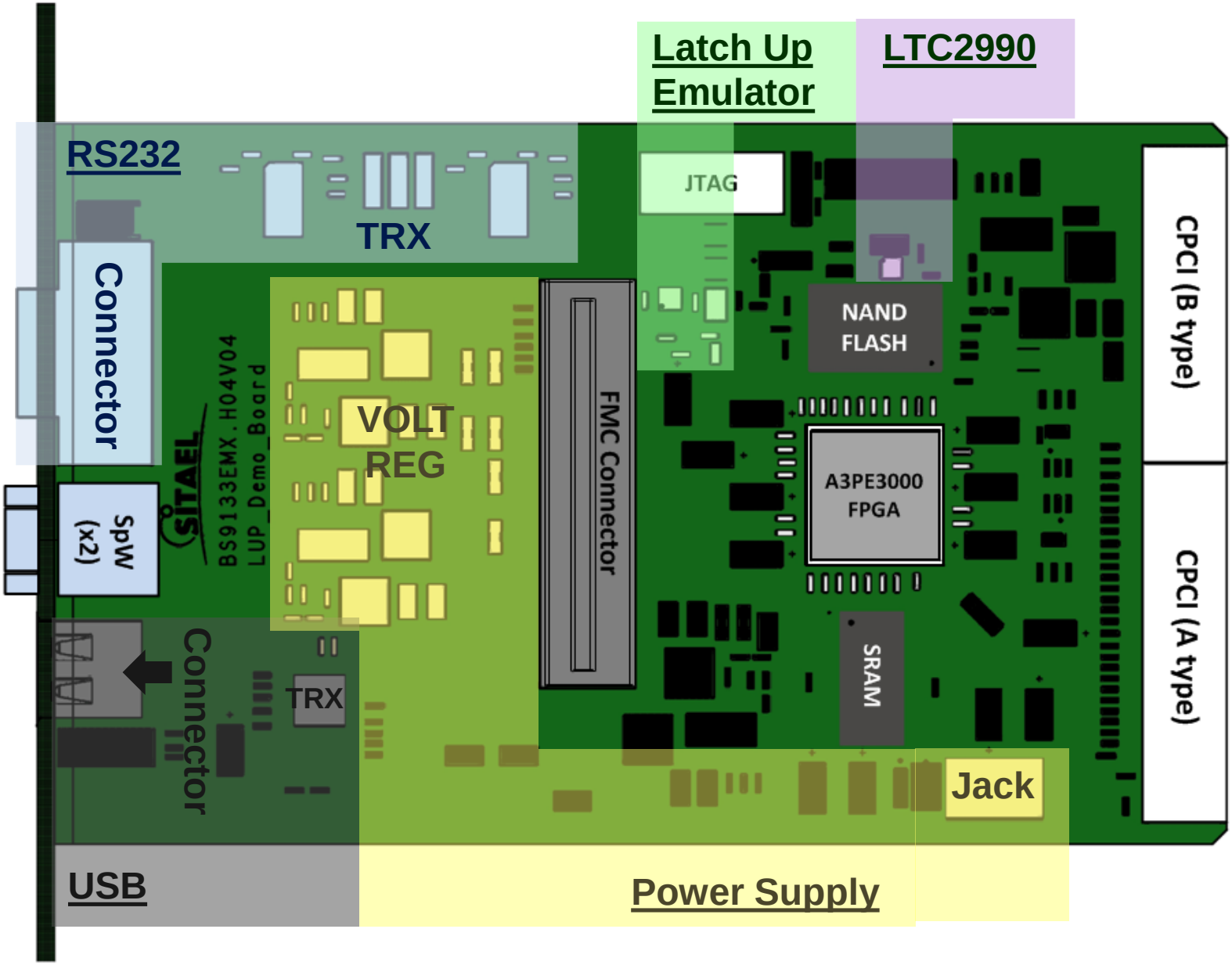


Demo Board

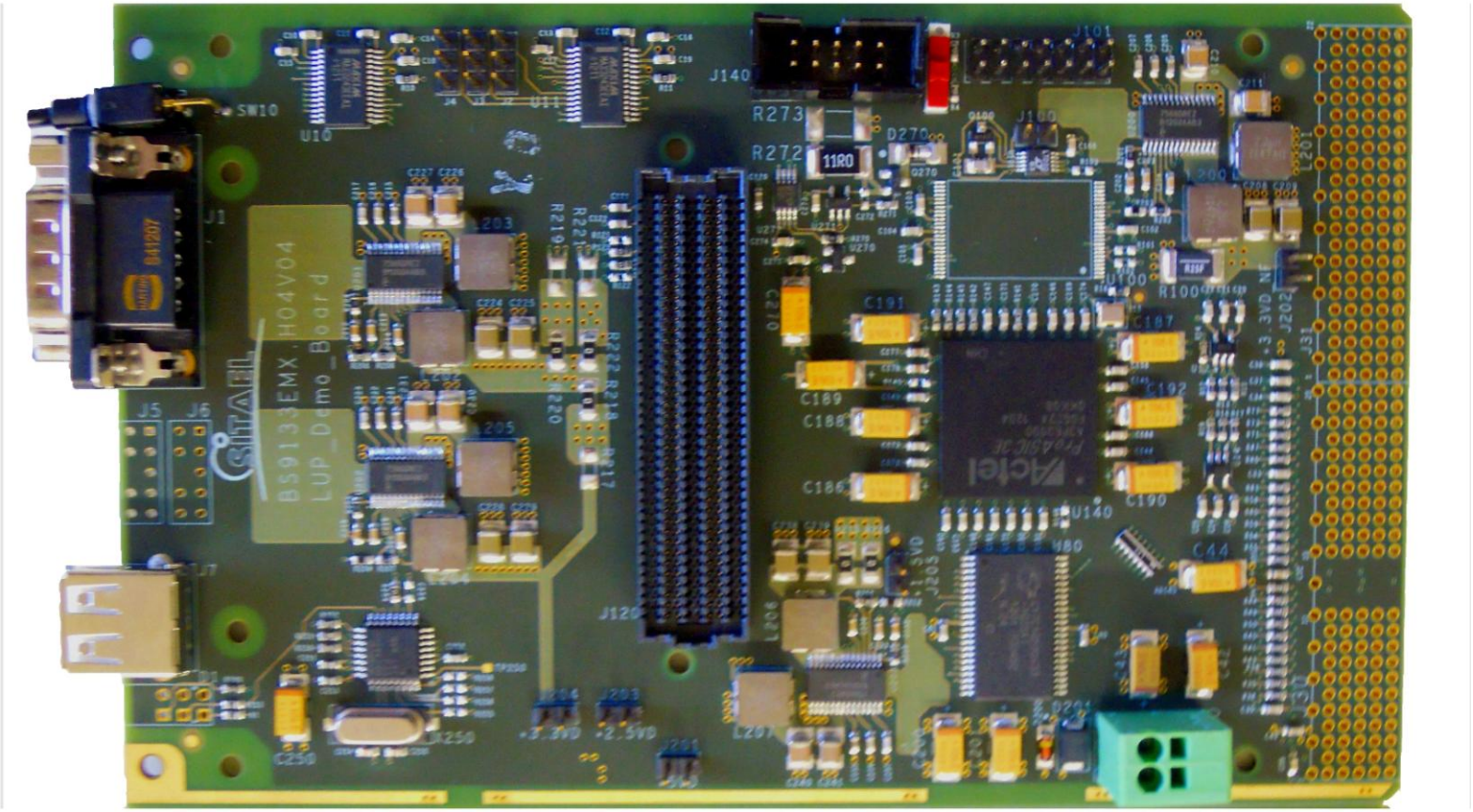
- CompactPCI 3U-8HP (RASTA compliant)
- Actel ProASIC3E A3PE3000
- Nand FLASH Micron MT29F64G08AJABA (UUT) 64Gbit with dedicated power Supply
- SRAM Buffer 1Mx8
- HK circuit based on I2C current and temperature monitor LTC2990 + Latch-Up emulator
- SpaceWire 2x ports + Serial RS232



Demo Board Layout



Demo Board Photo



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Conclusions and Next Steps

- **Project Status**
  - IMM architectural and detailed design complete
  - Manufacturing completed
- **Activities in Progress**
  - Test on Demo Board
  - IP Core Consolidation
  - RASTA Environment Integration
- **Next Steps**
  - Demo Application test case
  - NFATL algorithms evaluation/refinement

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Thank you for your attention!

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Spare 0

NAND FLASH timings:

- TSOP package asynchronous interface 50Mhz with DutyCycle1/2 == access time = 40 ns
- BGA package synchronous interface 100Mhz DDR == access time 5 ns
- 1 page = 2 Kbyte
- 1 page program = internal reg write + programming time = 85000 ns (@50Mhz)+ 200us =~ 285 us
- 1 page read = latency + internal reg read = 25 us + 85000 ns (@50Mhz) =~ 110 us
- 1 block = 128 page erase = 700 us

NFATL timings:

- 1 page = 2 Kbyte; 4096 blocks; 4 log block
- NFATL write: sequential page write min=326 us ; max 4 ms =~ (25+5) us * 128
- NFATL write: overwrite =~ 2 x sequential write
- NFATL write: overwrite + new log block =~ 23 ms
- NFATL read: min 230 us; max 5 ms =~ (25+5) us * 128 + log block scan

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Spare 1

- **NAFTL FSM complexity:**
  - System scheduler == 10 states
  - DMA engine == 32 state
  - Allocator == 467 states
  - Bad blocks Manager == 30 states
  - Power off == 66 states
  - Power on == 42 states

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BCH Vs DSCC (Difference Set Cyclic Code)

- Goal: strong random error protection with smallest complexity;
- 2 principals block-codes have been considered: BCH codes and DSCC codes (no RS codes, since burst errors aren't the main occurrence in NAND Flash soft errors events);
- BCH code has better performance for 2\4KB of block-length: fewer redundancy symbols in order to correct the same amount of random bit-errors;
- BCH decoding architecture is slightly smaller and faster (considering multiple Galois multipliers);
- BCH code guarantee the best fitting-factor for the granularity of the Flash memory: 2\4KB in data sector and ECC parity string into spare amounts.

Spare 2

- **NAFTL FSM complexity:**
  - System scheduler == 10 states
  - DMA engine == 32 state
  - Allocator == 467 states
  - Bad blocks Manager == 30 states
  - Power off == 66 states
  - Power on == 42 states

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