a Cohort plc company

– ADCSS 2012 –
Miniaturisation Workshop
– Miniaturisation for Space –

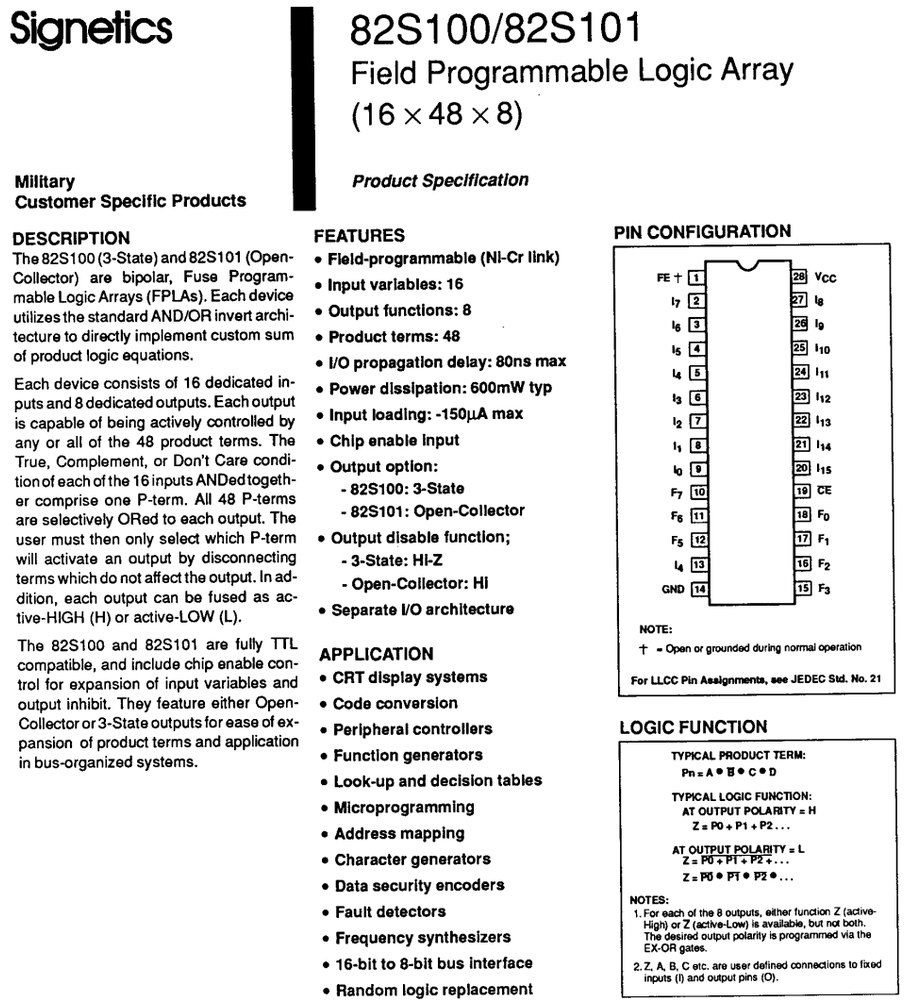
Presenter: Dick Durrant

Date: 24th October, 2012

- Background and European Context
  - An Historical Perspective Sensor Miniaturisation
- Current/Recent SEA Developments – Case Studies
  - What have we learnt and what have we not learnt
  - Architectural and interface considerations
  - Sensor requirements
  - Industrial Teamings
- Conclusions

- Space Telescope Faint Object Camera (1970s)
  - First use of integrated digital component (FPLA) for photon recognition.
  - Mass saved: 1 Kg in 78 Kg!
    But...
    - Increased flexibility for late changes
    - Lower power

- It was a start!



Signetics

82S100/82S101
Field Programmable Logic Array
(16 × 48 × 8)

Product Specification

Military
Customer Specific Products

DESCRIPTION

The 82S100 (3-State) and 82S101 (Open-Collector) are bipolar, Fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-term will activate an output by disconnecting terms which do not affect the output. In addition, each output can be fused as active-HIGH (H) or active-LOW (L).

The 82S100 and 82S101 are fully TTL compatible, and include chip enable control for expansion of input variables and output inhibit. They feature either Open-Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

FEATURES

- Field-programmable (Ni-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 80ns max
- Power dissipation: 600mW typ
- Input loading: -150μA max
- Chip enable input
- Output option:
  - 82S100: 3-State
  - 82S101: Open-Collector
- Output disable function;
  - 3-State: HI-Z
  - Open-Collector: HI
- Separate I/O architecture

APPLICATION

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit to 8-bit bus interface
- Random logic replacement

PIN CONFIGURATION

NOTE:
† = Open or grounded during normal operation

For LLCC Pin Assignments, see JEDEC Std. No. 21

LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \cdot \overline{B} \cdot C \cdot D$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L
$\overline{Z} = P0 + P1 + P2 + \ldots$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 8 outputs, either function Z (active-High) or $\overline{Z}$ (active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and output pins (O).

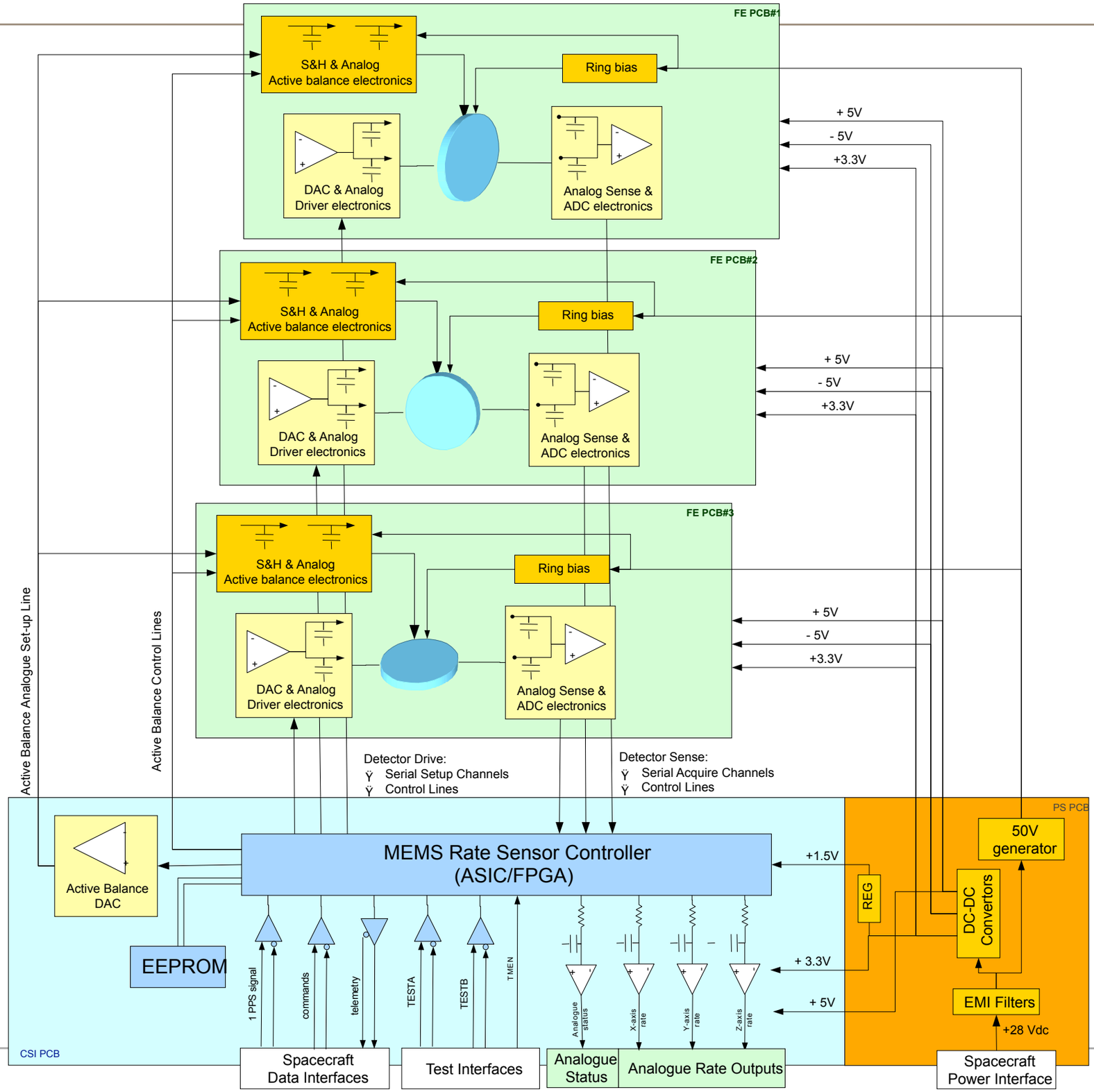
- FPGAs and ASICs 1980s
  - Initially CMOS-SOS ASICs
  - Emerging rad-hard FPGAs (Actel and Xilinx (partial))
  - Digital function miniaturisation
    - Diminishing returns over next 15-20 years.
- 1980s CCD imagers moving away from vacuum tube technologies.
  - Improvement in mass, volume and power, but difficult to use.
- 1990s, move away from fully mechanical systems to solid-state technologies.
  - Eg. FOGs
  - CMOS imagers available to replace CCDs.
- MEMs – 2000-2012
  - Detectors now smaller than electronics
  - Detector migration to space still evolving.

- Over the last 8 years SEA engaged in a number of projects addressing, supporting or exploiting miniaturisation:
  - MEMS Gyro development
  - MEMS Accelerometer development
  - Future IMU capabilities
  - Wireless Sensor networking
  - NEOMEX AOCS Electrical Interfaces
  - SMART Microsystems Study (Micro-nodes)

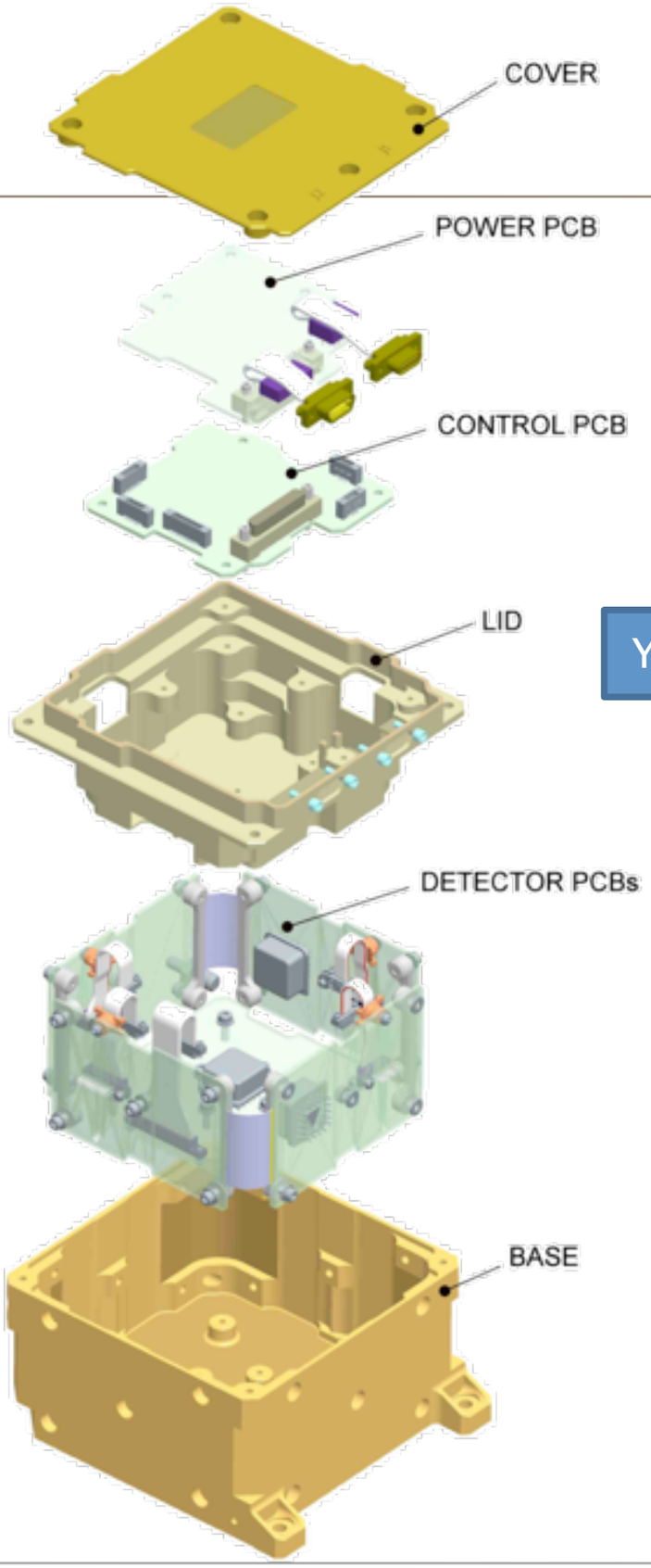
- Over the last 8 years SEA engaged in a number of projects addressing, supporting or exploiting miniaturisation:
  - **MEMS Gyro development**
  - MEMS Accelerometer development
  - Future IMU capabilities
  - **Wireless Sensor networking**
  - NEOMEX AOCS Electrical Interfaces
  - **SMART Microsystems Study (Micro-nodes)**

MEMS Case Study - MEMS Rate Sensor

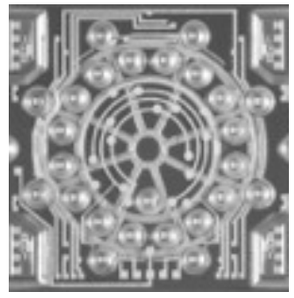
- MEMS sensor performance achieved by complex detector–electronics interaction
  - 4 control loops with supporting analogue circuits for each detector.
  - Common 50V ring bias generator and ring balancing control.
- During the development cost minimisation and ITAR restrictions increase analogue component count/size.



MRS Flight Experiment



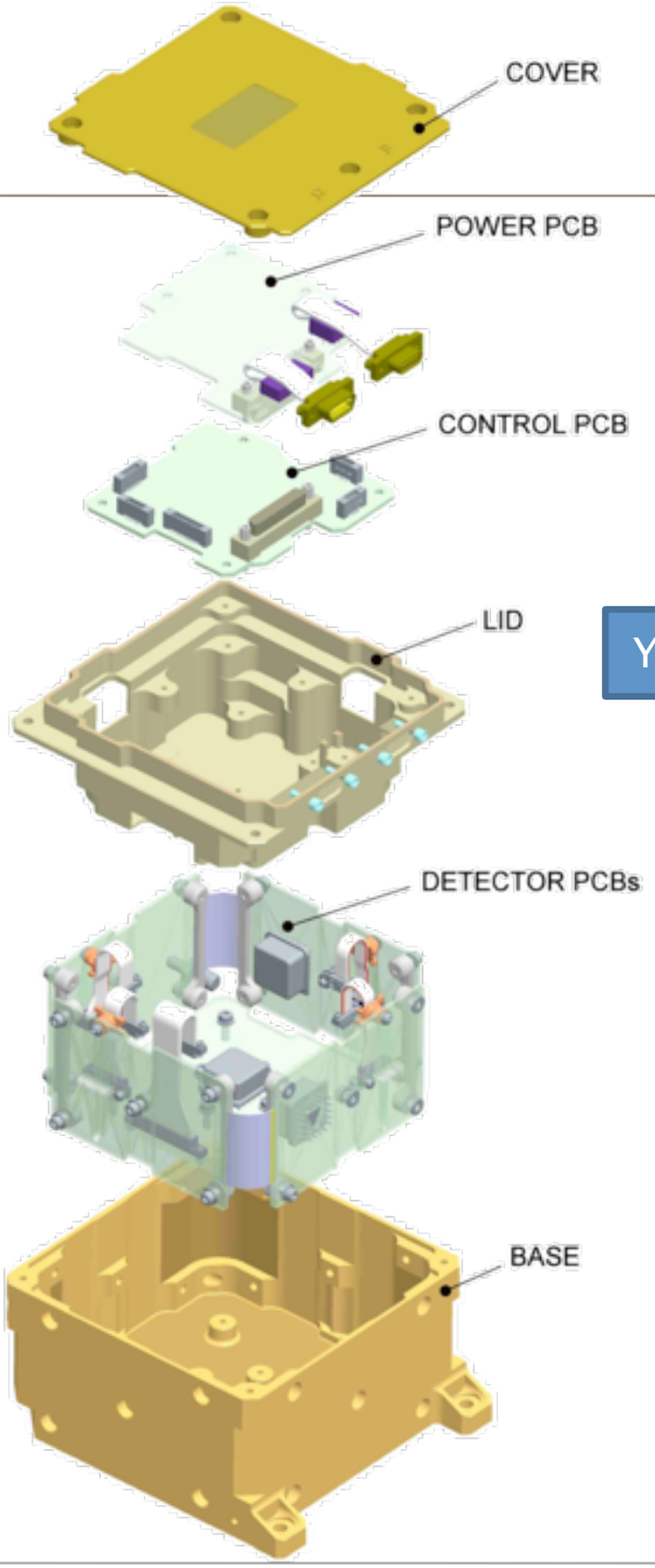
Y-axis PCB



X-axis PCB

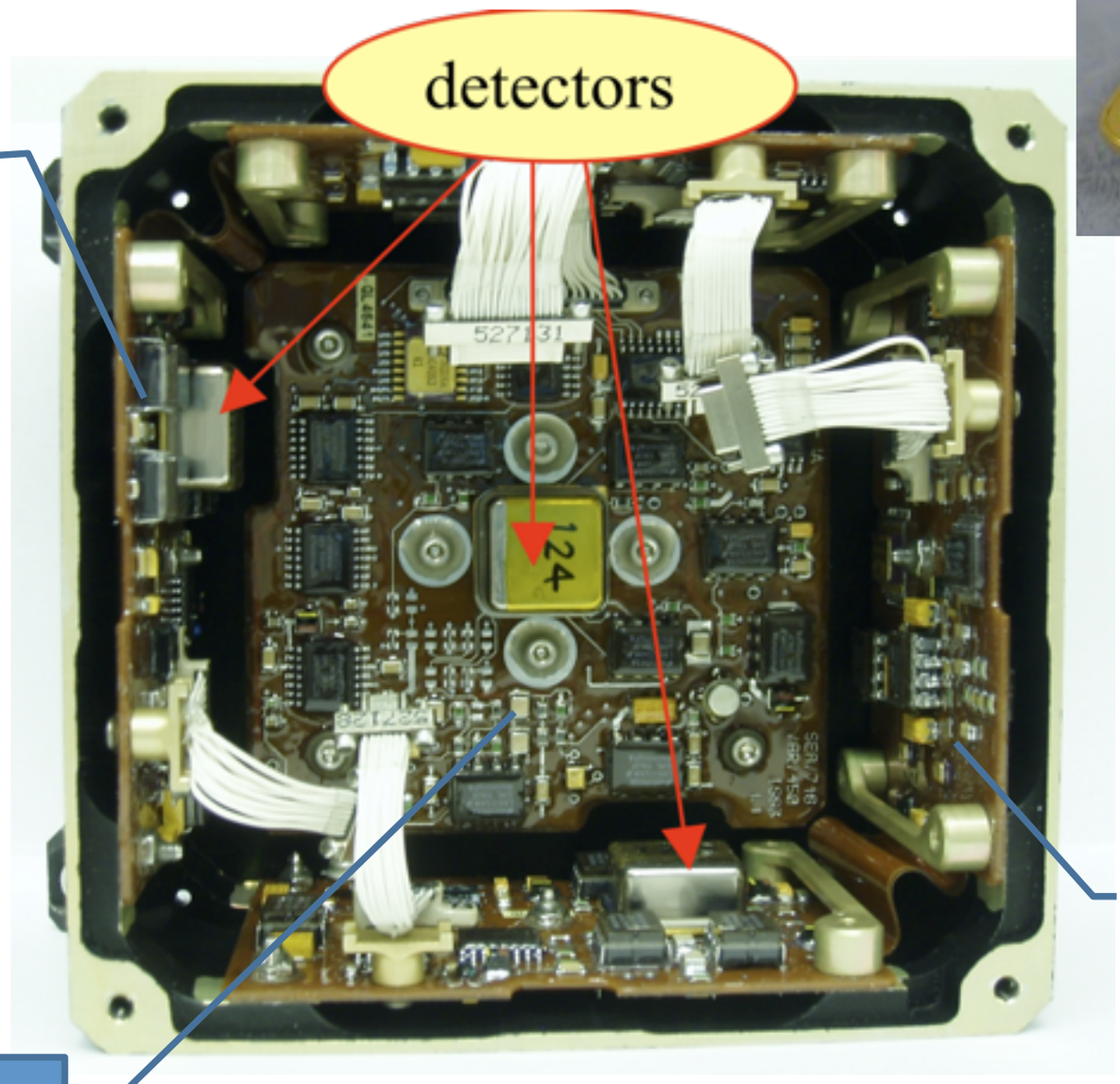
Z-axis PCB

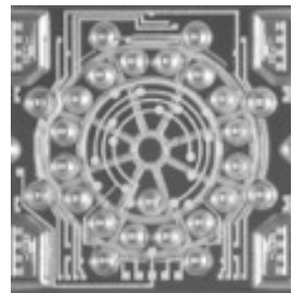
MRS Flight Experiment



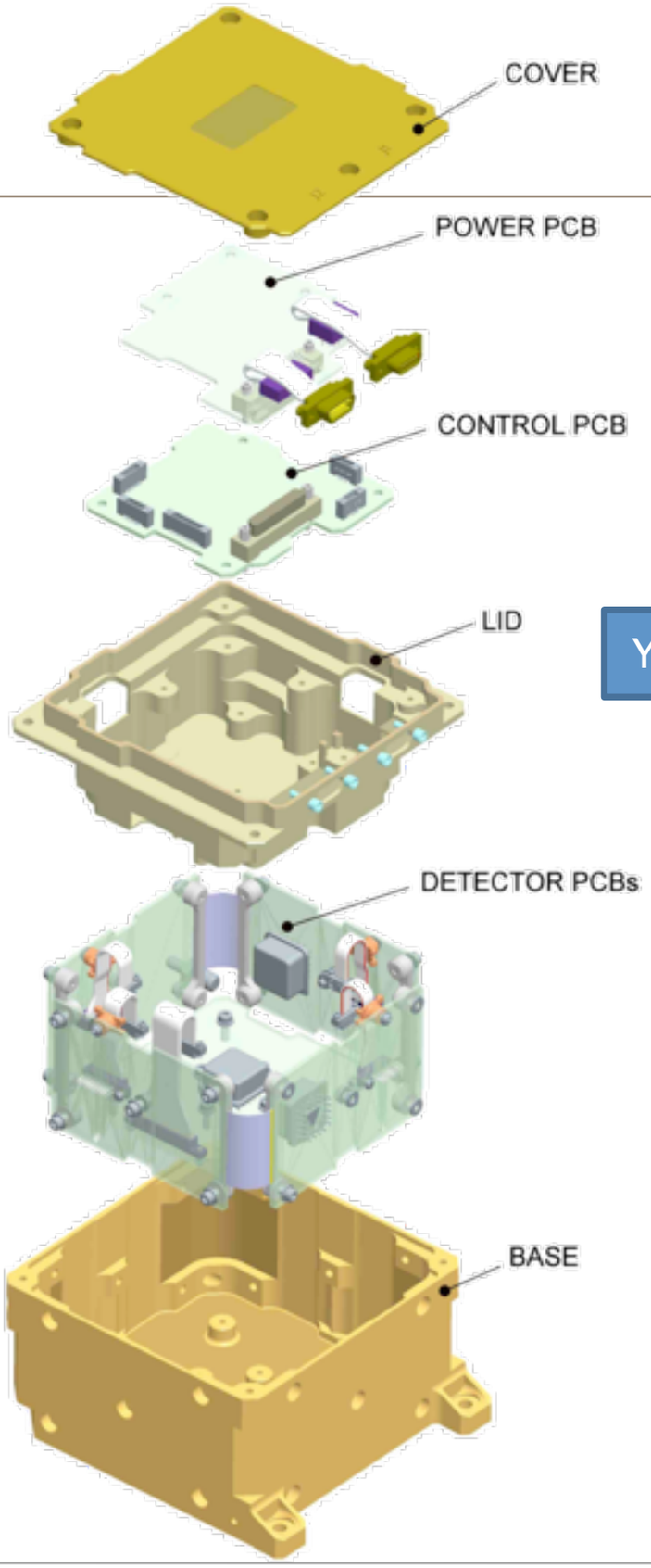
MEMS Detectors mounted on 3 off identical circuit PCBs

- Flexi central connections for side wall PCBs
- Mechanical/Thermal analyses confirm stability
- Rad-hard space qualified design

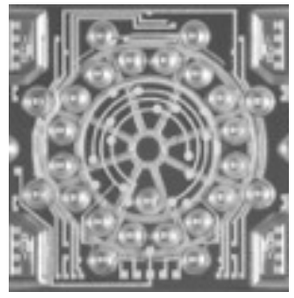




MRS Flight Experiment



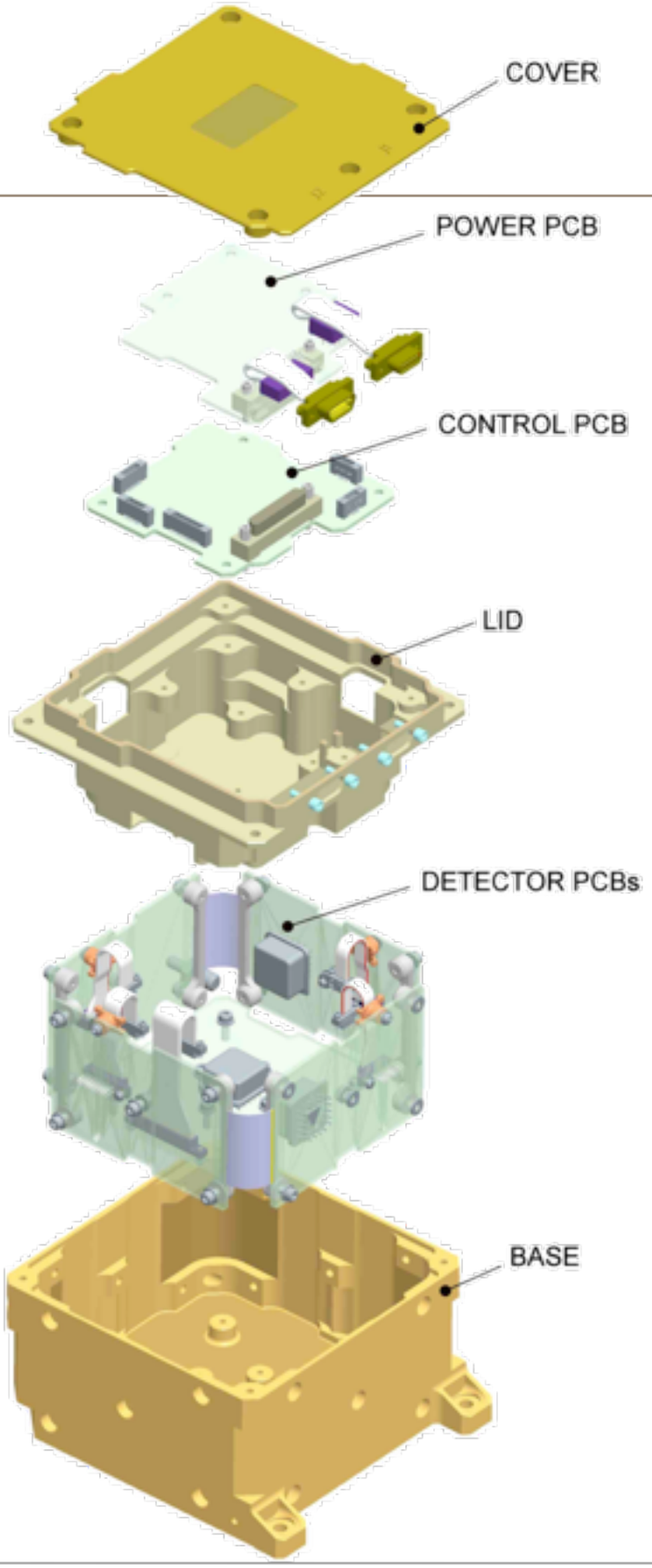
Y-axis PCB

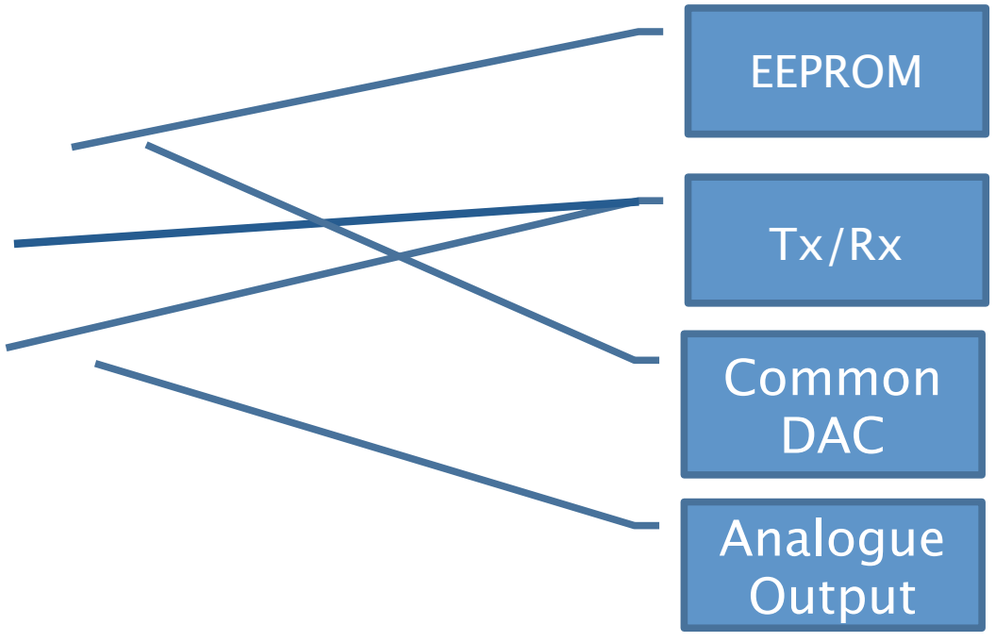


X-axis PCB

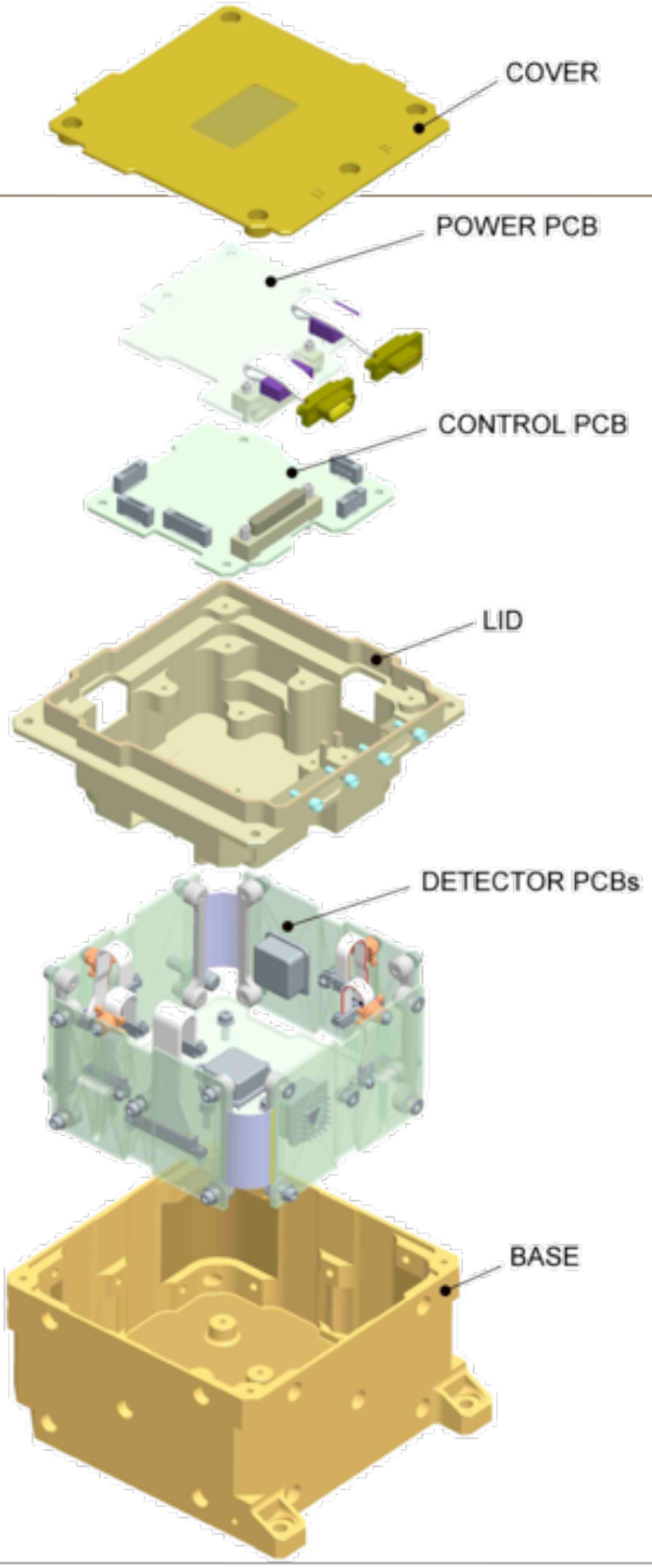
Z-axis PCB

MRS Flight Experiment



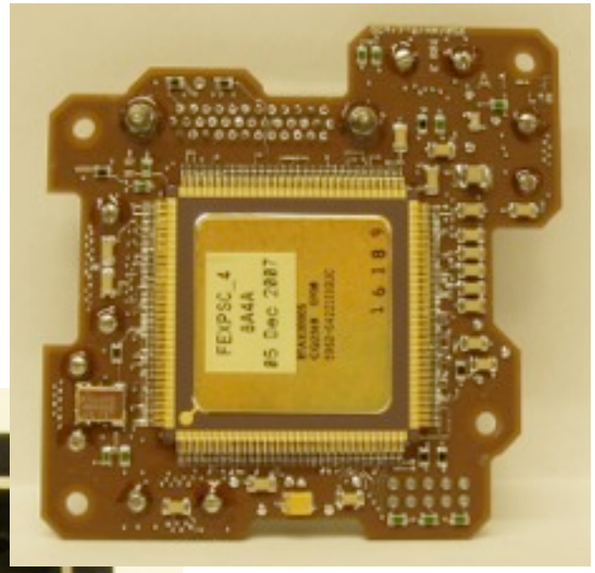


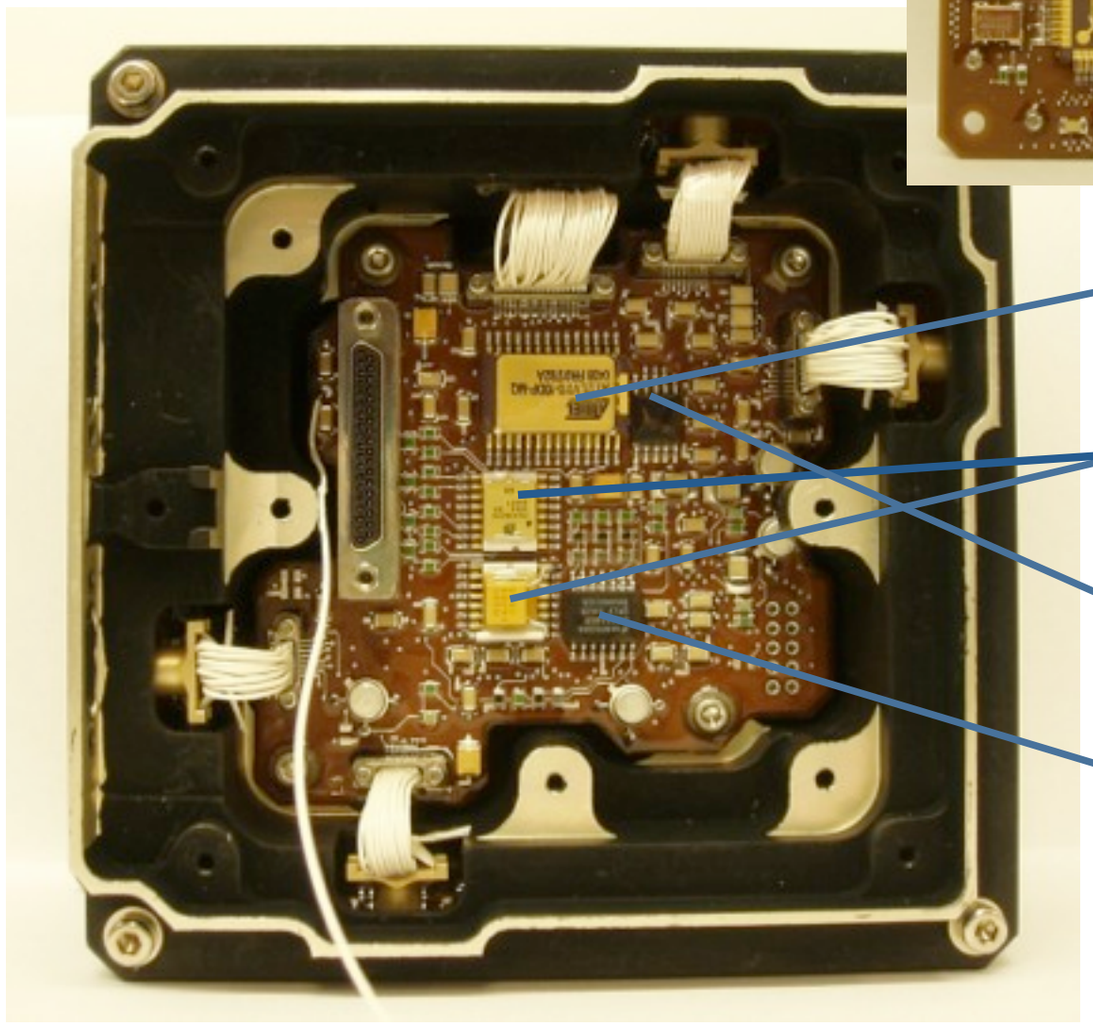
MRS Flight Experiment



Hardware (FPGA) implemented control algorithms

- Developed using SHARC/DSP
- VHDL implementation
- EEPROM parameter store





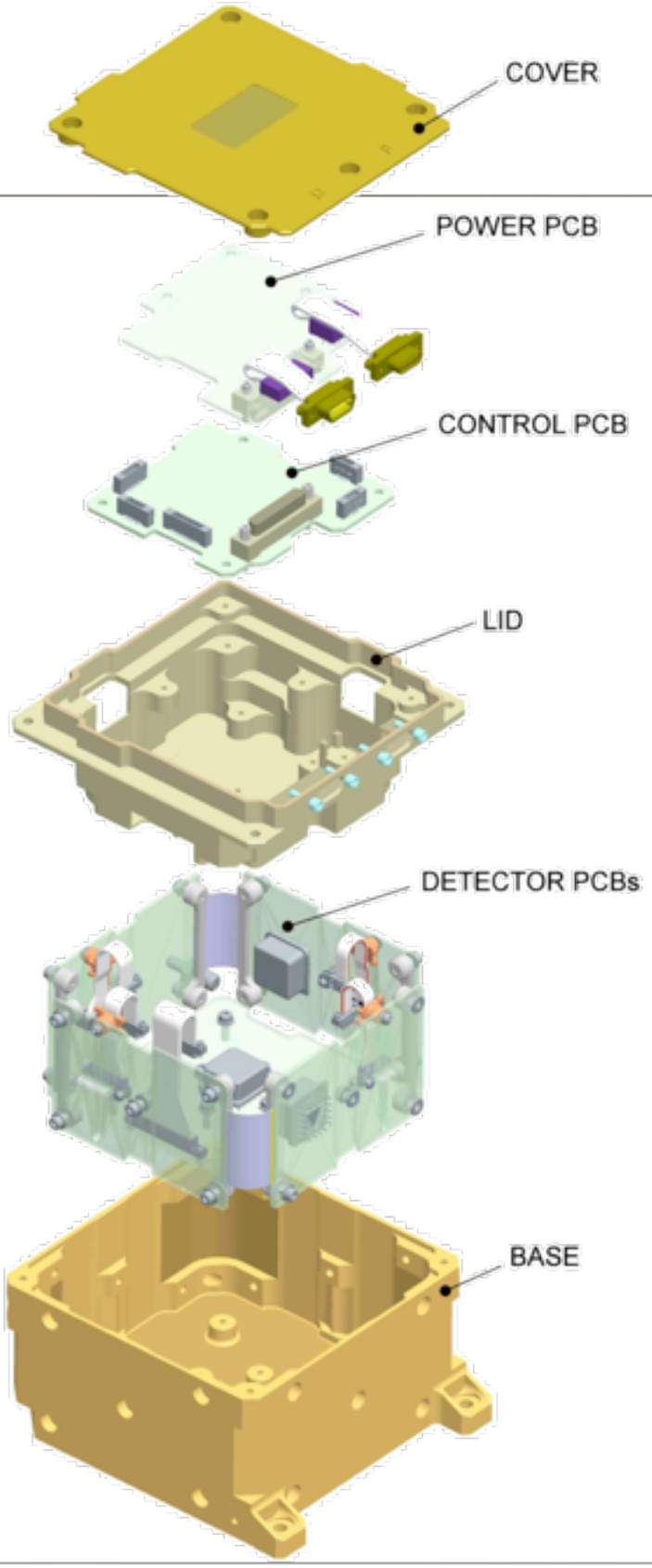
EEPROM

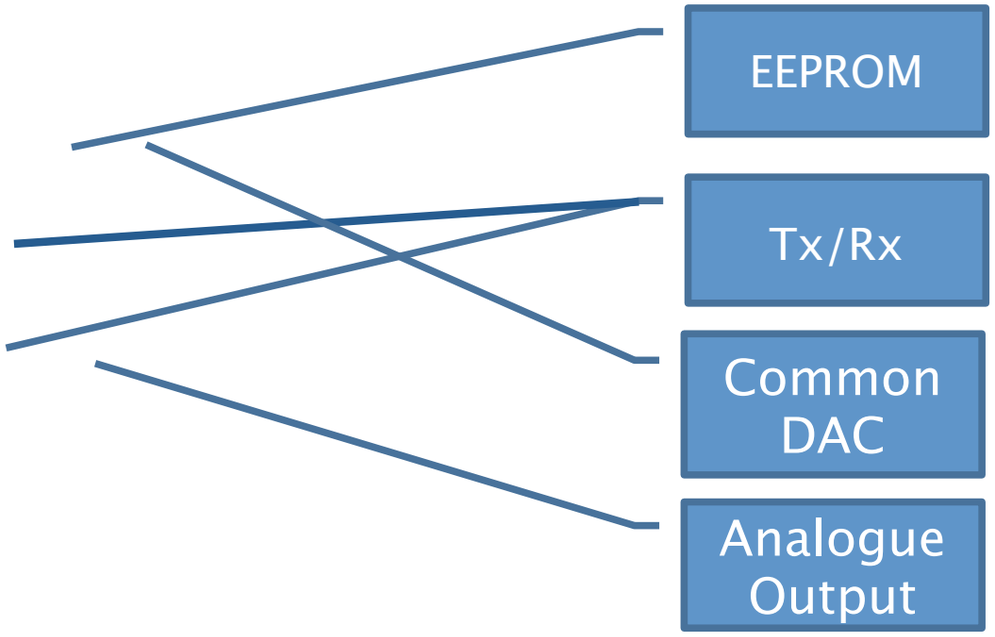
Tx/Rx

Common DAC

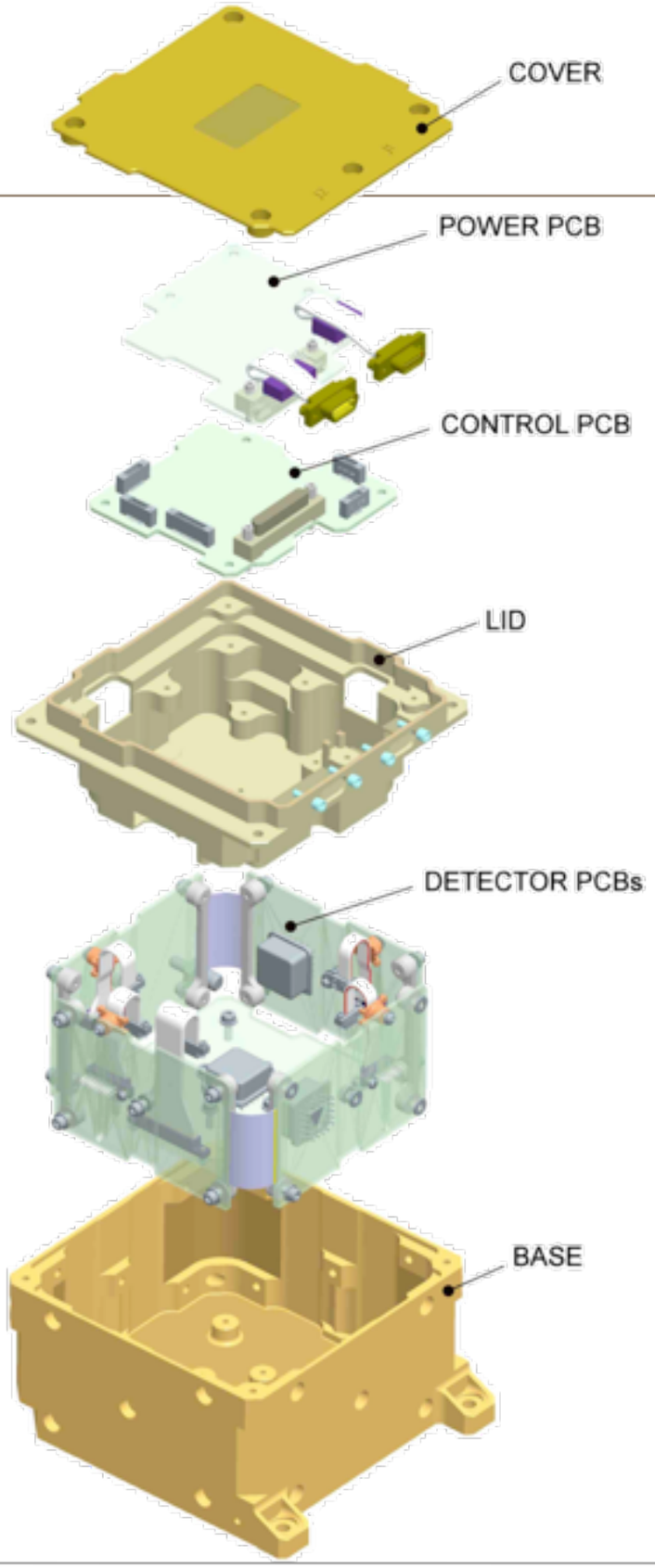
Analogue Output

MRS Flight Experiment



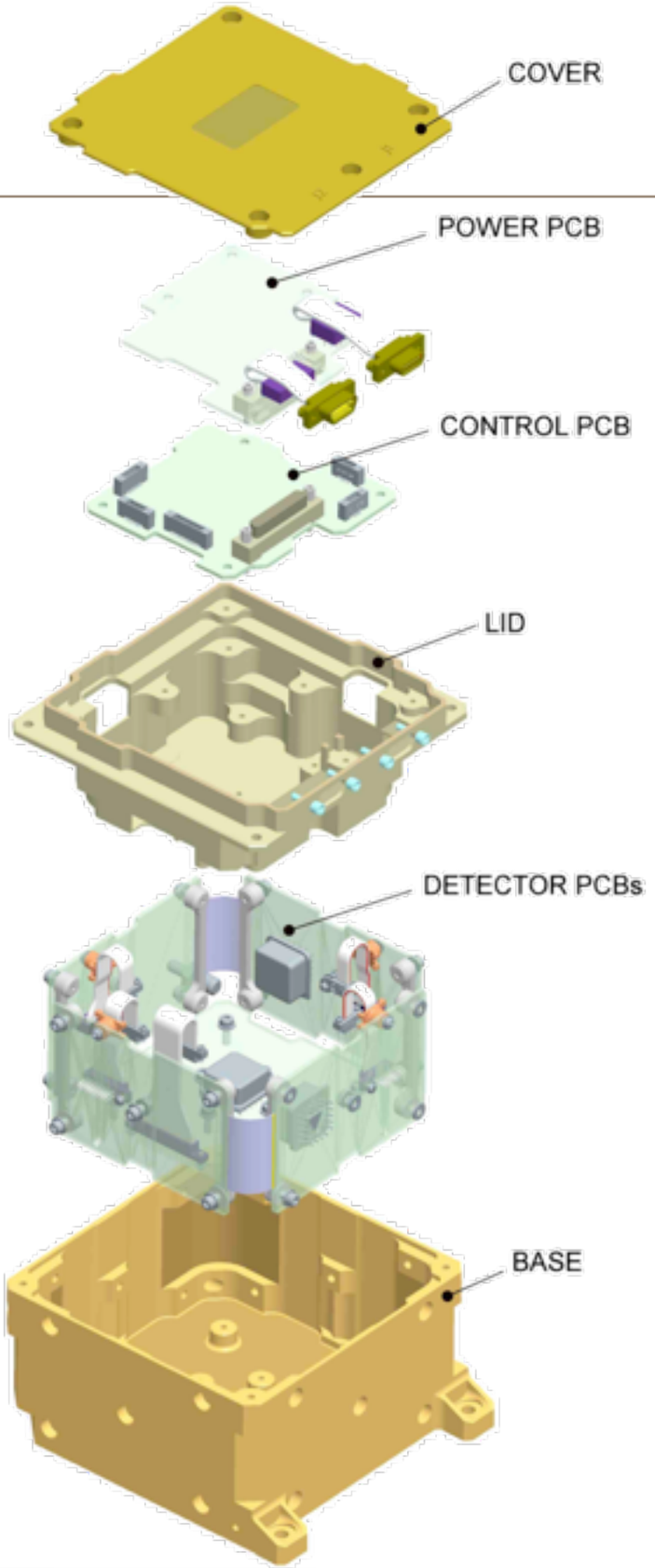


MRS Flight Experiment



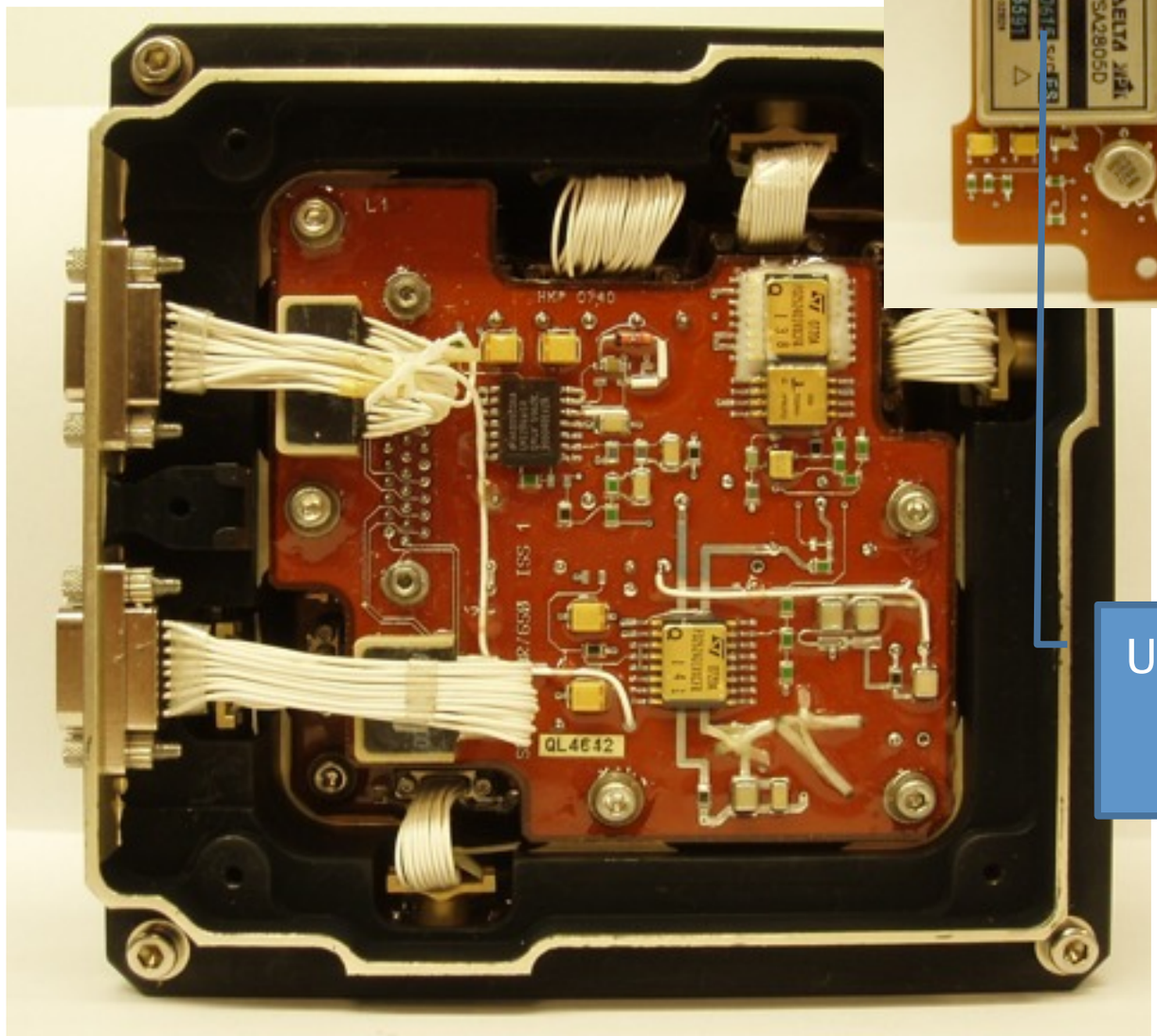
US Integrated DC-DC Modules

MRS Flight Experiment



DC-DC converter Modules based PSU
- Custom 50V bias generator
- Interconnect routing

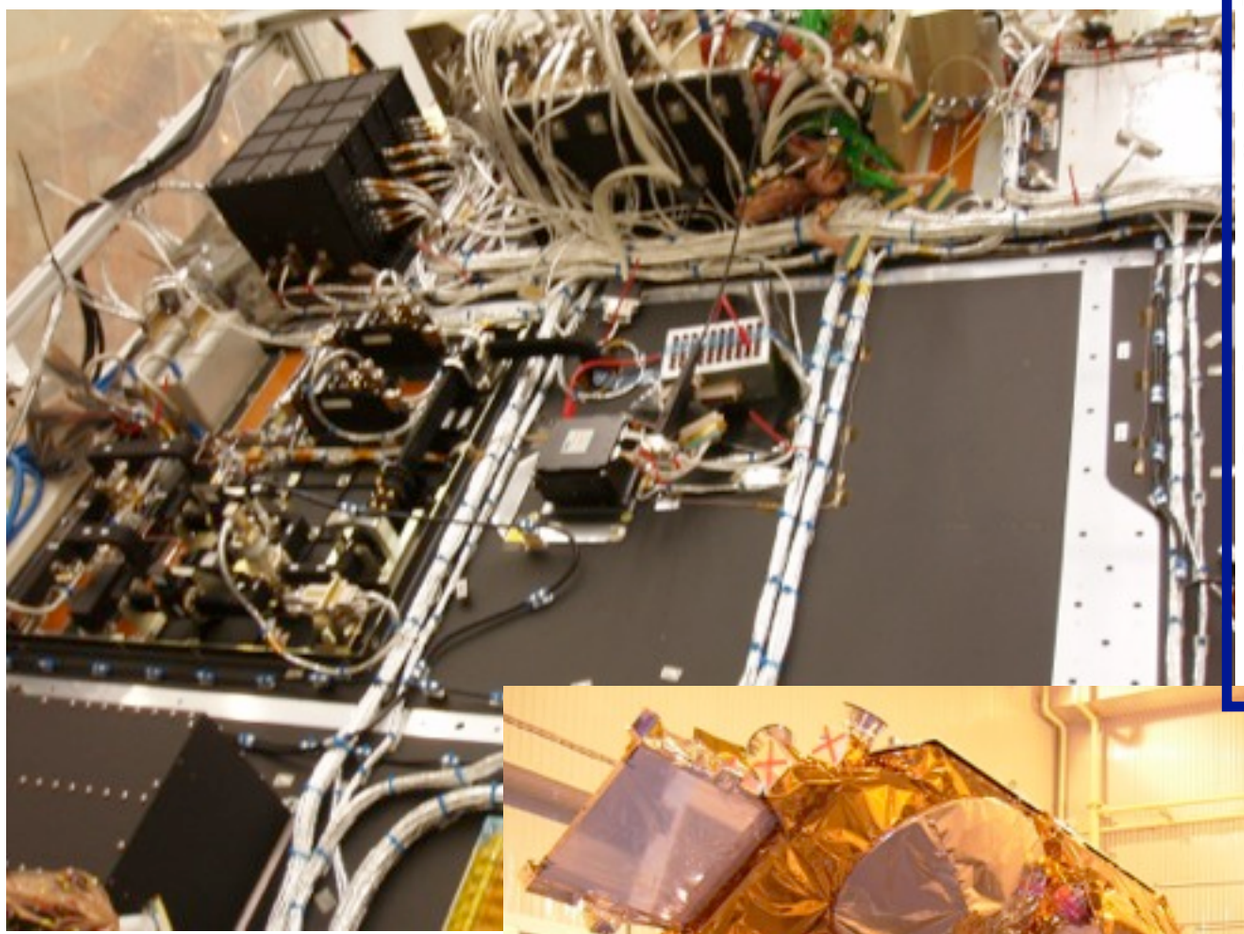
FMs discrete ITAR free design over 2 PCBs.



US Integrated DC-DC Modules

MRS FExp on Cryosat-2, and way forward

Unit still small on current spacecraft!



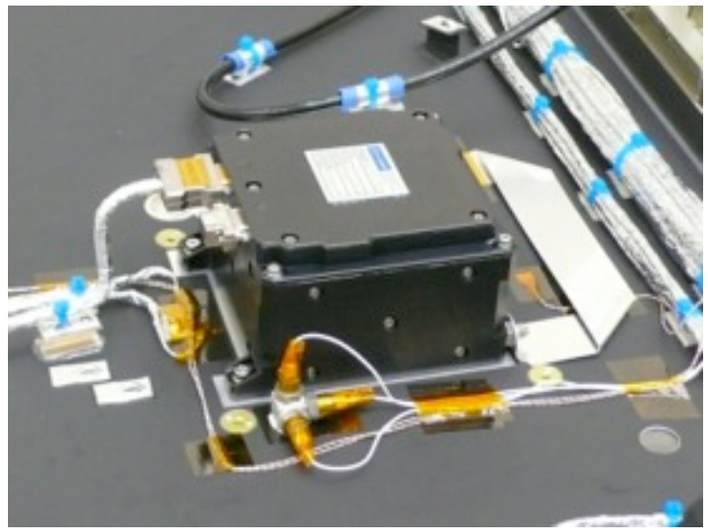
Way Forward

-Mixed signal integration of identified analogue & power functions, together with digital functions, next stage

- Reduced mass/volume, ease of accommodation at space vehicle level.

- But additional, and probably primary, advantages are:

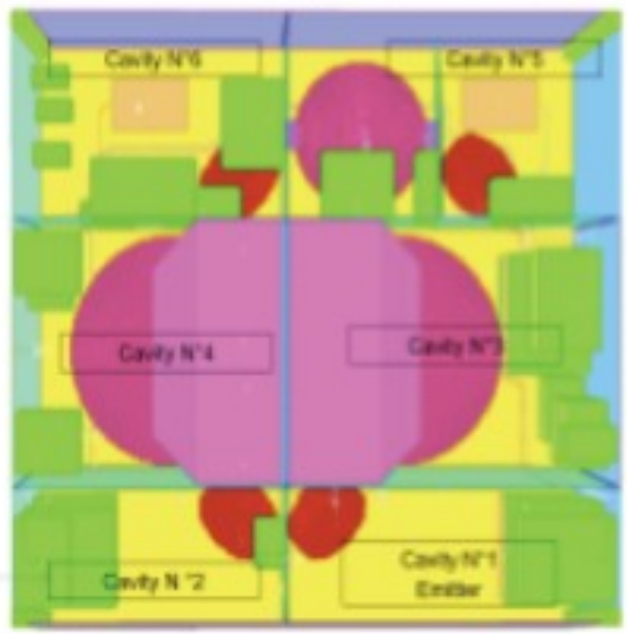
- ITAR and obsolescence mitigation.
- Reduced component/manufacturing costs.
- Reduced power supply implementation.



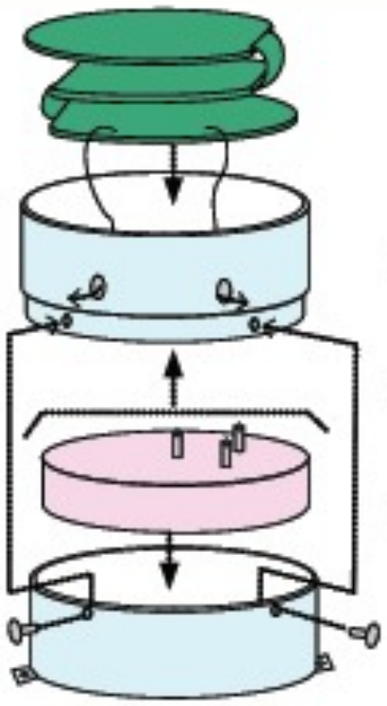
- With miniaturisation interfaces become dominant:
  - Number of wires
  - Connectors
  - Number of interface types
- RF Wireless is a potential future approach.
- Technology demonstration activity undertaken in 2009-2011 for a Low Power Proximity Network of sensors.
  - Intra-spacecraft and AIV/EGSE support.
    - AIV instrumentation possible early application.
    - SEA already using tablet PCs/remote access with wireless in the lab to ease user-test interface.

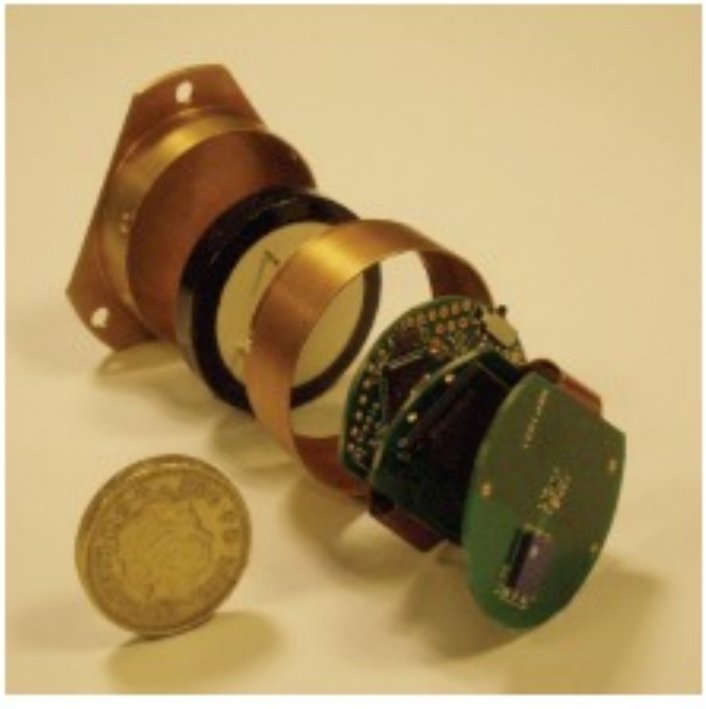
LPPNS Demonstration: Spacecraft Testing

- Spacecraft application modelling and testing performed by Astrium (Toulouse)
  - Link budget measurements demonstrated minimum +15dB margin in worst case configuration (opposite cavity between emitter and receiver).
  - EMC compatibility demonstrated against Astrium Telecom existing requirement:
  - +18dB margin between LPPNS RE and S/C unit RS
  - +46dB margin between LPPNS RS and S/C unit RE
  - Good correlations on the power distribution inside the S/C cavities between test and simulation results.
- Key issue with demonstrator system was robustness at higher data rates and battery lifetime.
  - Addressed in updates for launcher testing and for FM prototype development

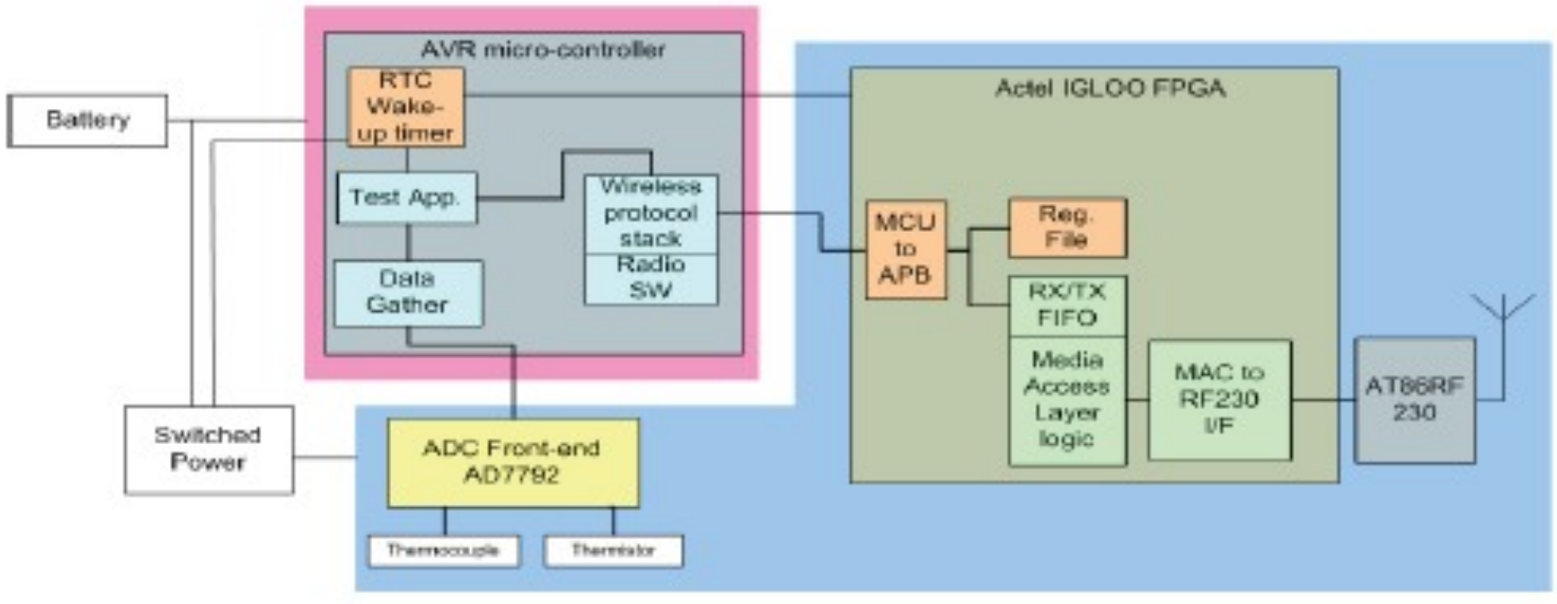


LPPNS FM Prototype



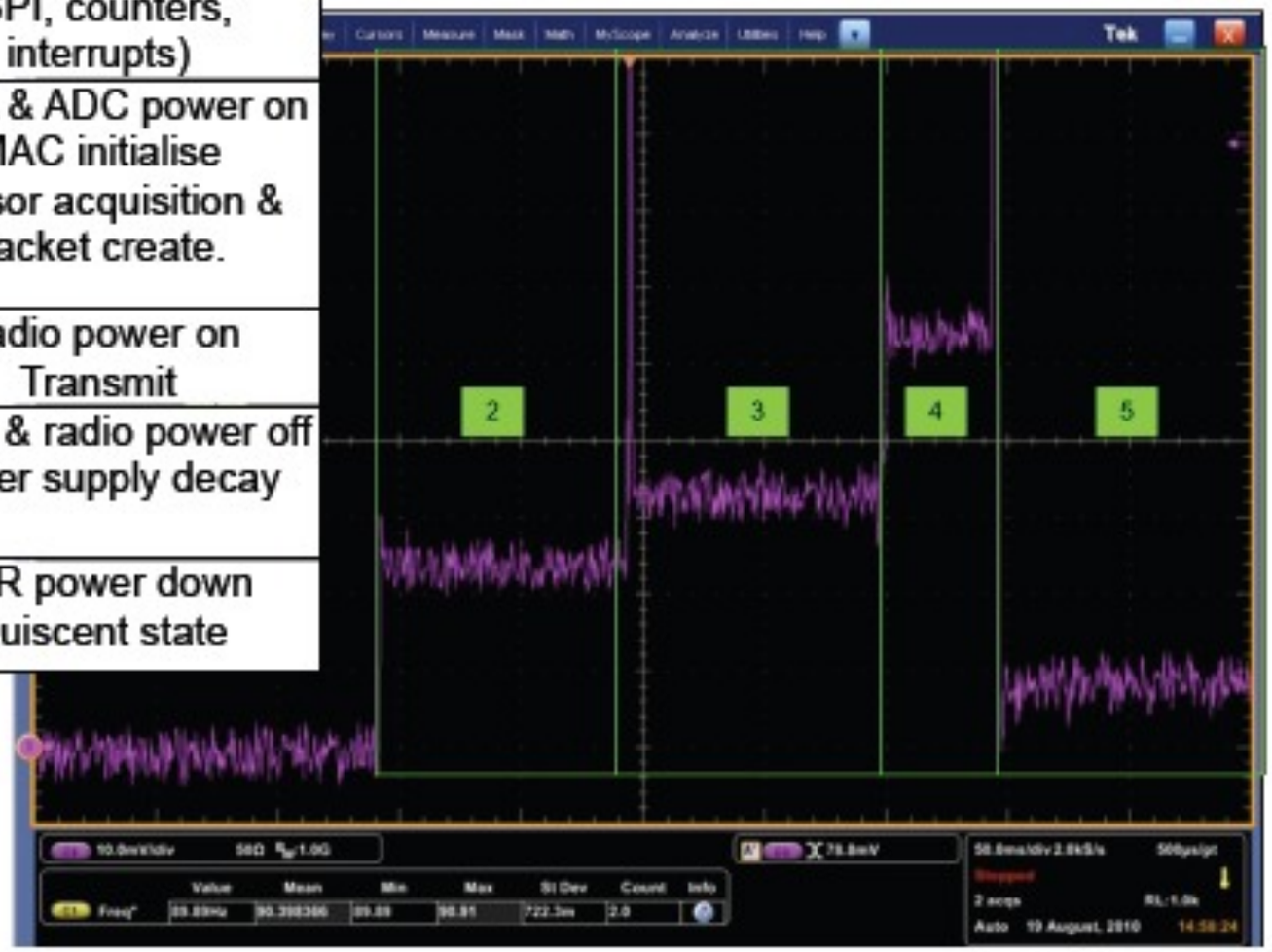


- FM prototype developed to:
  - Evaluate a low power application using COTS components (ie. FPGA based).
  - Provide a build standard capable of early environmental testing.
- Power reduction through:
  - Maximising AVR power down features.
  - Maximising Actel IGLOO very low quiescent current.



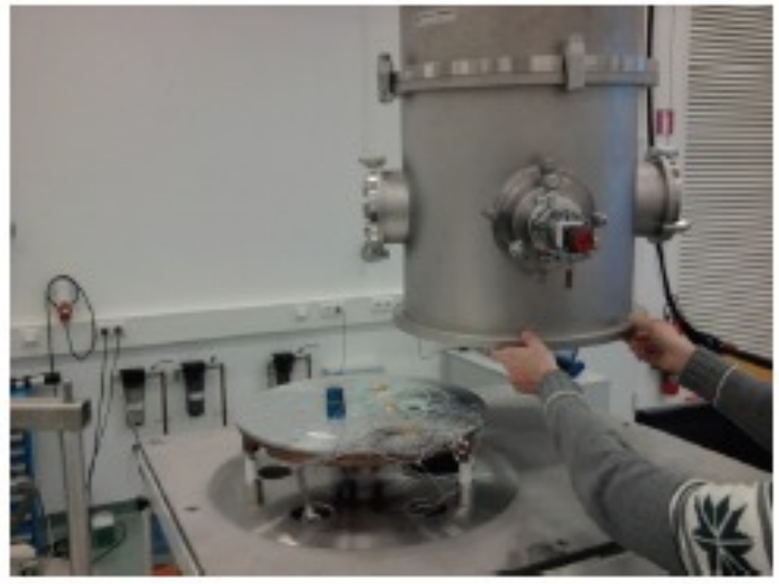
FM Prototype Power Profiling

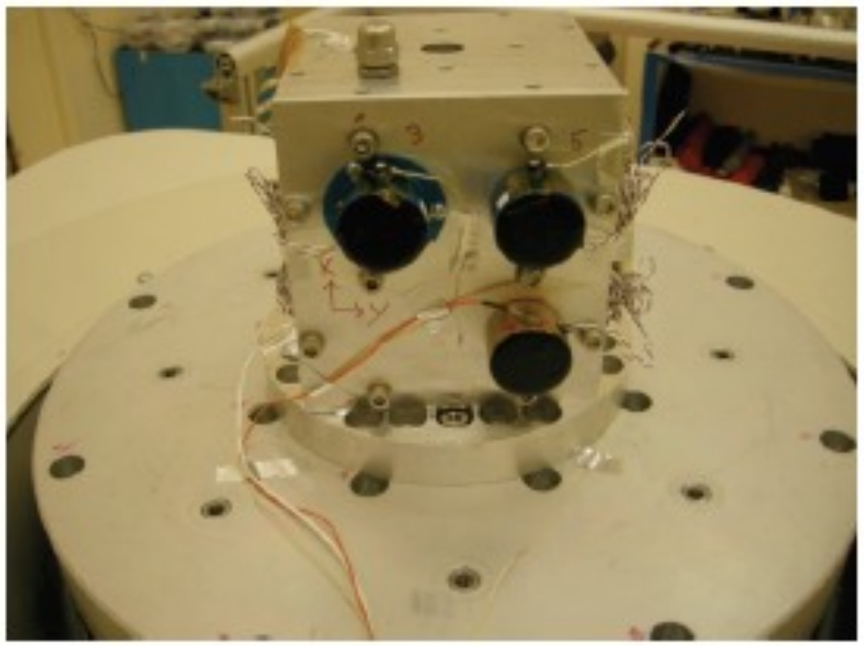
Mode	AVR	FPGA	Radio Transceiver	Current	Comment
Sleep	Off	Off	Off	0.04 mA	Quiscent state
Initialise	On	Off	Off	1.75 mA	AVR Wake-up I/O Initialise Peripherals initialise (SPI, counters, interrupts)
Acquisition	On	On	Off	2.25 mA	FPGA & ADC power on MAC initialise Sensor acquisition & packet create.
Transmit	On	On	On	3.25 mA	Radio power on Transmit
Power Down	On	Off	Off	1 mA	FPGA & radio power off Power supply decay
Sleep	Off	Off	Off	0.04 mA	AVR power down Quiscent state

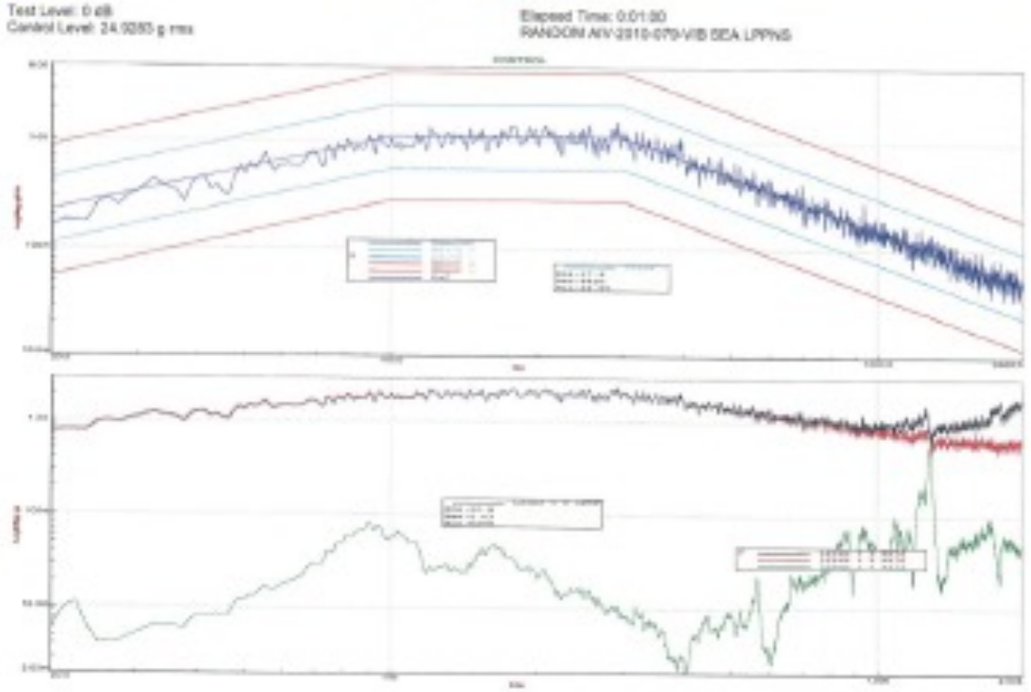


LPPNS FM Prototype Environmental Testing

- Vibration Testing successfully performed over launch profile.
  - Module attachment used bolts and double-sided tape.
- Temperature sensor calibration performed in SEA thermal chamber.
- Thermal/Vacuum testing performed over range -10 to +60 degC at ESTEC







Architectures/Interfaces Case Study – Micro-Nodes

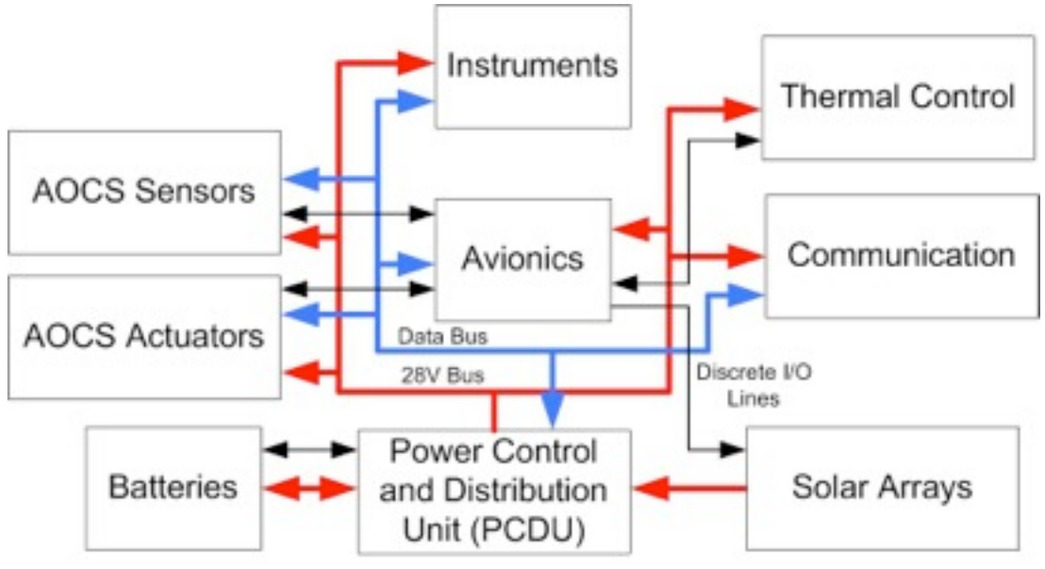
- Current ESA activity led by SEA with BAE SYSTEMS (ATC).
  - Study of de-centralised architectures making best use of:
    - current integrated electronics
    - MEMS technologies.

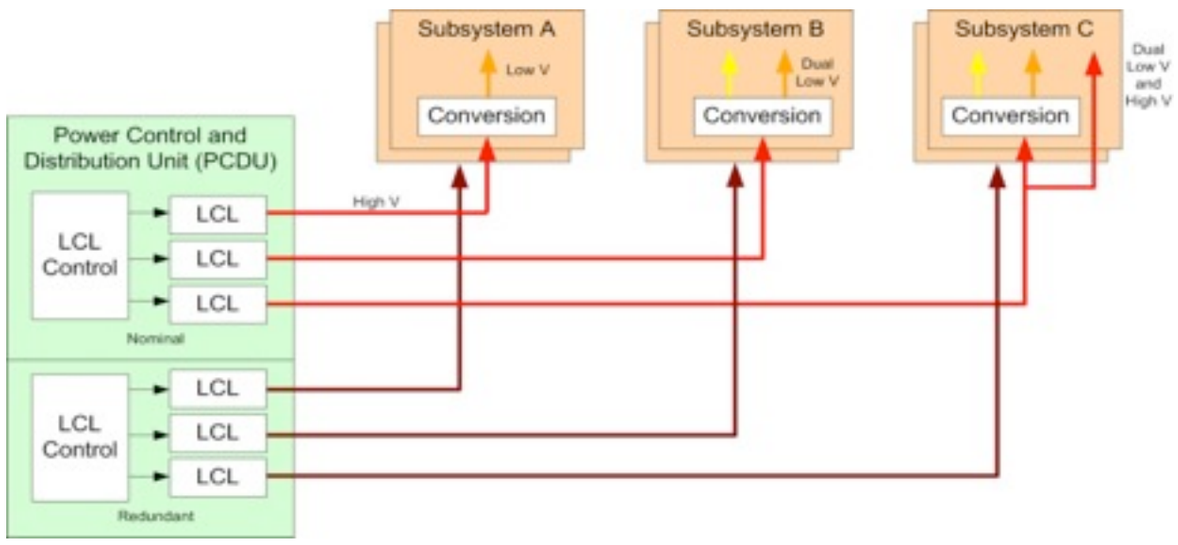
- From MNT Round Table 2012 – Session 8

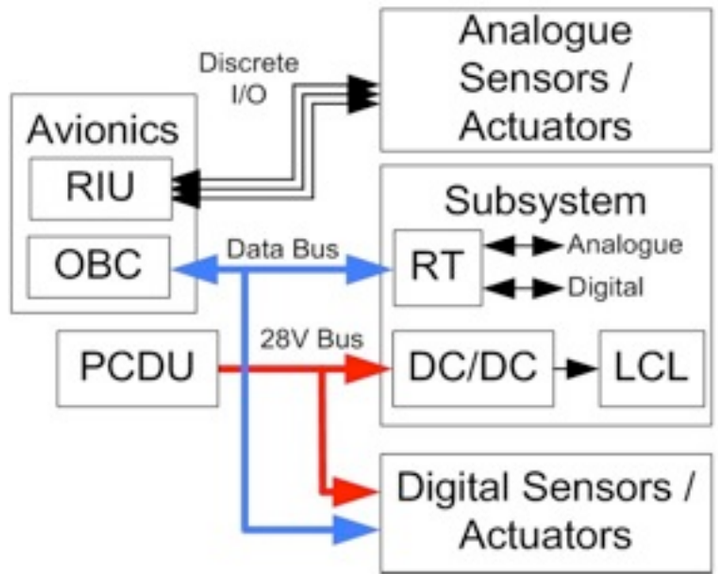
Centralised System Architecture

Traditional Centralised System

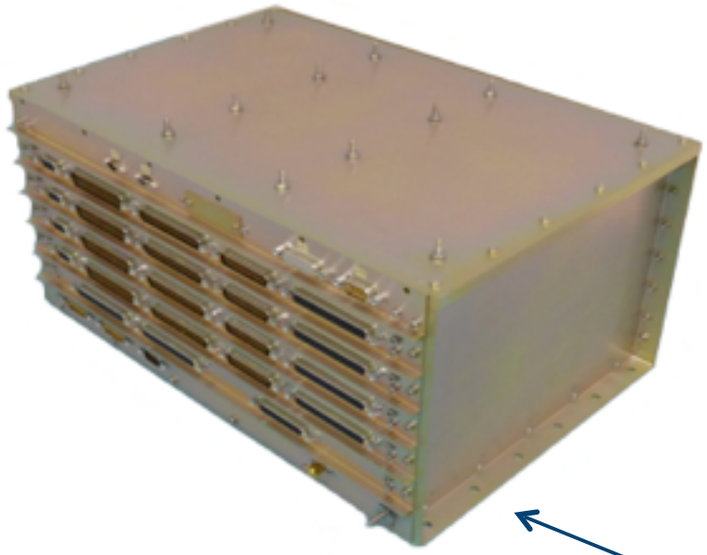
- Large Harness Mass (typically 9% of spacecraft mass).
- System Vulnerability to Failures.
- PDCU with separate Nominal and Redundant harnesses to each Spacecraft Module.



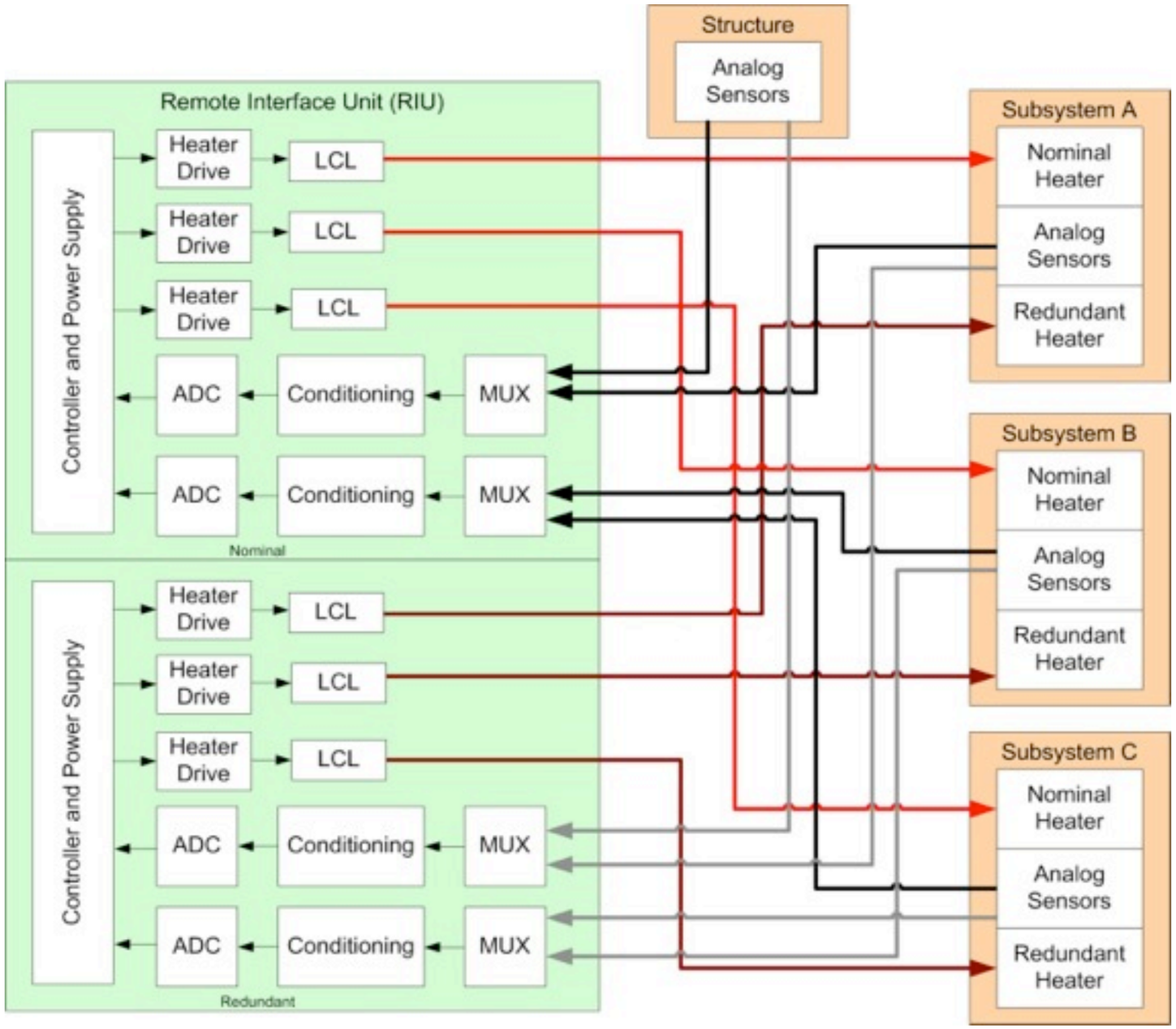




Centralised System Architecture including an RIU



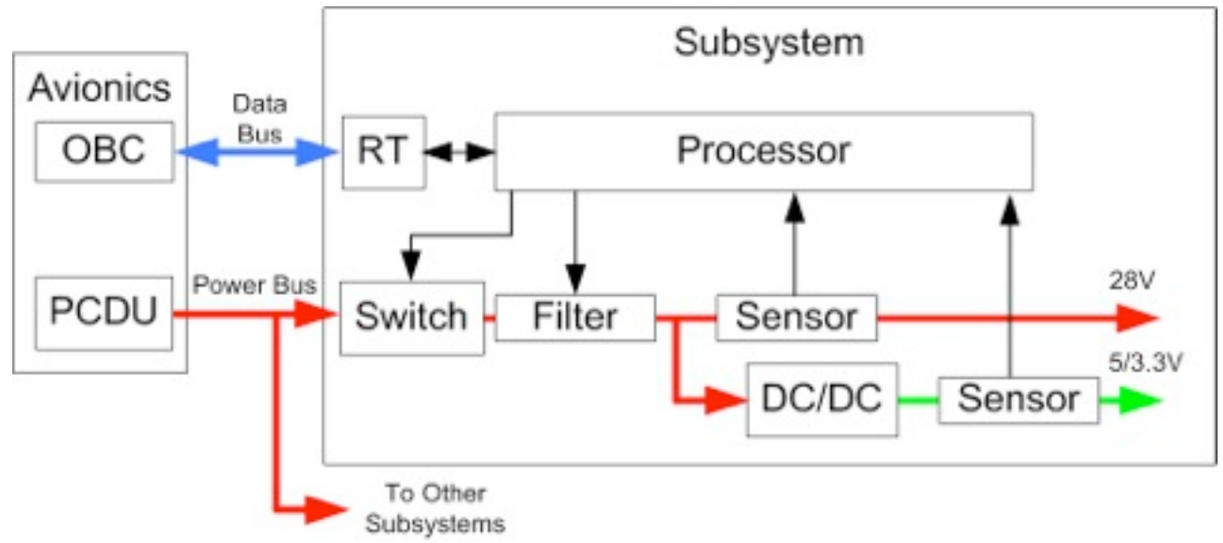
BepiColombo MPO Remote Interface Unit (RIU) built by SEA illustrating a typical centralised system with 360 Thermistor inputs, 56 Analogue inputs, 144 Relay Status and 32 Bi-level digital inputs.
16 Thruster Heater outputs, 8 Thruster Valve outputs and 8 Latch Valve



Why Use a Decentralised System ?

De-centralised System

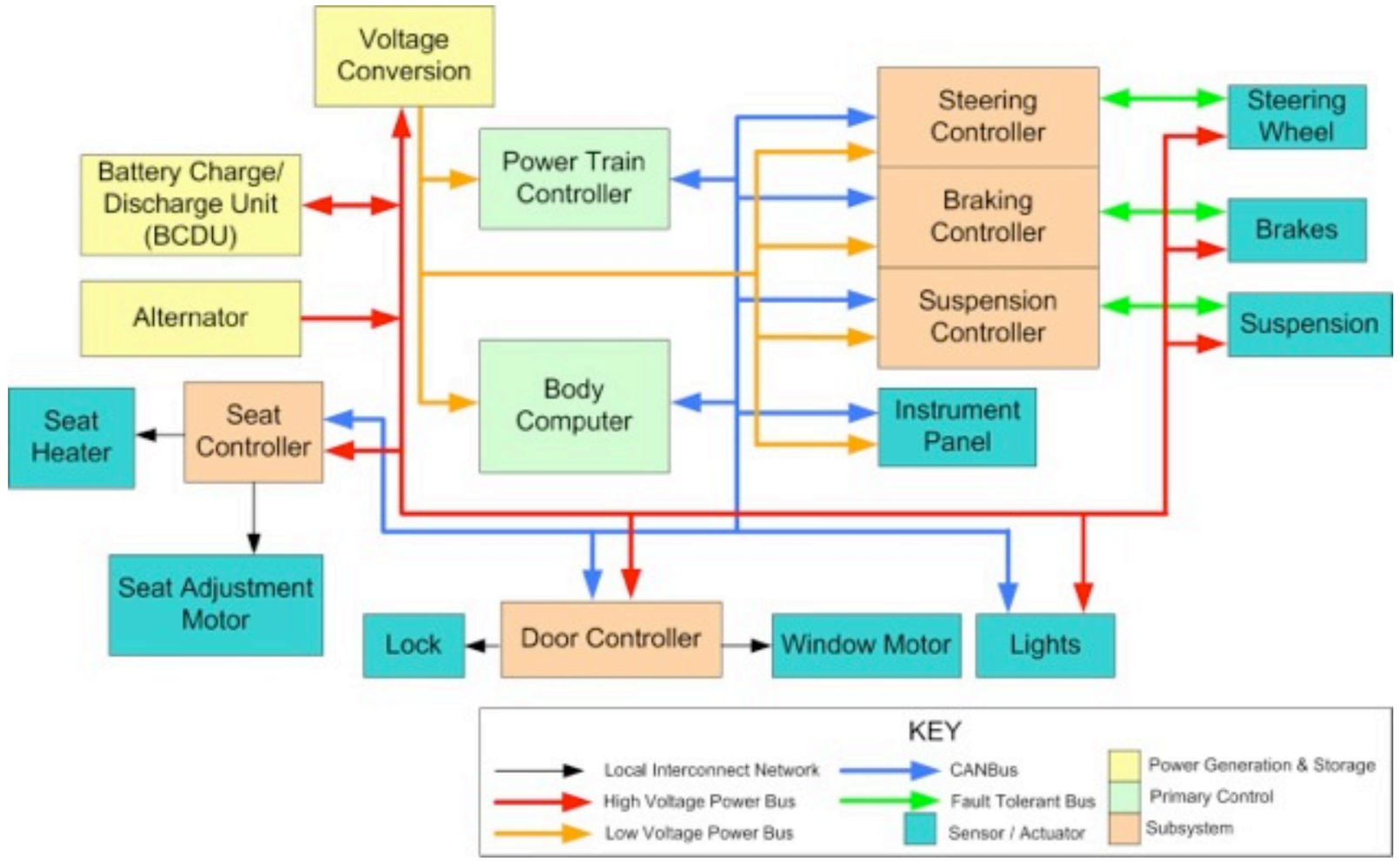
- Reduced Harness Mass.
- Localised Control Capability.
- Increased System Reliability due to less centralised architecture.
- Micronode design using Miniaturisation Technologies to achieve low mass, power & volume standardised modules.



Why Use a Decentralised System ?

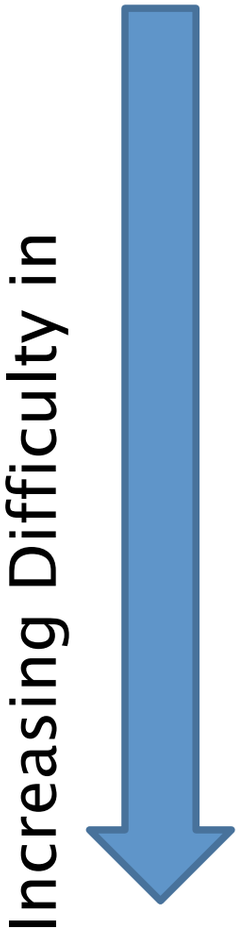
De-centralised System

- Synergy with modern de-centralised Automotive Systems.



Micronode Potential for MNT Utilisation

Micronodes are intended to be generic systems used on many satellites. This should alleviate some barriers to space qualification of MEMS in these applications



Barriers to Qualification;

- **Temp Range**
  - Not a big problem with many MEMS. Can be a problem with low cost packaging
- **Shock/ Vibration**
  - Can be a problem for sensitive MEMS devices (pressure, inertial, switch etc). But many examples where this has been overcome – especially spin in from Aerospace/Defence
- **Packaging**
  - Robustness hermeticity/outgassing Is a problem with the low cost commercial solutions
- **Radiation**
  - Almost universally the biggest barrier

Micronode Potential for MNT Utilisation

Which MEMS Devices could be used in Micronodes?

Increased

- COTS MEMS
  Very few. Most commonly non-rad hard electronics is the main issue.

- Adapted MEMS
  Most easily adapted are bulk Si fabricated devices (surface micro-machined often have integrated "terrestrial" CMOS)

- Bespoke MEMS
  Beyond one off science experiments there may be examples with sufficient volume or benefit at System level
  to justify development/qualification

Increased Ease of

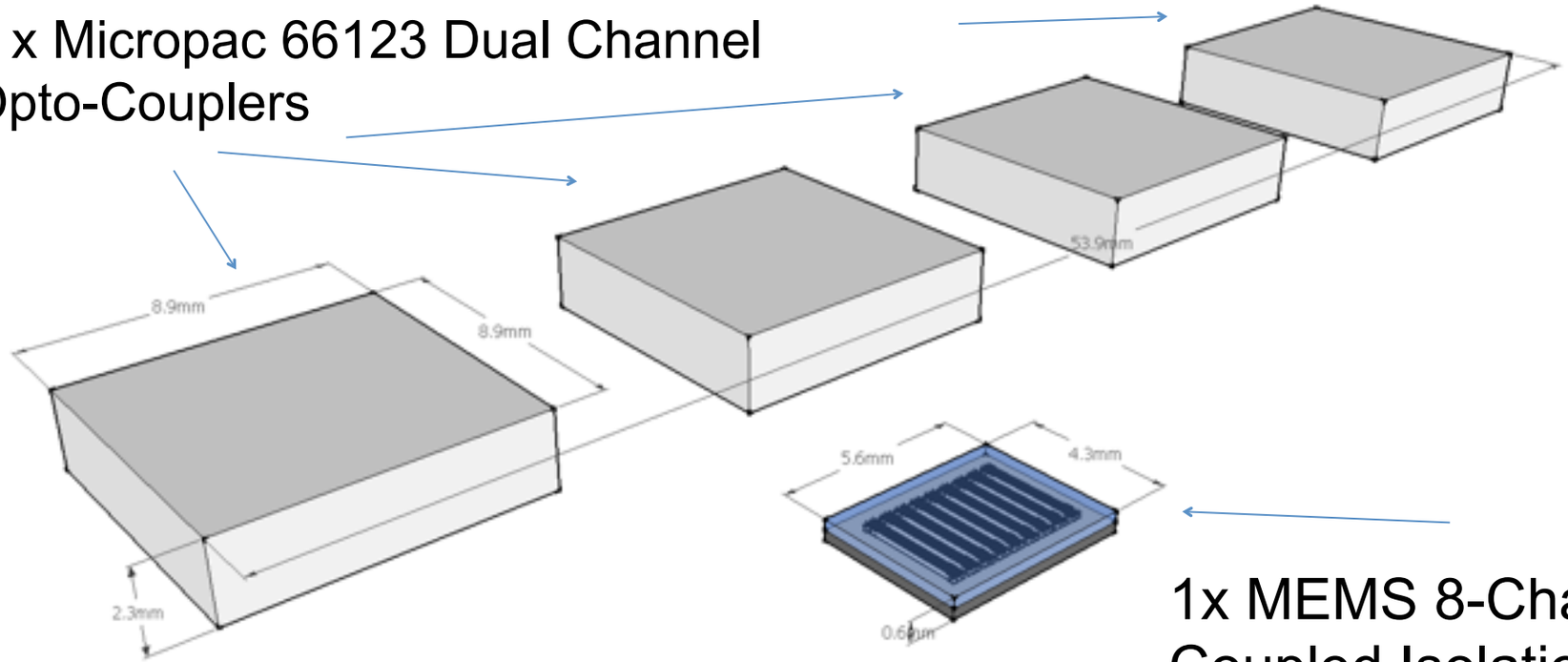
Examples for MNT Utilisation

Specific Example #1: Electrical Isolation Barrier

Main issue long term stability of Opto Isolators – RADIATION TOLERANCE & CTR Degradation

Potential Solution : replace with Capacitive Isolation Barrier

4 x Micropac 66123 Dual Channel Opto-Couplers



Advantages:

- Radiation Hard
- Much Smaller footprint
- JFET output
- Wafer level Packaged

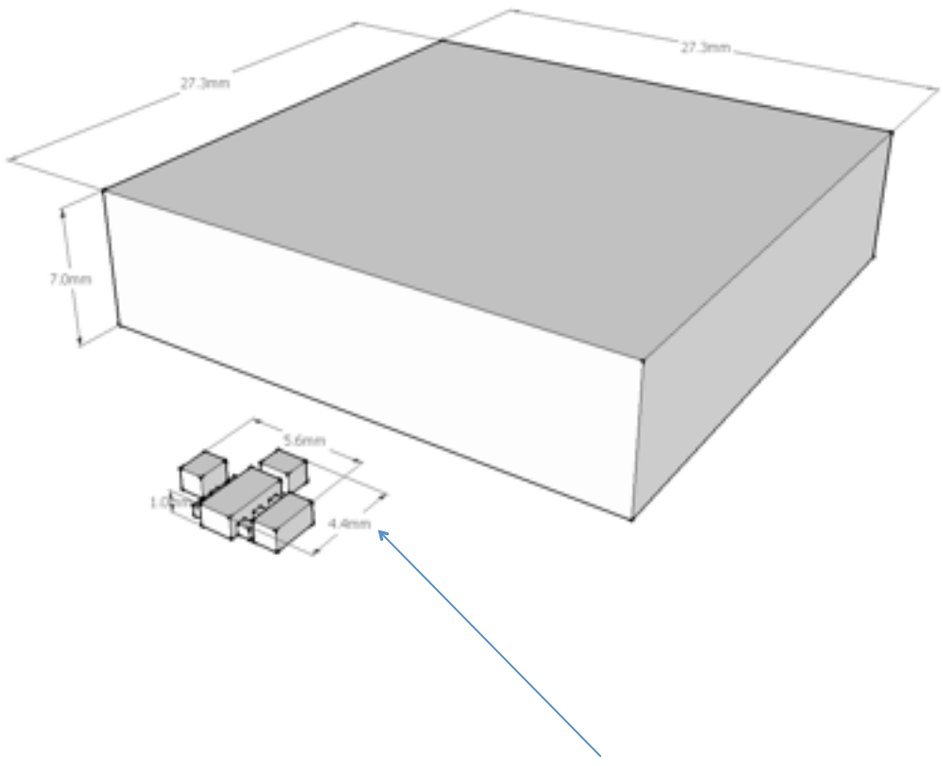
1x MEMS 8-Channel Capacitively Coupled Isolation Barrier
Rad hard JFET output

Examples for MNT Utilisation

Specific Example #2: DC-DC Converter

Main issue Space Qualified components – ITAR Free

Potential Solution : replace with Bespoke Rad Hard ASIC + MEMS Capacitors as SIP Chip
e.g. DC-DC Converters - SMSA 5W Series



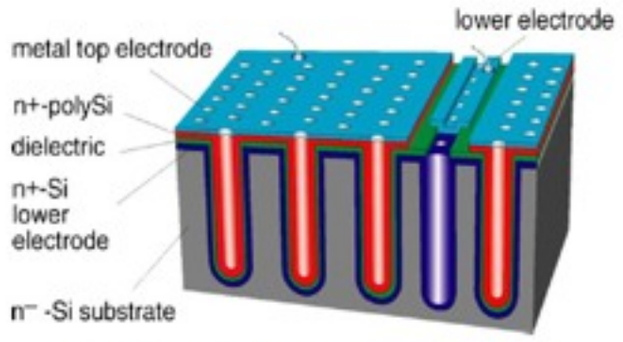
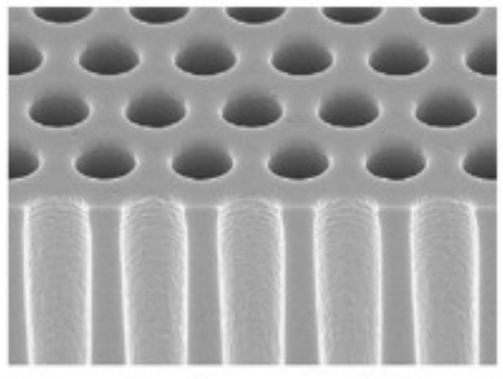


Fig. 2. Scheme of a 3D capacitor in PiCS technology.



Charge Pump (ASIC + 3 capacitors)

Advantages

- Radiation Hard
- ITAR Free
- Much Reduced Footprint
- Wafer level Packaged

Other Miniaturisation Challenges #1: So, really, what are the requirements?

- Often a trend in defining requirements based on:
  - What has worked before.
  - What existing equipment can provide.
    - ie. I want the same as before but smaller and cheaper.
  - This will drive MEMS development cost.

- Miniaturisation development is expensive
  - Production provides low cost – but only for high volume!
  - Setup for production is expensive in all cases.
    - MEMS for space at envisaged performance levels is not mature.
    - Lessons need to be learnt from terrestrial best practice.
      - Eg. MEMS, allow for several wafer runs, analysis->test->analysis->test->analysis, etc, etc.
  - In general space missions are pushing the envelope in terms of performance parameters for MEMS GNC sensors.

- Significant cost savings could be possible by providing true requirements.
  - Key point of what can be done at system level to reduce development costs.
  - Early system <- > sensor collaboration necessary.

Other Miniaturisation Challenges #2: Industrial Teamings and Long Term Engagements

- With emphasis on MNT technologies majority of technology availability and IP is from terrestrial developments.
  - Essential to ensure engagement of terrestrial partner through to production.
  - Terrestrial partner needs to gain from involvement in the space programme.
    - Dual use a key advantage.
      - Currently the case for the MEMS accelerometer development but was not for the MEMS gyro

- MNT technologies are not yet mainstream for space.
  - Essential to provide full technical support through all stages of the programme/supply.
    - There will be anomalies during production and FMs.
    - There will be many user questions with a new technology.

- Careful teaming considerations necessary at the outset.

Conclusions

- MEMS technology is following on from CMOS imagers in providing a seed change in space sensor developments for miniaturisation.
- Mixed signal ASIC technologies are key to the next stage of miniaturisation in the majority of cases.
  - ITAR, obsolescence mitigation and reduced component/manufacture cost are considered key advantages.
- Interfaces and systems architectures will need to be addressed; this will be the next standout issue.
  - All options (including wireless) should be considered.
- There are additional challenges:
  - Best practice from significant preceding terrestrial development investment needs to be brought into space developments.
  - Partnering and long term engagement with terrestrial partners needs to be improved (dual use an obvious advantage).
  - Derivation at system level of “true requirements” can significantly affect the development effort (cost) required.