ESA Deep sub micron program
ST 65nm

ESA Workshop on Avionics Data, Control and Software Systems (ADCSS)
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European Space Agency

Agenda

- **Rad Hard library development**
- High speed serial link development
- Test vehicles

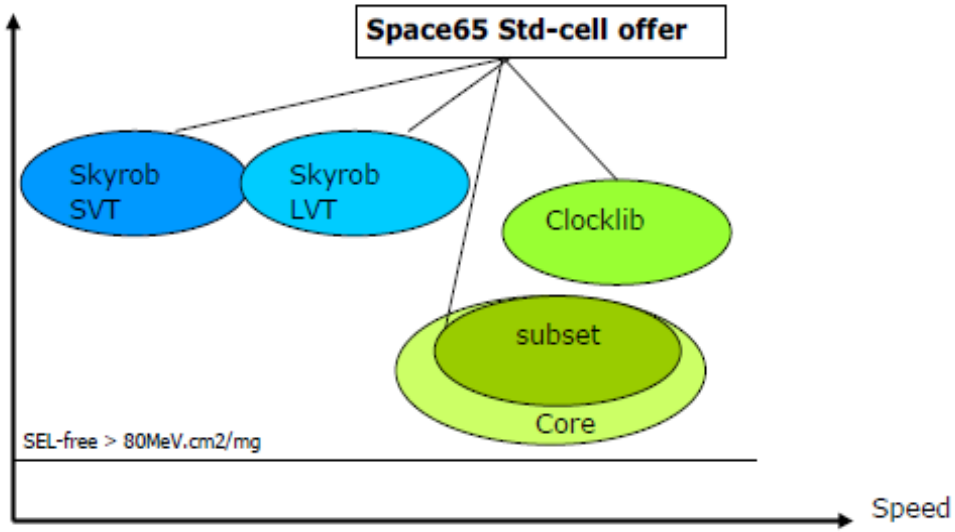
ST 65nm commercial process

- 65nm-LP CMOS from ST France : European technology, ITAR free
- 65nm CMOS commercially qualified in 2007
- 65nm CMOS Core Process :
  - Dual / Triple Gate Oxides
  - Dual / Triple Threshold Voltages for MOS Transistors
  - 7-9 Full Copper Dual Interconnect Levels
  - Low K

- performances:
  - 750 kgates/mm2
  - 2GHz stdcells
  - 5.7nW/(MHz x gates)
  - 1.25-7.5GBit/s HSSL modules

❖ ST Rad Hard offer based on CMOS 65nm-LP commercial process
❖ Reliability and Radiation maximisation performed at design stages

ST 65nm rad hard library



- **SKYROB65LPSVT** – radiation hardened library based on standard Vt transistors. SEU/SET improved by a factor ~ x100 compared to the commercial cells (CORE65LPSVT). Cells fully characterised under heavy ions during RADEF test campaign in December 2010. ST MAT20 (cells manufactured and characterised)
- **SKYROB65LPLVT** – duplication of the previous library with low Vt transistors (faster transistors). Library not yet characterised but expected to be as hard as SKYROB65LPSVT. Characterisation will be undertaken during year 2012 (Q2) under CNES LIBEVAL contract. ST MAT10 (cells designed but not yet characterised)
- **CLOCK65LPSVT** – Clock-tree cells of this library have been designed to limit the duty cycle distortions on clock trees; this library is ST MAT30, ready for mass production
- **CORE65LPSVT** – library offering a wide range of combinational and sequential cells for area/power optimisation, without specific radiation hardening; this library is ST MAT30, ready for mass production – only a subset of this library is proposed. The final cell list will be based upon results of characterization on extended reliability operating points

ST 65nm rad hard library

Technology	Std cells libraries	Total Cells-drives	Target
65 nm SPACE	CLOCK65LPSVT	110	Clock Network
	CORE65LPSVT	866	General purpose
	SKYROB65LPSVT	15 (DFF) 58 (Combinatorial)	Radiation Hardened
	SKYROB65LPLVT	15 (DFF) 58 (Combinatorial)	Radiation Hardened (Q2-2012)
	PRHS65	154	Place & route cells

- All cells latchup immune (characterised up 80Mev)
- Rad Hard cells, SEU rate enhanced by a factor ~ 100 compared to commercial cells
- Library cells ageing models extended from 10 years (commercial library) to 20 years (Space library)
- Ageing models sustaining temperature ranges from -40°C to +125°C Tj
  Extreme corners simulations supported:
  MAX (125°C Tj/Process Slow/Voltage MIN/20 year ageing)
  MIN (-40°C Tj/Process Fast/Voltage MAX/0 year ageing)
- -55°C characterisations have been carried out under CNES contract LIBEVAL
- Library fully compatible with standards flows based on Synopsys or Cadence

ST 65nm rad hard library
Hardened DFF characterisation

"SEU rate improvement factor with SKYROB ranging from 80 to 500"

	Cell type	library	Upset rate in GEO (SEU/bit/day)	Improvement factor compared to standard commercial DFF		description
				best	worst	
	Standard DFF from CORELIB with latchup protection (DNW)	CORE65LPSVT (Standard Vt = Slow)	1.6E-7 (best)	x	x	Reference DFF (commercial lib - CORELIB)
	Standard DFF from CORELIB with latchup protection (DNW)	CORE65LPLVT (Low Vt = fast)	4.1E-7 (worst)	x	x	Reference DFF (commercial lib - CORELIB)
✓	SKYROB65_LSDGURFD 12_DFPQX6	SKYROB65LPSVT (Standard Vt)	0.812E-9	197	**504**	Harden DFF with drive 6. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
	SKYROB65_LSDVURDF 12_DFPQX3	SKYROB65LPSVT (Standard Vt)	0.896E-9	178	457	Harden DFF with drive 3. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
✓	SKYROB_LSDGFD12S_ SDFPRQTX10	SKYROB65LPSVT (Standard Vt)	1.23E-9	130	333	Harden DFF with drive 10. Scan-out D flip-flop with 1 phase positive edge clock, reset active low, Q and TQ outputs
	SKYROB_LSDVFD12V_ DFPQX9	SKYROB65LPSVT (Standard Vt)	1.45E-9	110	282	Harden DFF with drive 9. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
✓	SKYROB_LSDGFD12S_ DFPQX18	SKYROB65LPSVT (Standard Vt)	1.82 E-9	87	225	Harden DFF with drive 18. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
	SKYROB_LSDGFD12DP _DFPQX10	SKYROB65LPSVT (Standard Vt)	1.98E-9	**81**	207	Harden DFF with drive 10. D-type flip-flop with 1 phase positive edge triggered clock, Q output only

✓ Cells selected to be integrated in the final offer

Data computed with tool web based CREME96

- GEO orbit @ solar quiet
- Shielding 100mils Aluminium
- ions up to element Z=92
- Weibull fit from experimental results at RADEF (December 2010)

ST 65nm rad hard library
Hardened DFF versus commercial DFF

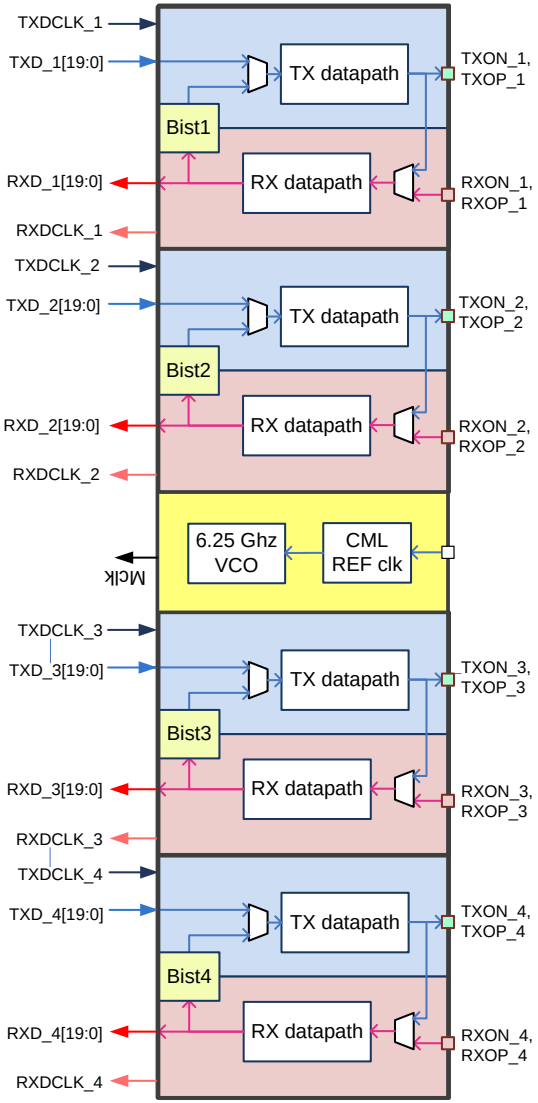
	CORELIB Commercial library (reference)	SKYROB (Ultra Robust – Slow - SVT) characterised in Q4-2010	SKYROB (Robust – Fast - LVT) characterised in Q2-2012
SEU rate SEU/bit/day (Geo) shielding 100mils Al	1.6E-7 (best)	1.23E-9 x130	1.8E-9 x90
Timing Set-up + delay (ps)	536	636 ~ 20% slower	536 As fast
Area (um^2)	13	26 x2.0	23 x1.8
Energy (pJ)	2.05	4 x2.0	3.8 x1.8

Comparison with a DFFX10 cell from commercial library (CORELIB)

Agenda

- Rad Hard library development
- **High speed serial link development**
- Test vehicles

HSSL IP = 4 data slices + one clock slice



Note: data slice = Tx lane + Rx lane

European Space Agency

HSSL general features

- ✓ Independent TX and RX lanes throughput of 6.25 Gbps, 3.125 Gbps or 1.5625 Gbps
- ✓ BER < 10^{-14} (in terrestrial conditions)
- ✓ Independent global and per link TX & RX power downs
- ✓ Tx (or Rx) link aggregation is possible but requires external control logic for lane control and sync pattern encoding/decoding
- ✓ Programmable through a control bus.
- ✓ Single 1.2V power supply
- ✓ HSSL is a CML serial communication PHY
- ✓ SPACEFIBER codec compliant
- ✓ HSSL will be delivered as an IP part of ST 65nm Rad Hard offer
- ✓ HSSL will be provided as a Flip chip ready layout IP (hard macro)

- ✓ Rad hardening targets:
  - ✓ Minimize BER sensitivity under Heavy Ions
  - ✓ No Single Event Functional Interrupts (SEFIs):
    - ✓ Self recovery of Single Event Transients (SETs) and Single Event Upsets (SEUs) in the signal processing path
    - ✓ TMR protection on configuration registers
  - ✓ Full immunity to Single Event Latch-up (SEL) failures for the IP and the whole Test Vehicle versus Heavy Ions with a LET up to 80MeVcm2/mg, at 125°C Tj and maximum voltage supplies values

Clock slice & TX features

Clock slice:

- ✓ Very stable internal clock based on LC VCO frequency synthesizer
- ✓ 156.25 MHZ CML AC coupled external differential reference clock

TX data lane:

- ✓ Output: Differential CML signaling with programmable bit polarity and order inversion
- ✓ Programmable output amplitude
- ✓ Programmable 100 ohms differential terminations
- ✓ 4 tap programmable pre-emphasis (1 precursor, 3 post-cursor)
- ✓ Support up to ± 100ppm data rate offset versus reference clock frequency (plesiochronous mode)
- ✓ Programmable input word width: 20, 10 and 5 bit

RX features

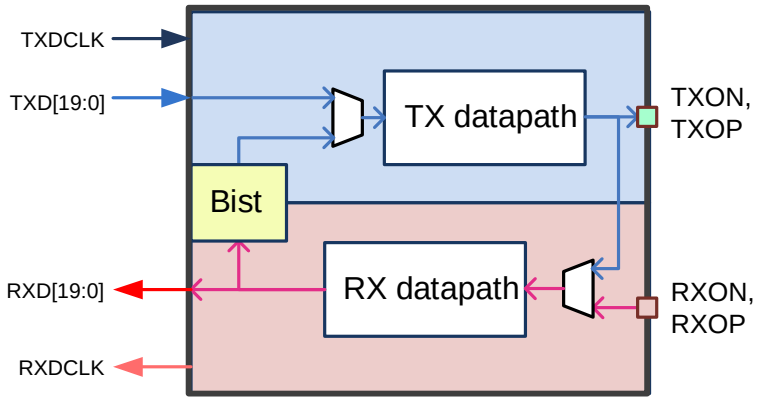
RX data lane:

- ✓ Input: RX Differential CML signaling with programmable bit polarity and order inversion
- ✓ Programmable 100 ohms differential terminations
- ✓ 4 tap adaptive Decision Feedback Equalizer (DFE)
- ✓ Linear Equalizer and gain control with up to 15 dB equalization at Nyquist frequency
- ✓ Programmable output word width: 20, 10 and 5
- ✓ Separate sampler for eye mapping & extraction of ISI coefficients for equalizer adaptation
- ✓ Signal loss detection circuitry based on signal amplitude, transition density, and eye opening
- ✓ Independently configurable per link multi-rate digital RX Clock & Data Recovery (CDR)
- ✓ Support up to ± 100ppm data rate offset versus reference clock frequency (plesiochronous mode)

TX & RX characteristics

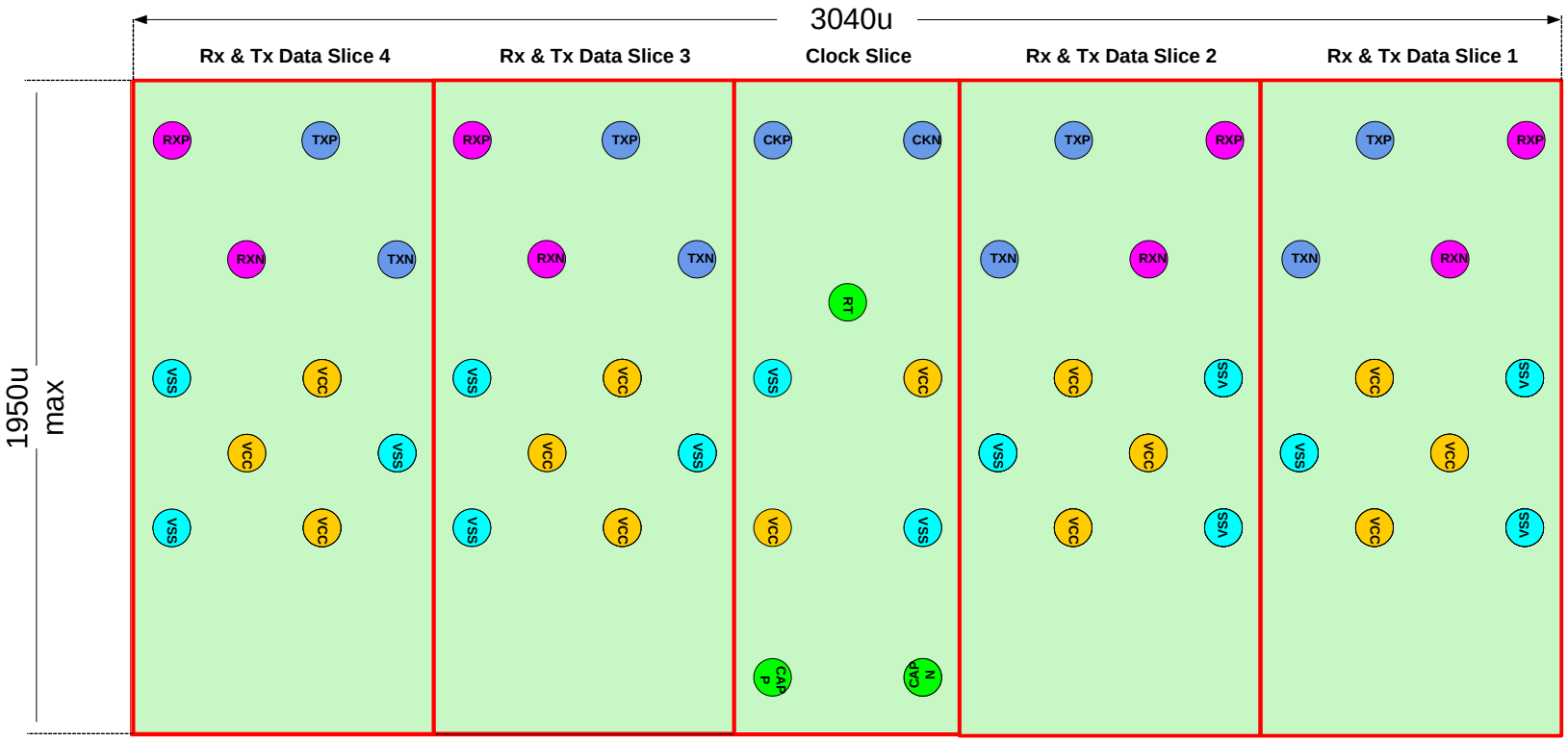
	Symbol	Parameter	Min	Typ	Max	Unit	Notes
TX	V_{OCM}	Output Common Mode Voltage	800	1000	1200	mV	DC coupled, all terminations to 1.2V
			N.A.				AC coupled
	V_{OD}	Output peak Differential Voltage		300	600	mV	AC or DC coupled.
	Z_{OD}	Differential Output Impedance	90		110	ohm	Not including S_{22} effects > 1 GHz.
	Z_{OCM1}	Common Mode OP Impedance	24	28	32	ohm	Common Mode Term. sw. closed
RX	V_{ICM}	Input Common Mode Voltage	700	1.0	AVCC	mV	Internally compensated
			N.A.				AC coupled
	V_{ID}	Input Peak Differential Voltage	62.5		600	mV	AC or DC coupled
	Z_{ID}	Differential Input Impedance	93		107	ohm	At frequencies < 1 GHz. With proper trim setting.
	Z_{ICM1}	Common Mode Input Impedance	24	28	32	ohm	Termination sw. closed

HSSL data slice internal test capabilities



- ✓ TX -> RX full speed serial loop-back
- ✓ TX –> RX and RX –> TX parallel loop-back
- ✓ Five standard PRBS patterns unit with separate generation and detection
- ✓ Programmable fixed pattern generation
- ✓ Jitter generation and BER measurement
- ✓ Programmable RX sampling position within the data eye
- ✓ IEEE 1149.1 (DC) and 1149.6 (AC) JTAG boundary scan support

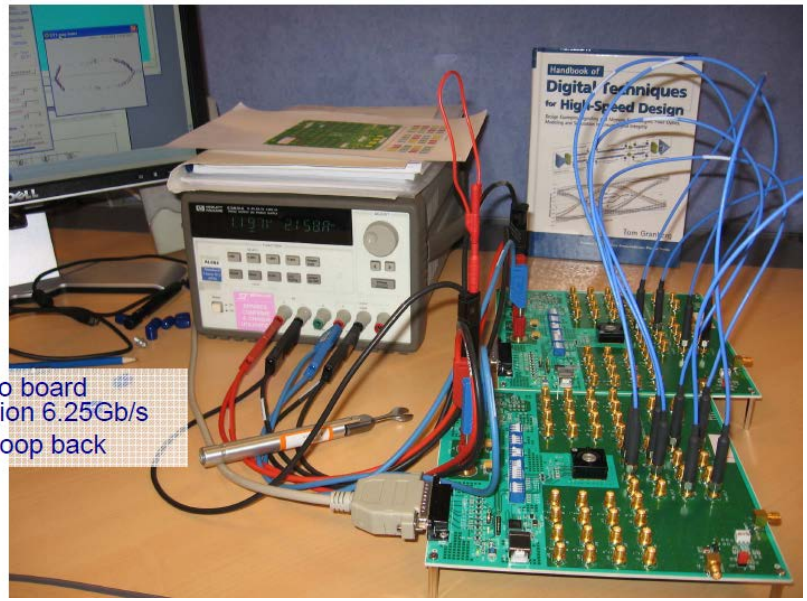
HSSL top layout view (preliminary data)



Agenda

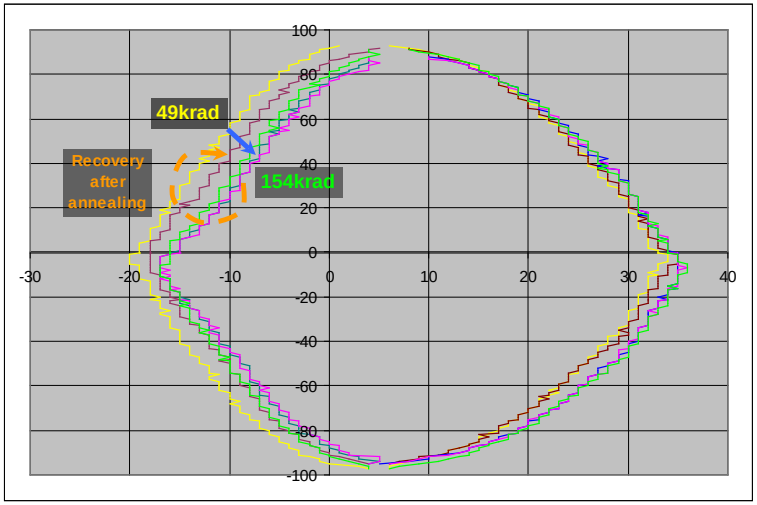
- Rad Hard library development
- High speed serial link development
- **Test vehicles**

High speed serial link characterisation on Quatuor test vehicle

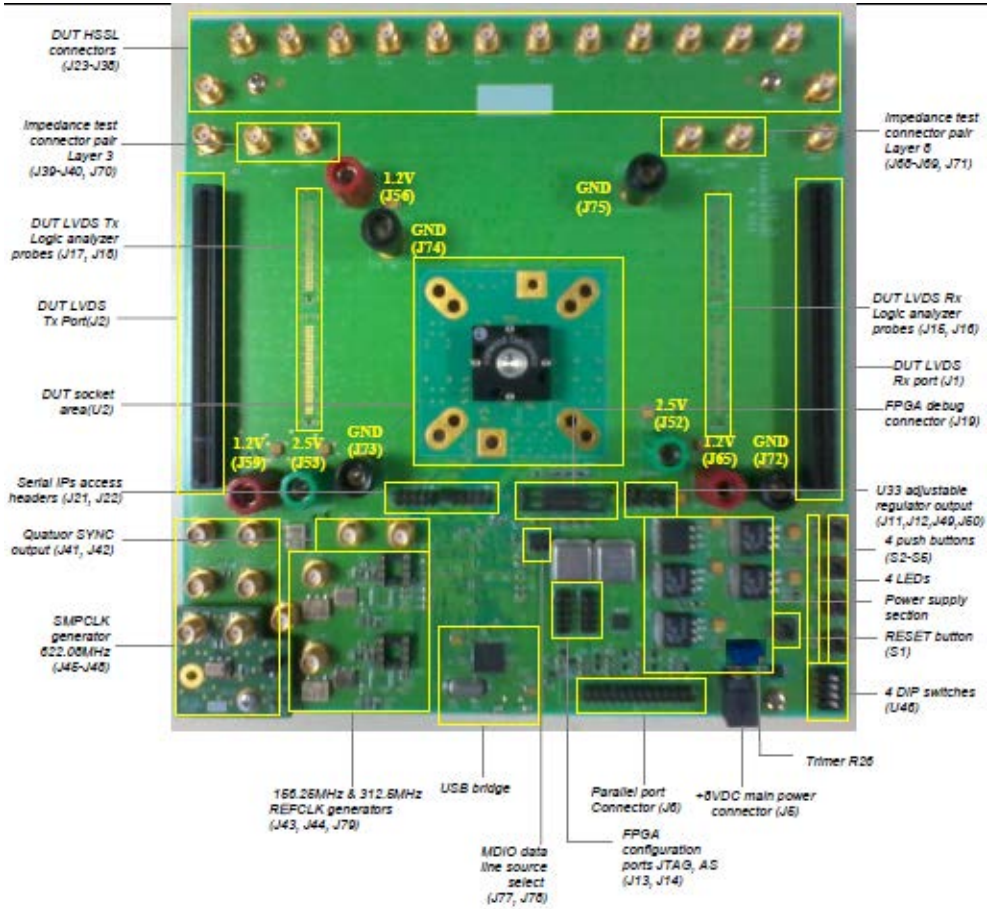


Board to board
Communication 6.25Gb/s
Remote loop back

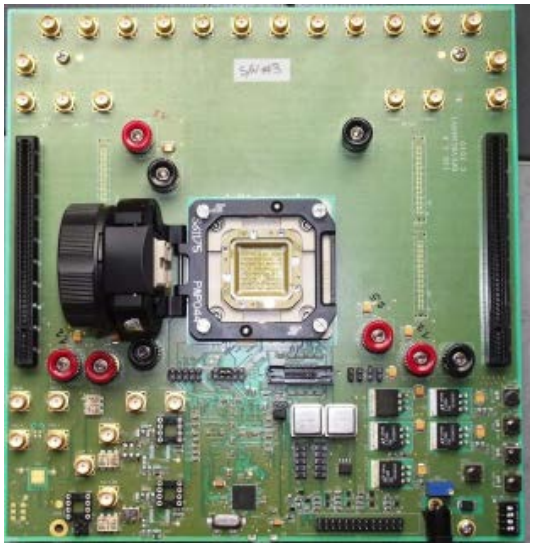
Receiver eye diagram opening
TID test campaign performed at
ENEA December 2009
Device fully operational at 200 Krads
+
heavy ions test campaign performed at
RADEF December 2010
(ESCC 25100 guidelines)



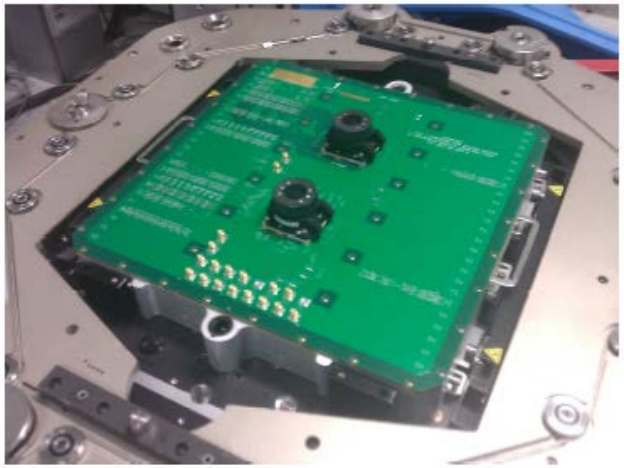
High speed serial link validation boards



Quatuor electric characterisation board



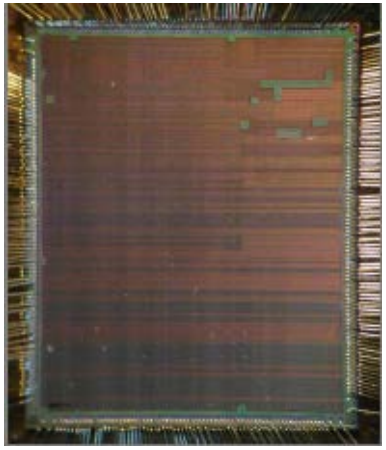
Quatuor radiation & reliability characterisation board



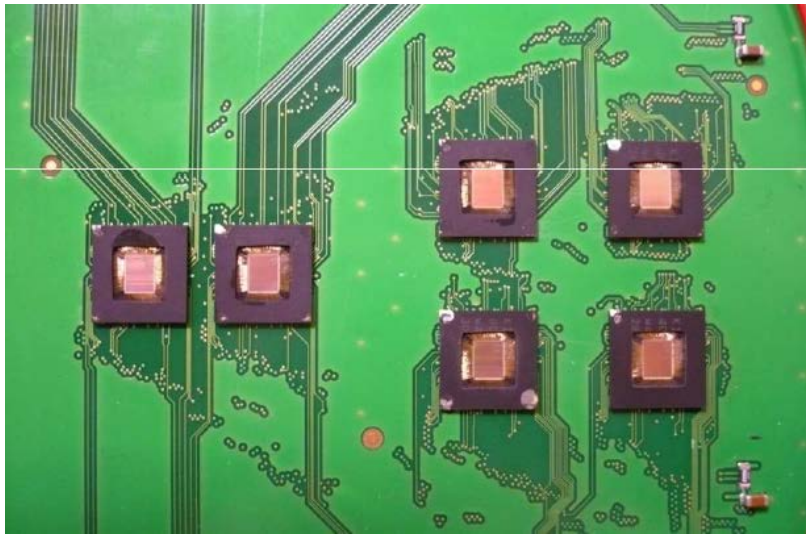
Quatuor automated test equipment board (ATE)
ST Integraflex tester

ST 65nm rad hard library radiation validation board

"Key IP SAT" 1.0 layout (KIPSAT)



KIPSAT 1.0 die (~ 24 mm^2)



KIPSAT radiation test board
heavy ions test campaign RADEF December 2010

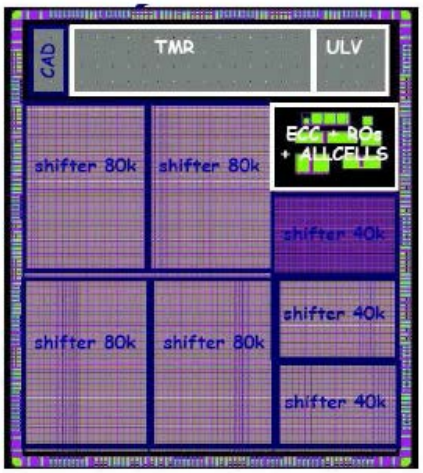
KIPSAT 1.0 main features

- 7 shift registers (40k and 80k DFFs)
- 4 ECC SRAMs with different MUX ratio (4, 8, 16)
- 1 TMR shift register (120k DFFs)
- 1 CAD modelling block (library silicon correlation)

ST 65nm test vehicles already characterised ESA-CNES contracts

TC1 (rad hard library - KIPSAT1.0):

- all cells from SKYROB lib (slow - Rad Hard) ~ 73 cells
- all cells from CORROB lib (fast - Rad Tol) ~ 73 cells
- commercial flip flop + TMR
- hardened flip flop (but no TMR)
- SRAM + ECC
- 7 ring oscillators to characterise the process

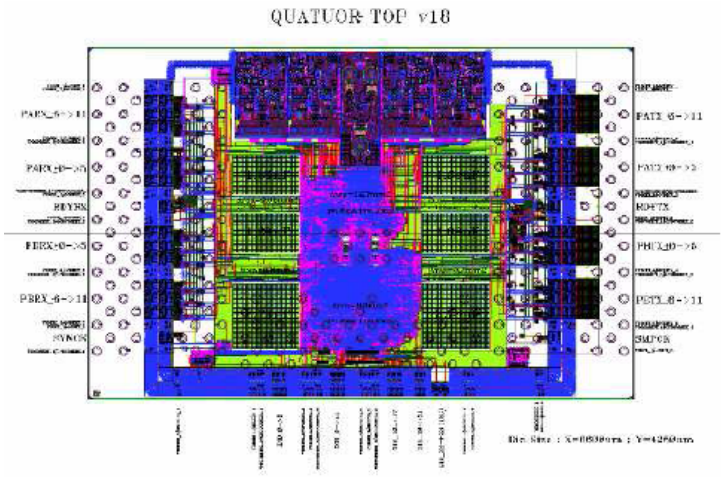


TC2 (PLL 1st type):

- high performance multiphase PLL covering frequency range from 50MHz … 1.2 GHz (6 phases)
- special IOs
  - cold spare CMOS
  - cold spare LVDS
  - SSTL
  - I2C

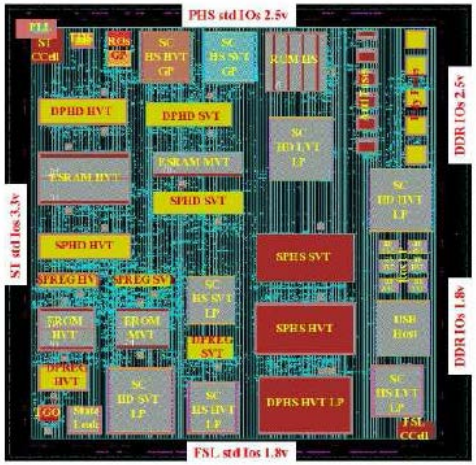
TC3 (high speed serial link / HSSL):

- Quatuor / 4 x 6.25 Gbps



TC4 (commercial library - CORELIB):

- commercial library full set (~ 1000 cells)



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THANK YOU ☺