XentiumDARE IC
DSP SoC Demonstration ASIC

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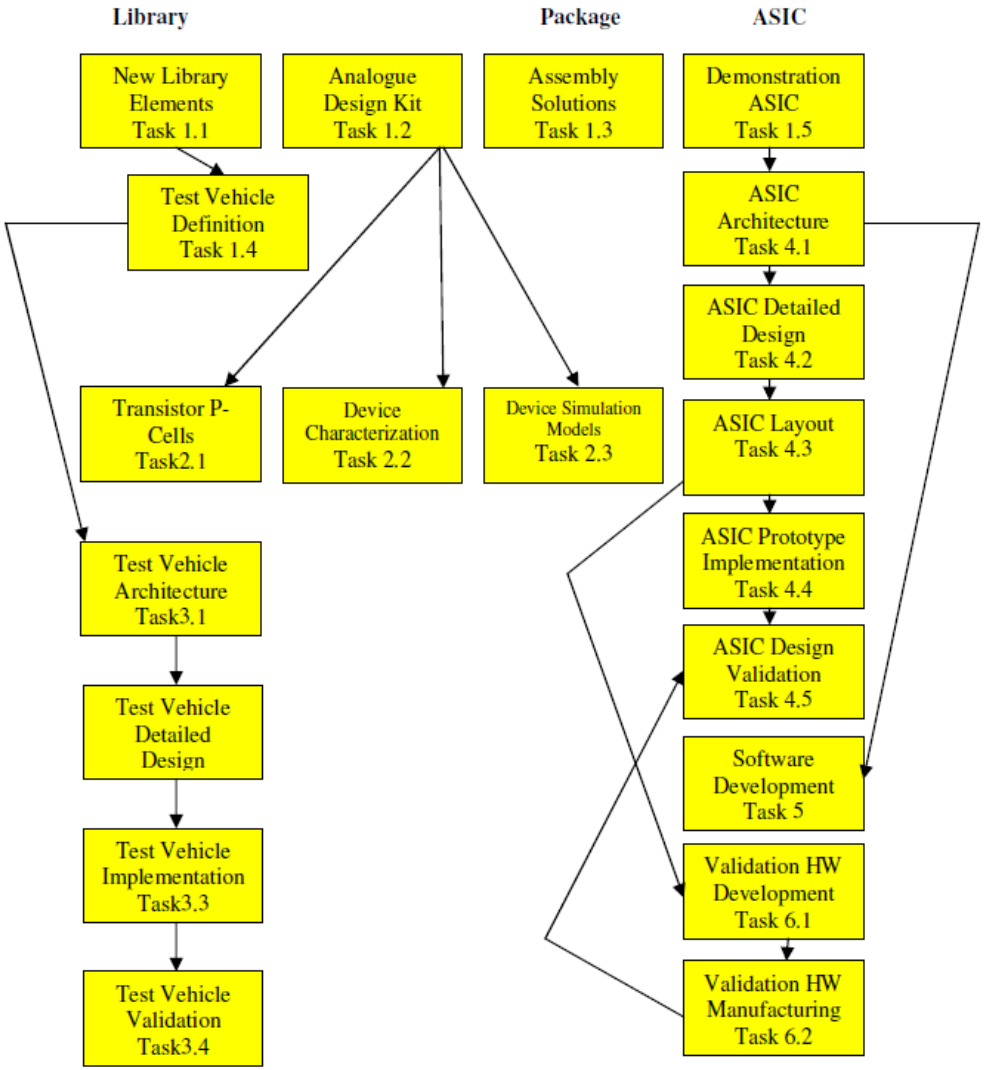
Objectives

- Demonstrate implementation of IP building blocks multicore DSP for payload processing in DARE180 technology

- Context: DSP for payload processing
- ESA TRP activity
  - MPPB
    - Feasibility/benchmark study for next generation multi-core DSP for space applications (Jan ‘09 – Aug ‘12)
- ESA CTP activity
  - SSDP
    - Scalable Sensor Data Processor (2014-)
    - Multicore DSP for Juice deep space mission

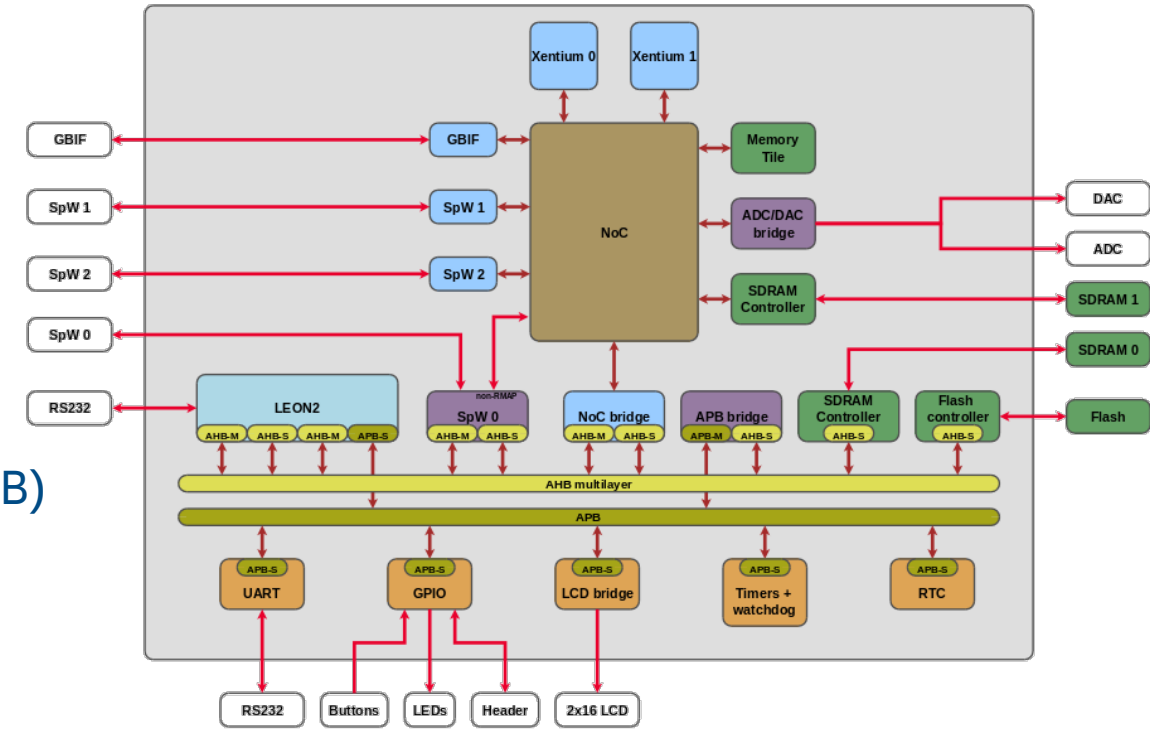
Activities

- SoC Design & Verification
- FPGA-based verification
- IC manufacturing
- Validation
- Benchmarking
- Irradiation testing



MPPB architecture Multicore DSP

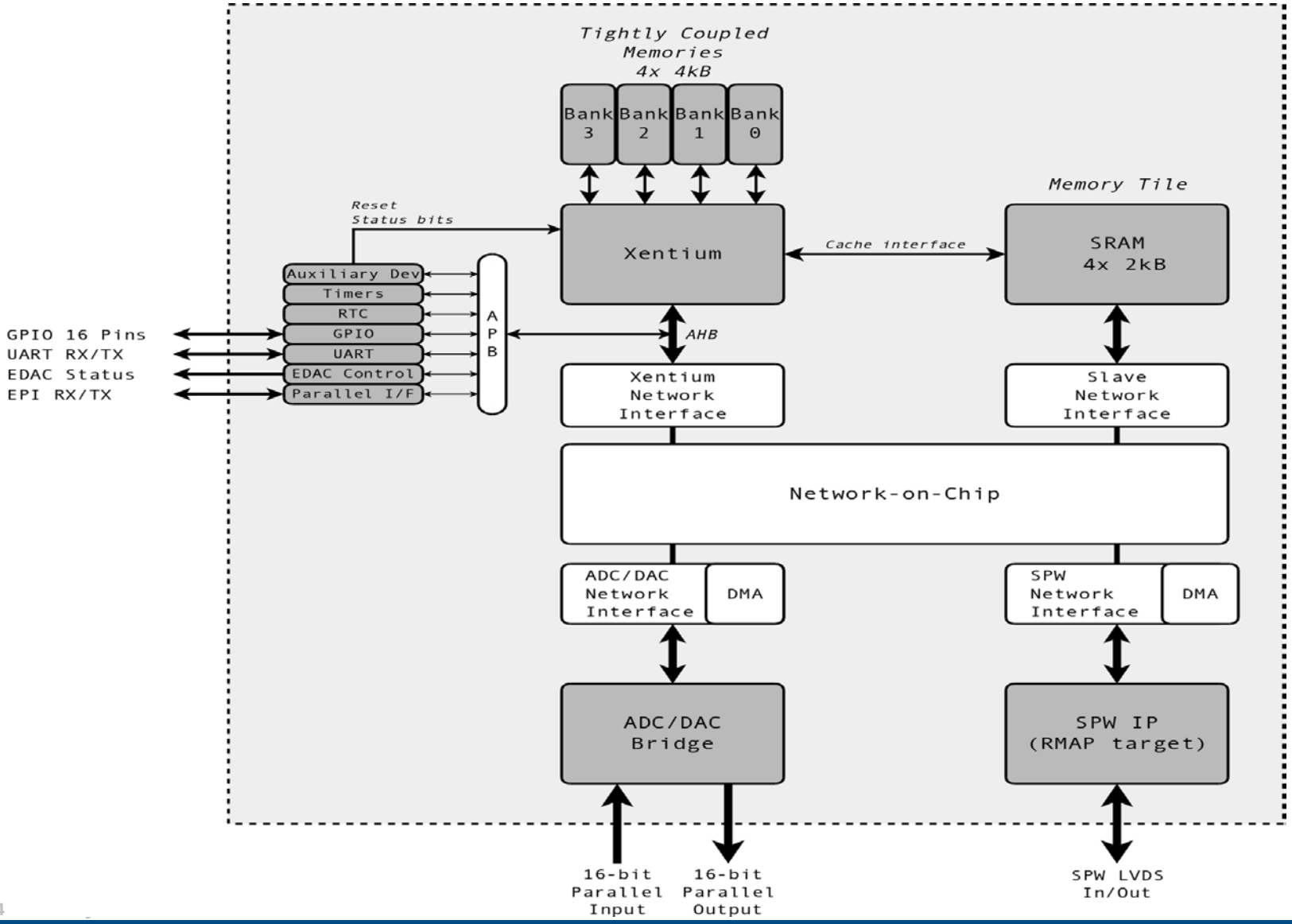
- Xentium-based DSP subsystem
  - Network-on-Chip (NoC)
  - 2 Xentium DSP core
  - Memory Tile
  - DMA controller
  - High speed interfaces
  - ADC/DAC interfaces
  - DDR
- Leon-based GPP subsystem
  - AMBA Bus system (AHB/APB)
  - SpW RMAP
  - DDR, Flash
  - Standard peripherals



XentiumDARE Overview

- Scaled-down MPPB DSP subsystem
- Rad. hardened in DARE180
- Fully operational and programmable system-on-chip (SoC)
- Key building blocks from MPPB DSP subsystem
  - Xentium DSP Core
  - I + D memories, memory tile
  - NoC and NoC bridges to extern ADC/DAC
  - SpW RMAP IF (STAR-Dundee)
  - UART, GPIO, Timers, EDAC control,…
- Die size: 5x10 mm2 – 2 seats on MPW

XentiumDARE Architecture



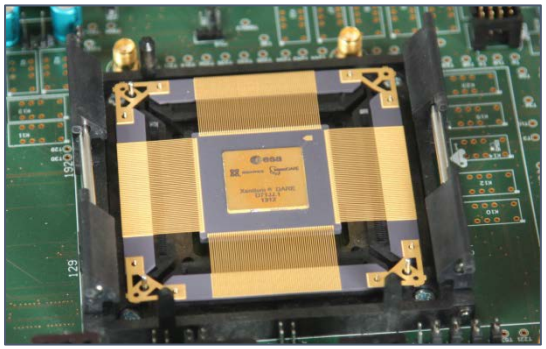
XentiumDARE IC
Radiation Hardening Strategy

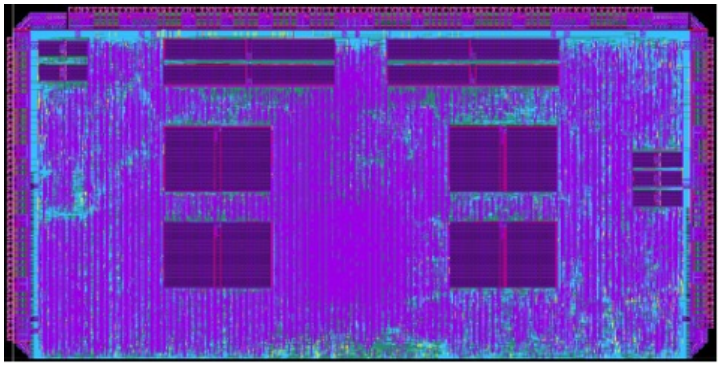
Mitigation Techniques	Design level	Radiation Effects						
		TID	SEL	SEU	SBU	SMU	SET	SEFI
Hardening by design (DARE)	Process	X	X	X			X	
HIT flip-flops (DARE)	Process			X				
Reset tree hardening	Layout			X			X	
SRAM bit interleaving	Layout					X		
EDAC	System				X	X		
Watchdog	System							X

- EDAC protected SRAM access
  - FIFOs - SEC-DED (39,7)
  - Instruction cache - SEC-DED (39,7)
  - Data banks – SEC (12,4)

XentiumDARE IC

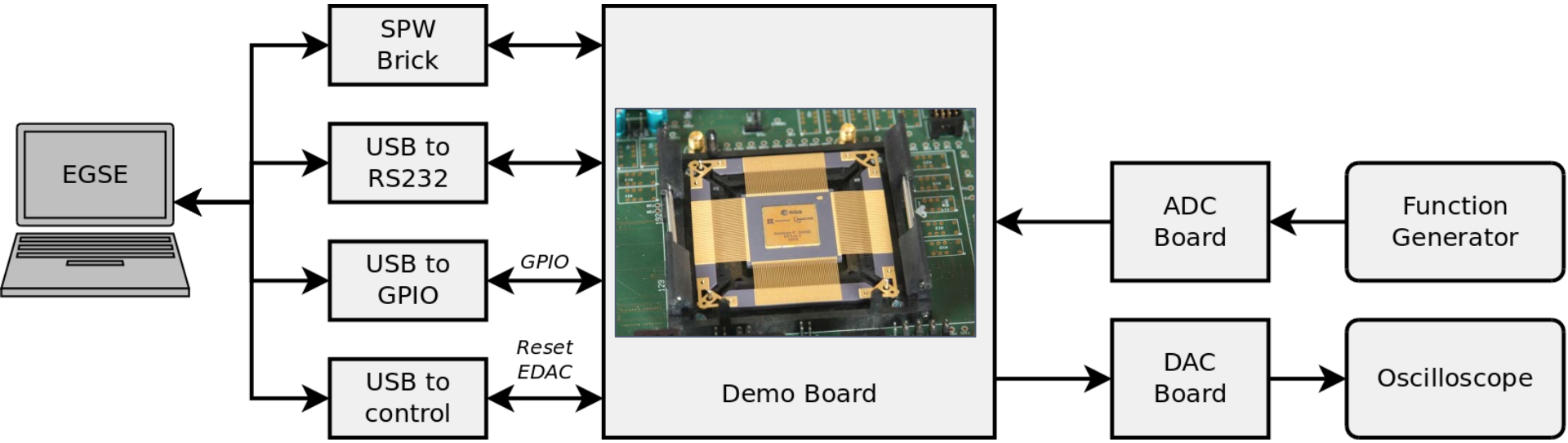
- Die size: 5x10 mm2 – 2 seats on MPW
- IO and power rings on 3 sides only to save area
- Kyocera full-custom CQFP 256-pin package
- DARE180nm technology – 5.1 beta
- Memory (SRAM):
  - 8kB I-cache / memory
  - 4 x 4kB data banks
  - 4 x 128B
- External clocks:
  - System: up-to 100MHz (80MHz WCMIL)
  - SpW: 200MHz
- Critical timing in single-cycle SRAM access
  - 100MHz target pushed for future projects
  - DARE180 improvements on-going in DARE+ project
  - No area available for speed trade-off on EDAC





XentiumDARE Validation Setup

- Functional testing
  - ESA NGDSP benchmarks
- Radiation testing
  - TID
  - SEE - SEU / SET



Benchmark Environment

Benchmarks Introduction

- Subset of “Next Generation Space DSP Software benchmarks”
- Implemented 4 of 5 benchmarks
  - Benchmark 1: I/O Performance
  - Benchmark 2: Analog acquisition, processing and output
  - Benchmark 4: Onboard Data Processing Case 1
  - Benchmark 5: Onboard Data Processing Case 2
- Operating conditions
  - System frequency: 50 MHz
    - Reduced due to IR-drop on validation board
  - SpaceWire frequency: 200 MHz (transmit clock)
  - Board power supply voltage: 1.95 V
- Numbers presented at ESA DSP Day 2014
  - Less than 1 watt power consumption (at 50 MHz)
- XentiumDARE IC fully operational and programmable SoC

Lessons learned

- Radiation hardening by design effective with DARE180 flow
- Do not use test board as validation / demo board
- Predicable convergence is difficult when technology libraries and SRAMs improvements are on-going
- Further speed vs area trade-off analysis / investigations needed for single-cycle memory access (EDAC + SRAMs).

Summary

- Successfully demonstrated
  - Rad. Hardened Xentium DSP IP & NoC IP using DARE180 technology and flow
- Tested DARE180 library and SRAM improvements
  - DARE180 - 5.1 beta
    - new cells and pads including clock gating cells
  - Single and dual port SRAMs
- Next Generation DSP benchmarks numbers available for most benchmarks; including power numbers
- Improvements and experiences applicable to Scalable Sensor Data Processor (SSDP) project

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