DARE+ - ASICS FOR EXTREMELY RAD HARD & HARSH ENVIRONMENTS

FINAL PRESENTATION

9/12/2014

(4000104087/11/NL/AF)

imec

AGENDA

Project overview and objectives

Device Characterization and Analog Design Kit

Library Elements

Application ASIC

Lessons Learned and Conclusions

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OVERVIEW/OBJECTIVES HISTORY DARE

DARE+ is a continuation of previous ESA contracts for library development for rad-hard library design using UMC 0.18µm technology

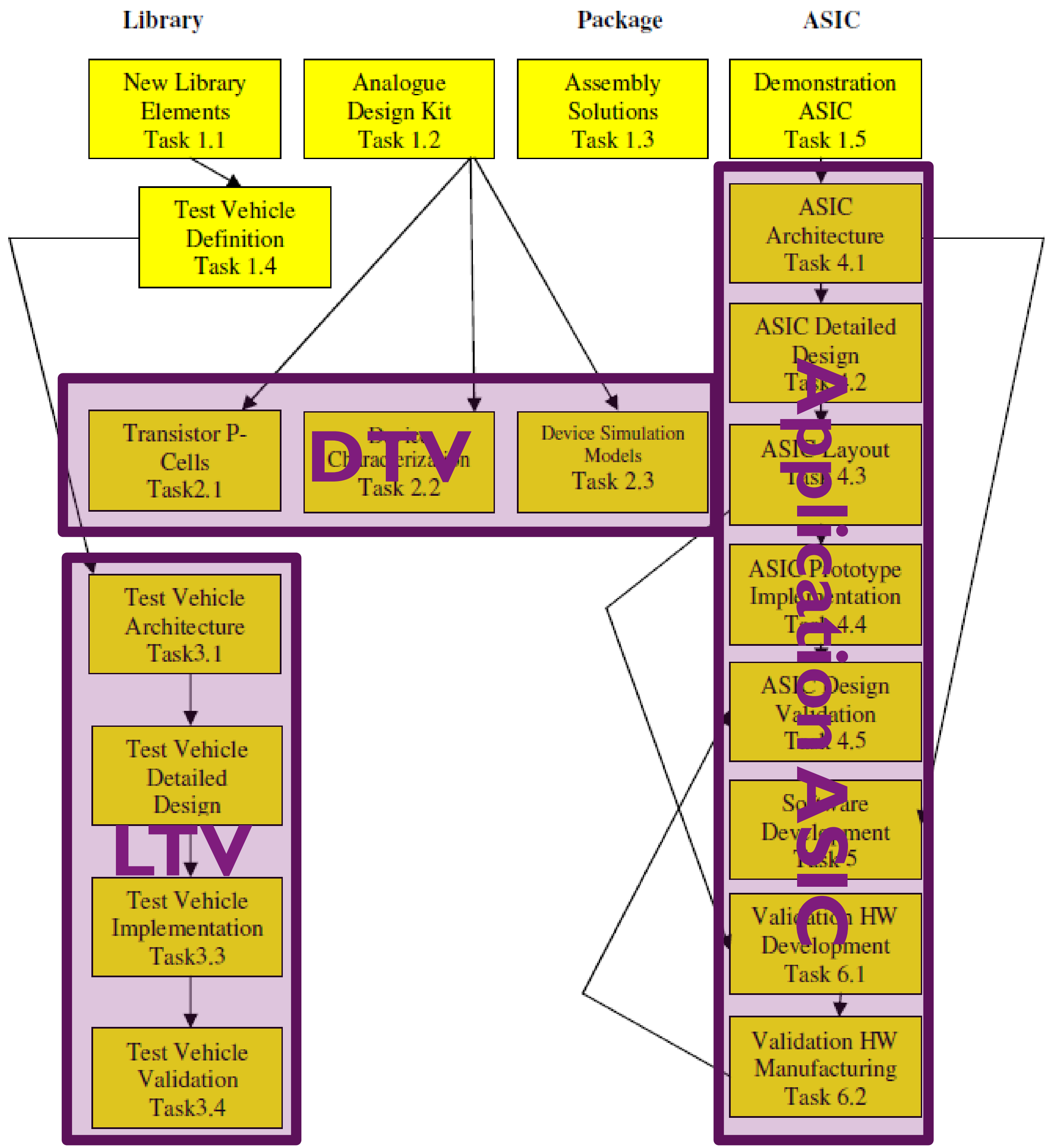
- Proof of concept (RHBD1, 14177/99/NL/FM)
- NSGU, Main Library Development (RHBD2, 14932/00/NL/DS)
- Radiation Hardening by Design (RHBD3, 15852/01/NL/FM)
- ASICs for Space, Fabricated with RHBD Library (LEONDARE, 19916/06/NL/JK)

OVERVIEW/OBJECTIVES
OBJECTIVES

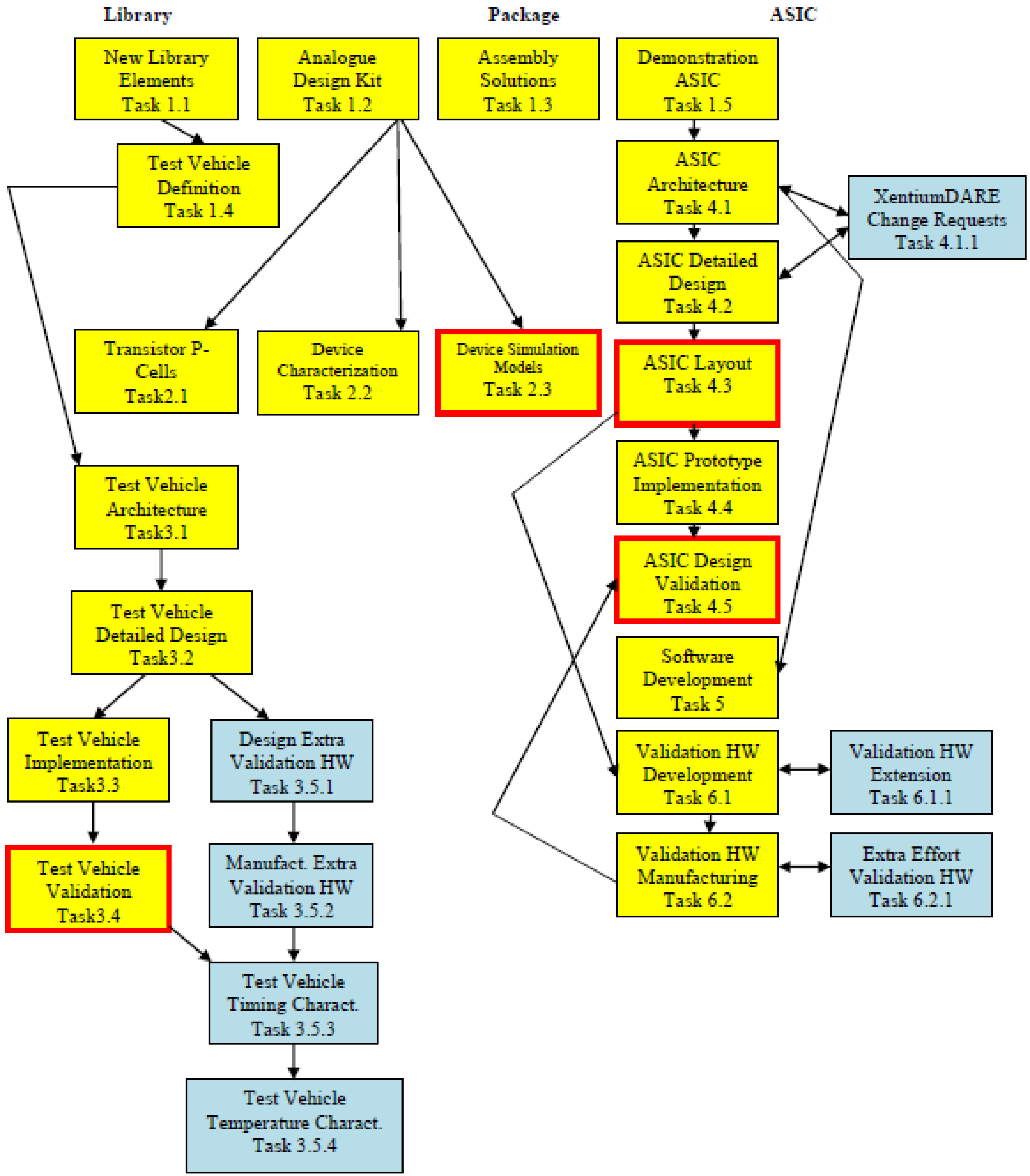
This activity's objective is to provide a suitable and mixed-signal capable microelectronic technology with a well-established IP library for platform and payload elements of spacecrafts on JUICE and other missions. At the same time the maturity of the existing DARE 180nm platform will be increased and further demonstrated for applications in very harsh radiation environments up to 1 Mrad(Si).

Two test vehicles and an application chip will be designed and tested to reach the goal. The first test chip is to characterize the devices of the technology. The second test chip is to test the library elements. The objective of the Application ASIC is to demonstrate the implementation of basic reconfigurable building blocks for payload processing in DARE180 technology

OVERVIEW/OB
OVERVIEW



OVERVIEW/OE
OVERVIEW



OVERVIEW/OBJECTIVES OVERVIEW

Contributors

- imec
- Recore Systems
- Microtest s.r.l.
- Cyclotron Resource Centre at Louvain-la-Neuve
- Co60 at ESTEC

ESA overview/guidance/support

- Boris Glass
- Richard Jansen
- Roland Trautner

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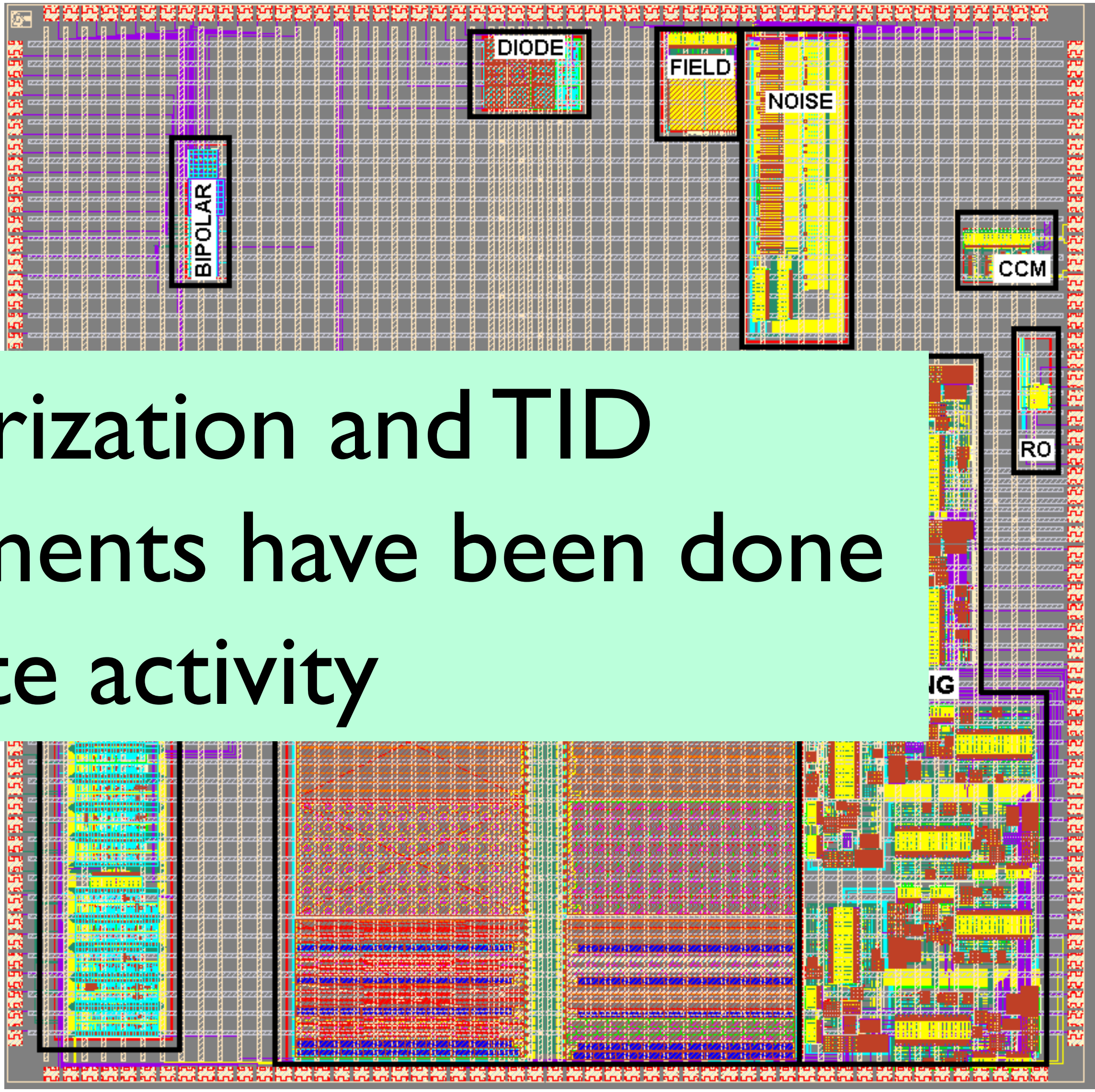
DTV AND ADK STRUCTURES OVERVIEW

- IV
- CV
- Matching
- Dio
- RO
- CC
- No
- Fiel

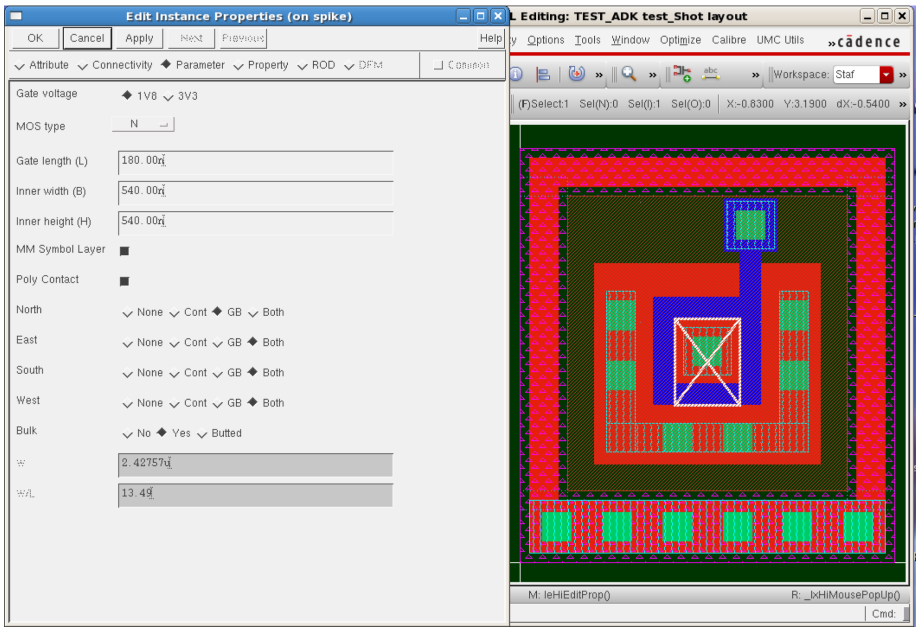


Characterization and TID measurements have been done in separate activity

ADK
SEPTEMBER 2011

ADK = Analog Development Kit

Layout/schema pcell Cadence Virtuoso IC5 and IC6



LVS/PEX deck

ADK
APRIL 2012

Bug fixes

Added symbol, spectre and auCdl view to ELT pcell

Compute w of ELT transistor is now rounded to nearest nm.

Deprecated IC5 support

ADK
DECEMBER 2014

(Intermediate alpha releases done used in other activities)

- Rem
- V2 o regic layou
- Rad
- Impr trans avail

- Poly crosses P+diffusion guard
- Nmos gate NOT enclosed
- 1.8V Leaky STRAIGHT N+diffusion regions
- 3.3V Leaky STRAIGHT N+diffusion regions
- 1.8V Leaky ELT N+diffusion regions
- 3.3V Leaky ELT N+diffusion regions
- Leaky Nwell-N+diffusion regions
- Leaky Nwell-Nwell regions

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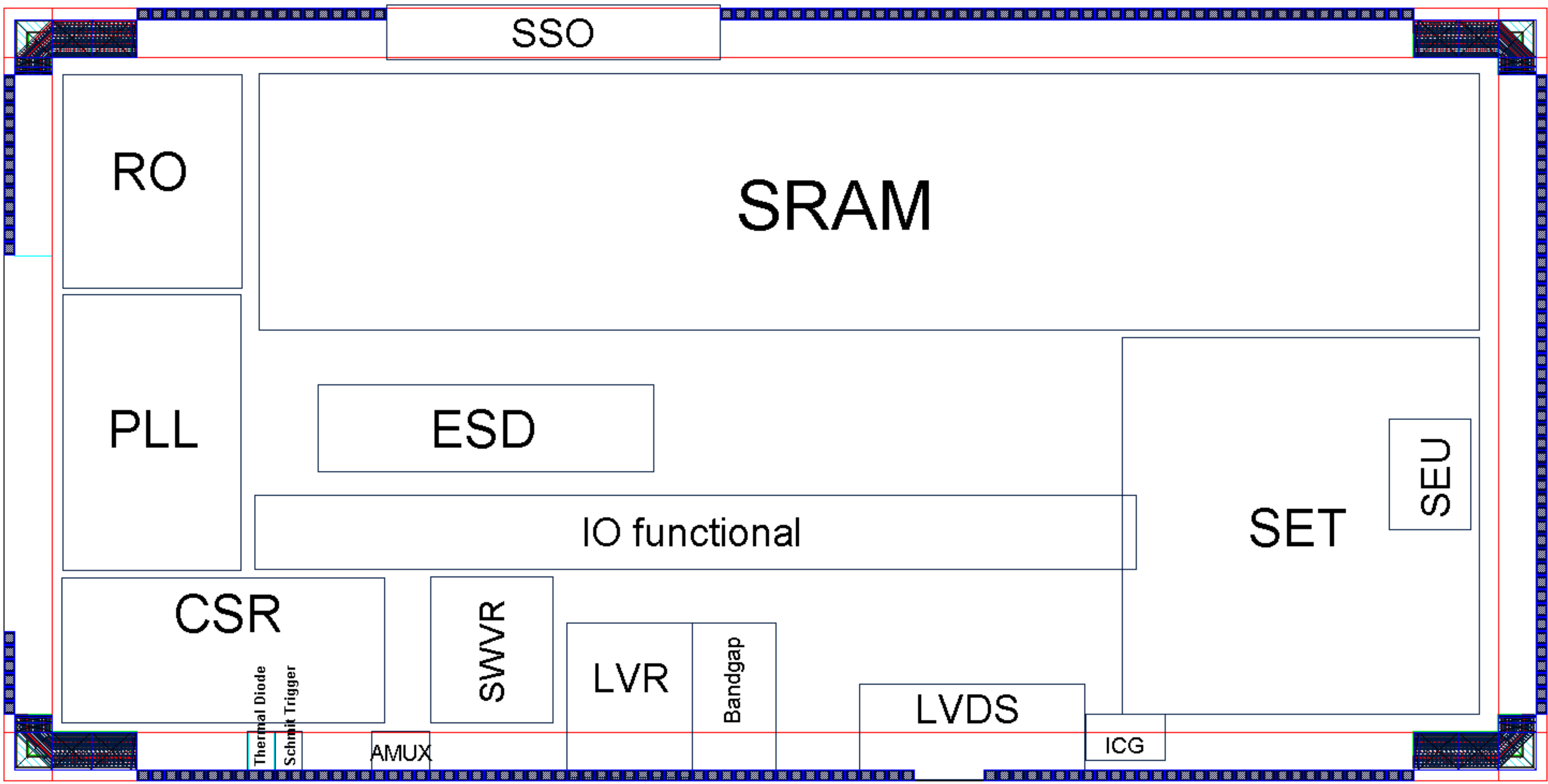
LIBRARY ELEMENTS
STRUCTURES OVERVIEW



LIBRARY ELEMENTS

Single port compiler

Parameter	Minimum	Typical	Maximum	Unit
Junction Temperature	-55	27	145	°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	bits
Word Count	32	-	8192	words
Word Length	8	-	256	bits
Write Mask Granularity	8	-	-	bits
Operating Frequency	-	-	200	MHz

Dual port compiler

Parameter	Minimum	Typical	Maximum	Unit
Junction Temperature	-55	27	145	°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	Bits
Word Count	32	-	8192	Words
Word Length	8	-	256	Bits
Write Mask Granularity	8	-	-	bits
Operating Frequency	-	-	>100	MHz

LIBRARY ELEMENTS TEST OVERVIEW

Test structure	SEL	Functional	SEU	SET	TID		Temp
					Leakage	Functional	
XICG cells	X	X				X	
LVDS with ECM	X	X				X	
I/O cells							
SSO	X	X				X	
Schmitt triggers	X	X					
ESD structures							
SRAM memory blocks	X	X	X		X	X	X
SRAM subcells	X	X			X	X	
PLL	X	X		X			
Linear voltage regulator	X	X		X		X	
Bandgaps	X	X			X	X	X
Switched voltage regulator	X	X				X	
Analog multiplexer	X	X					
Ring oscillators	X	X			X	X	
SEU test structures	X	X	X				
Countermeasures shift-registers	X	X			X	X	
SET test structures	X	X		X			

LIBRARY ELEMENTS TEST OVERVIEW

Test structure	SEL	Functional	SEU	SET	TID		Temp
					Leakage	Functional	
XICG cells	X	X				X	
LVDS with ECM	X	X				X	
I/O cells		Available @imec for debug purposes					
SSO	X	X				X	
Schmitt triggers	X	X					
ESD structures		Available @imec for debug purposes					
	X	X	X		X	X	X
	X	X			X	X	
	X	X		X			
Linear voltage regulator	X	X		X		X	
Bandgaps	X	X			X	X	X
Switched voltage regulator	X	X				X	
Analog multiplexer	X	X					
Ring oscillators	X	X			X	X	
SEU test structures	X	X	X				
Countermeasures shift-registers	X	X			X	X	
SET test structures	X	X		X			

ESD specs are verified in other activities

LIBRARY ELEMENTS TEST OVERVIEW

Test structure	SEL	Functional	SEU	SET	TID		Temp
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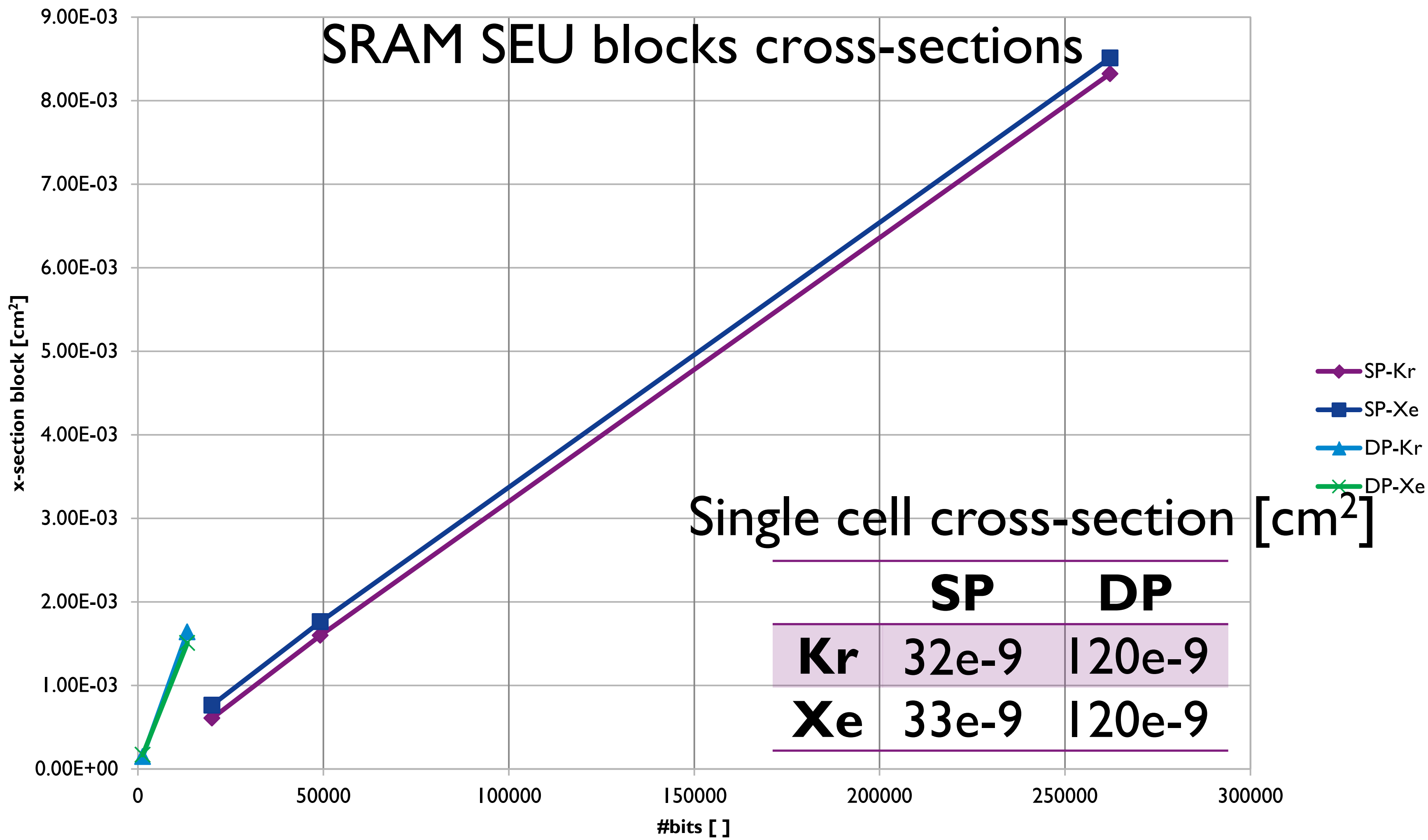
XICG cells	X	X				X	
LVDS with ECM	X	X				X	
I/O cells		Available @imec for debug purposes					
SSO	X	X				X	
Schmitt triggers	X	X					
ESD structures		Available @imec for debug purposes					
SRAM memory blocks	X	X	X		X	X	X
SRAM subcells	X	X			X	X	
PLL	X	X		X			
Linear voltage regulator	X	X		X		X	
Bandgaps	X	X			X	X	X
Switched voltage regulator	X	X				X	
Analog multiplexer	X	X					
Ring oscillators	X	X			X	X	
SEU test structures	X	X	X				
Countermeasures shift-registers	X	X			X	X	
SET test structures	X	X		X			

LIBRARY ELEMENTS TEST OVERVIEW

SSO are in spec but not easy to relate to simulation due to indirect measurement procedure

Test structure					TID		Temp
					eakage	Functional	
XICG cells						X	
LVDS with ECM						X	
I/O cells					debug purposes		
SSO	X	X				X	
Schmitt triggers	X	X					
ESD structures		Available @imec for debug purposes					
SRAM memory blocks	X	X	X		X	X	X
SRAM subcells	X	X			X	X	
PLL	X	X		X			
Linear voltage regulator	X	X		X		X	
Bandgaps	X	X			X	X	X
Switched voltage regulator	X	X				X	
Analog multiplexer	X	X					
Ring oscillators	X	X			X	X	
SEU test structures	X	X	X				
Countermeasures shift-registers	X	X			X	X	
SET test structures	X	X		X			

LIBRARY ELEMENTS TEST OVERVIEW



Single cell cross-section [cm^2]

	SP	DP
Kr	32e-9	120e-9
Xe	33e-9	120e-9

LIBRARY ELEMENTS TEST OVERVIEW

Test structure	SEL	Functional	SEU	SET	TID		Temp
					Leakage	Functional	
XICG cells	X	X				X	
LVDS with ECM	X	X				X	
I/O cells		Available @imec for debug purposes					
SSO	X	X				X	
Schmitt triggers	X	X					
ESD structures		Available @imec for debug purposes					
SRAM memory blocks	X	X	X		X	X	X
SRAM subcells	X	X			X	X	
PLL	X	X		X			
Linear voltage regulator	X	X		X		X	
Bandgaps	X	X			X	X	X
Switched voltage regulator	X	X				X	
Analog multiplexer	X	X					
Ring oscillators	X	X			X	X	
SEU test structures	X	X	X				
Countermeasures shift-registers	X	X			X	X	
SET test structures	X	X		X			

LIBRARY ELEMENTS TEST OVERVIEW

Test structure	SEL	Functional	SEU	SET	TID Leakage	TID Functional	Temp
XICG cells	X	X				X	
LVDS with ECM	X	X				X	
I/O cells	Available @imec for debug purposes						
SSO	X	X				X	
Schmitt triggers	X	X					
ESD structures	Available @imec for debug purposes						
SRAM memory blocks	X	X	X		X	X	X
SRAM subcells	X	X			X	X	
PLL	X	X		X			
Linear voltage regulator	X	X		X		X	
Bandgaps	X	X			X	X	X/X
Switched voltage regulator	X	X				X	
Analog multiplexer	X	X					
Ring oscillators	X	X					
SEU test structures	X	X	X				
Countermeasures shift-registers	X	X					
SET test structures	X	X		X			

3.3V supply bandgap is according spec
1.8V supply bandgap need die-2-die variation improvement

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APPLICATION ASIC
RECORE

Architecture + Verification Results

APPLICATION ASIC
SEE IRRADIATION TESTS

SEU	SRAM
	Scan chains
SET	ATPG
	Functional
SEL	Latch-up

- Cross-section seems somewhat higher than isolated LTV blocks

- Rad hardness hit DFF confirmed
- non hardened cells in set/reset

Max. cross-section full XentiumDARE seen is 4.10^{-5} cm^2

No latch-up seen on chip

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LESSONS LEARNED

- For the DTV delays were introduced due to measurements done in other activity. From the other side we learned that it is difficult to estimate resources needed for mixed-signal design, characterization and radiation testing if specs are investgated during the project.
  No ideal way seems available.
- Combining functional validation/demo board and radiation load board did not save resources.

LESSONS LEARNED

- We think it is better to split such big activities in to two or three projects with less broad objectives for each.
- Following Murphy's law taping a sub-optimal design will come back later. In this case, for XentiumDARE not maximum frequency could be reached for all benchmarks due to compromises made for layout of an area-, pin- and timing-constrained design.

CONCLUSIONS

A long journey has in the end resulted in a mature radiation hardened DARE180U library for full-custom analog (DTV) and mixed signal (LTV+ApplASIC) ASICs.