

FSS in support of MBSE

Final Presentation – Demonstration

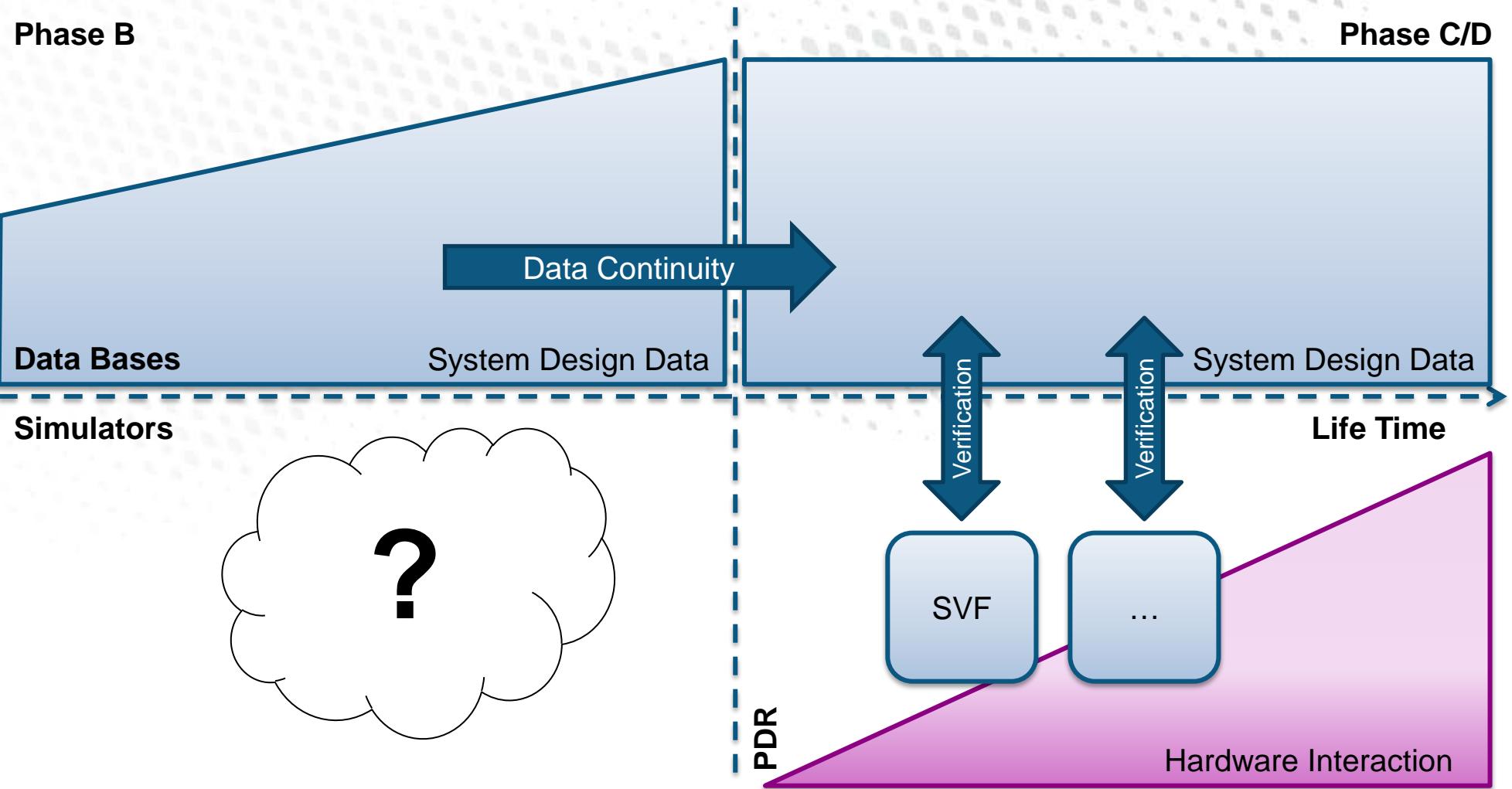
TEC-ED & TEC-SW Final Presentation Days 2014

P. M. Fischer

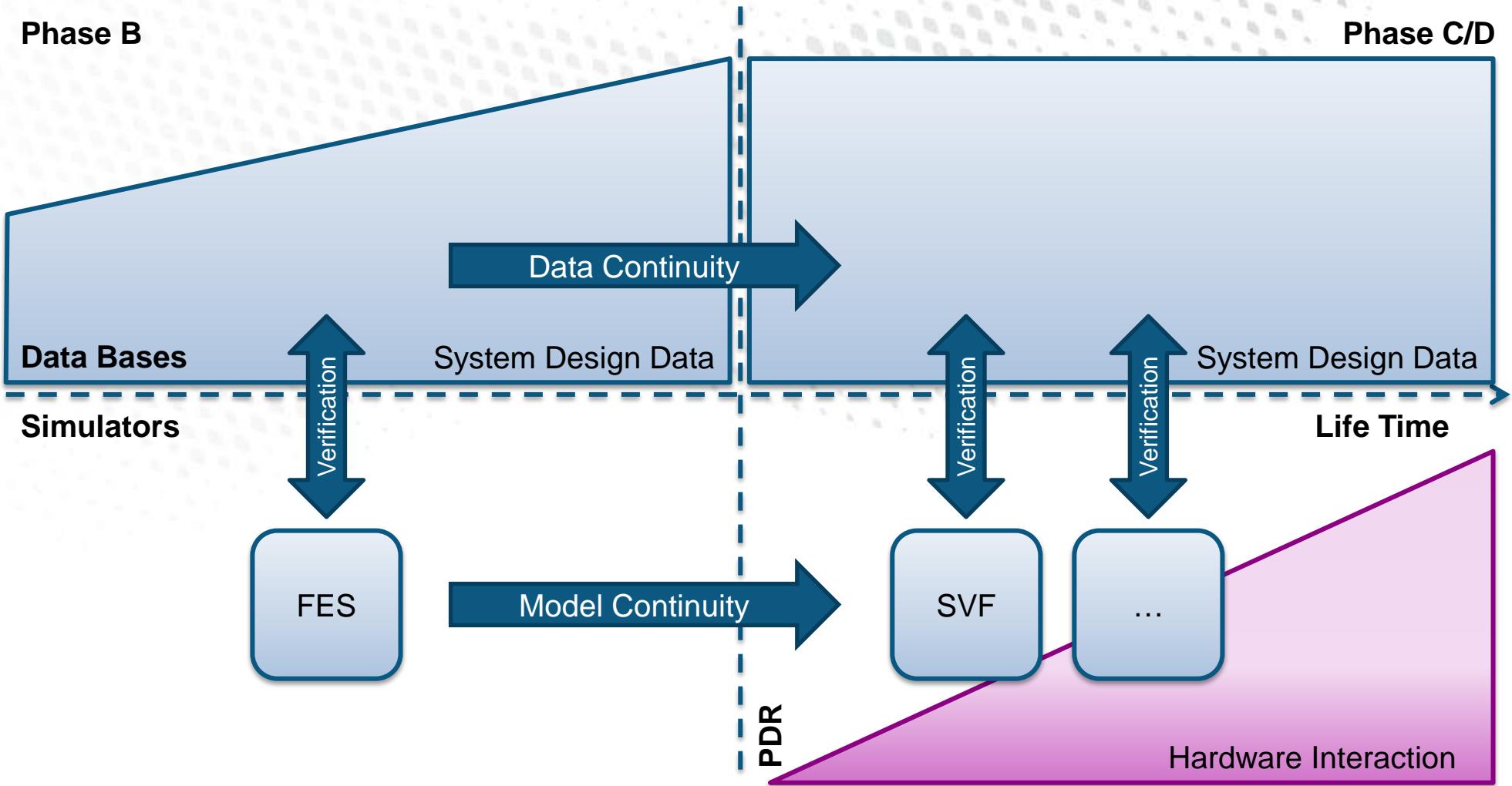
9th December 2014

FSS in MBSE Study Goal and Consortium

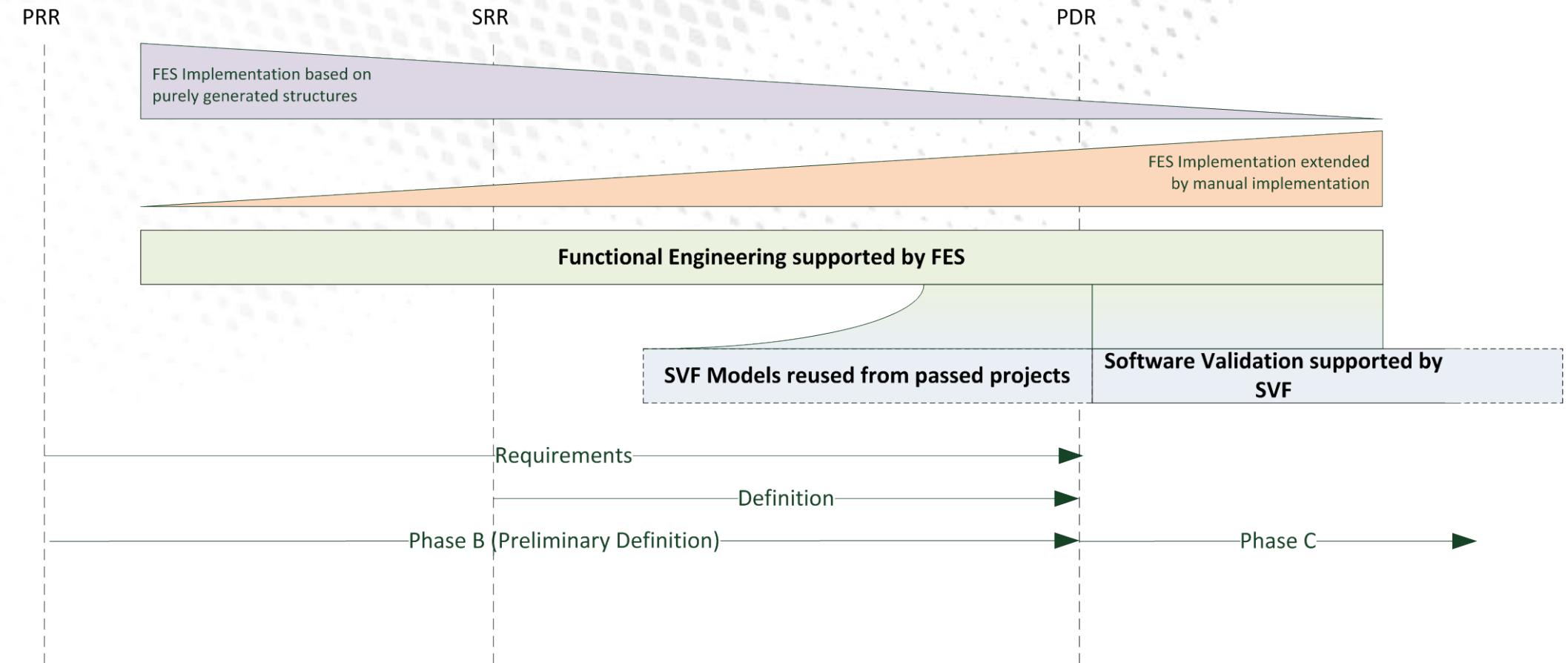
Need to Improve Design Maturity allready in Phase B



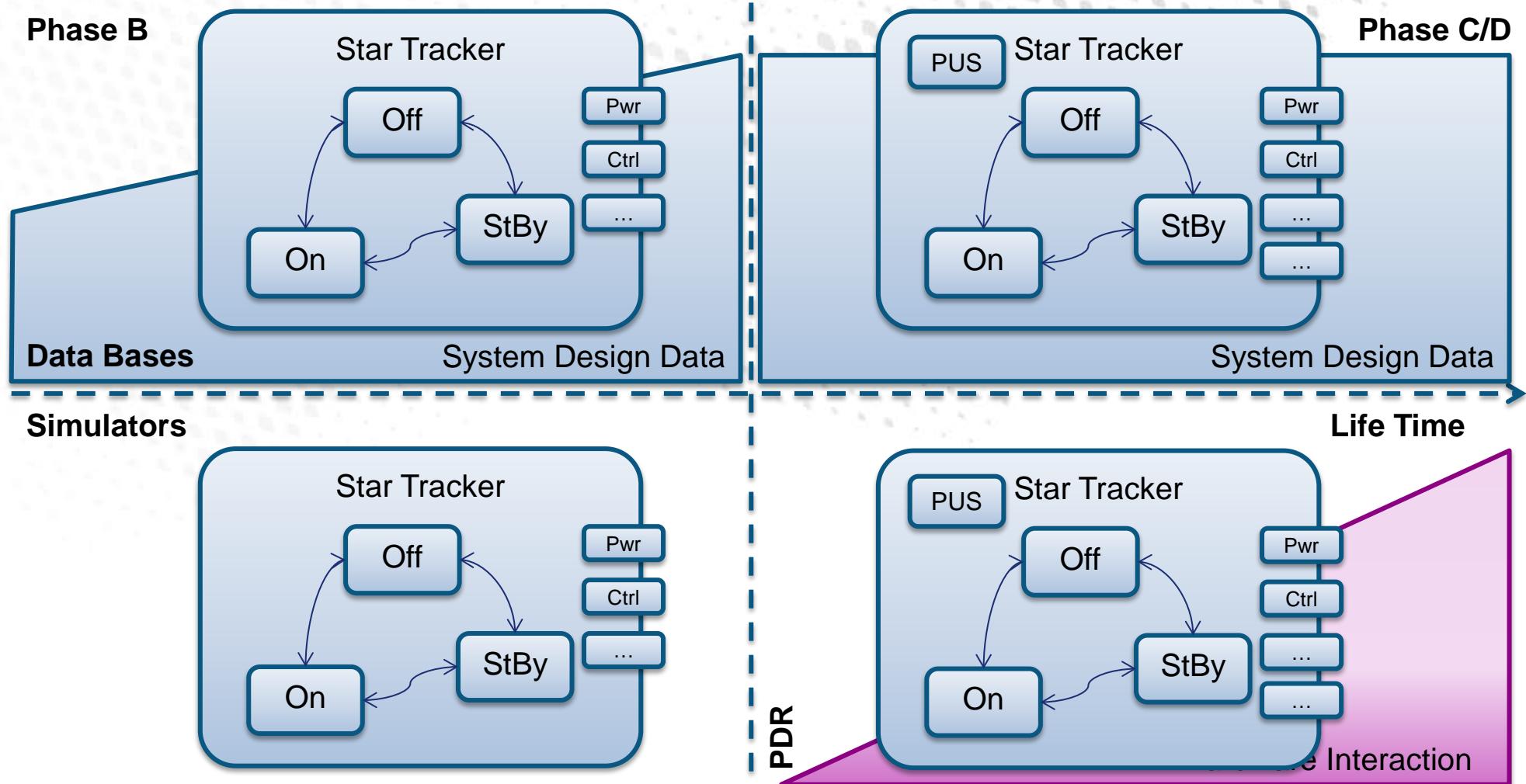
Goal I: Configure Simulator from System Design to Verify Before PDR



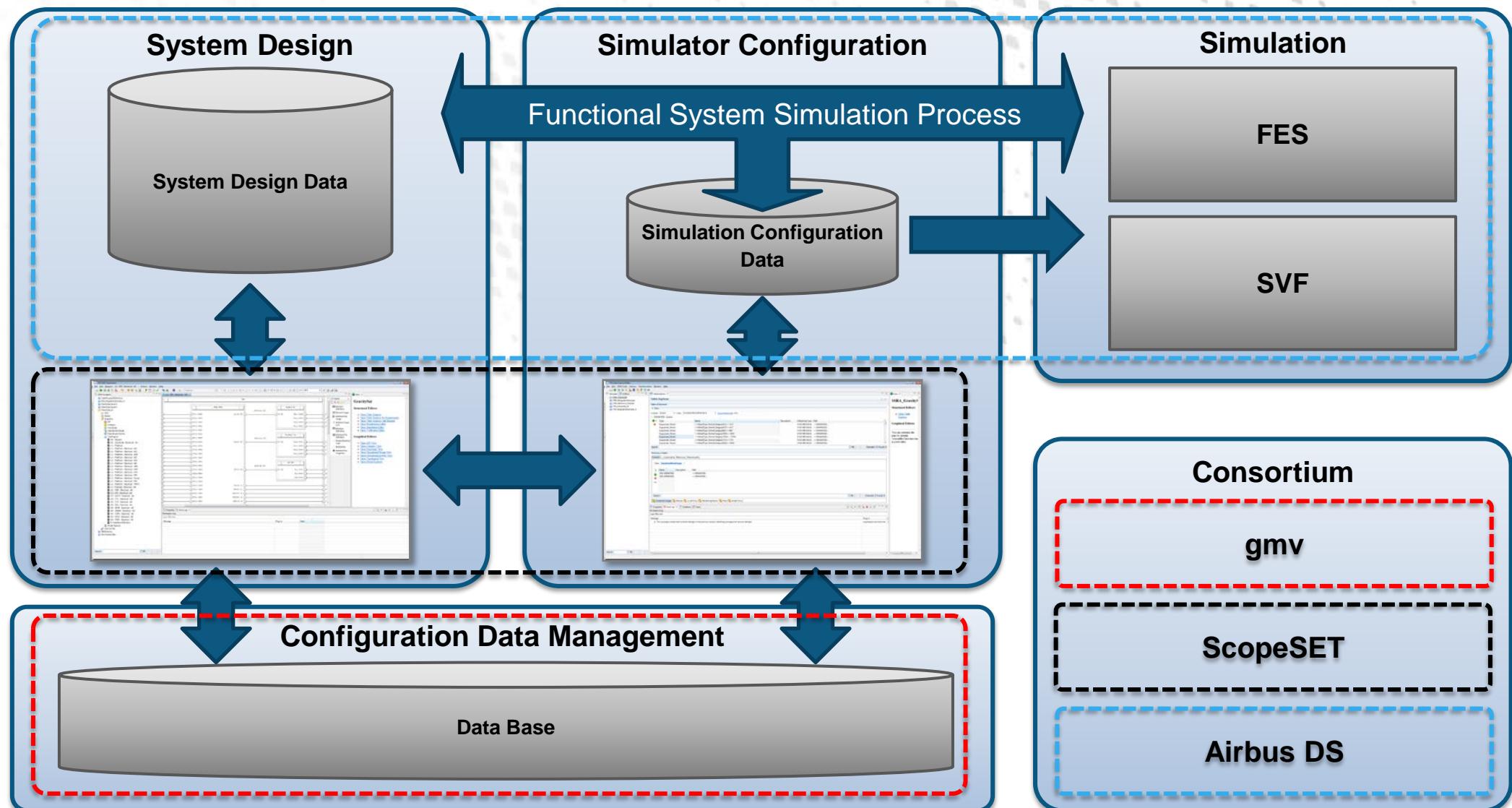
Goal II: Model Continuity from FES to SVF in the Design Phases



Example: Common Components in System and Simulation Data

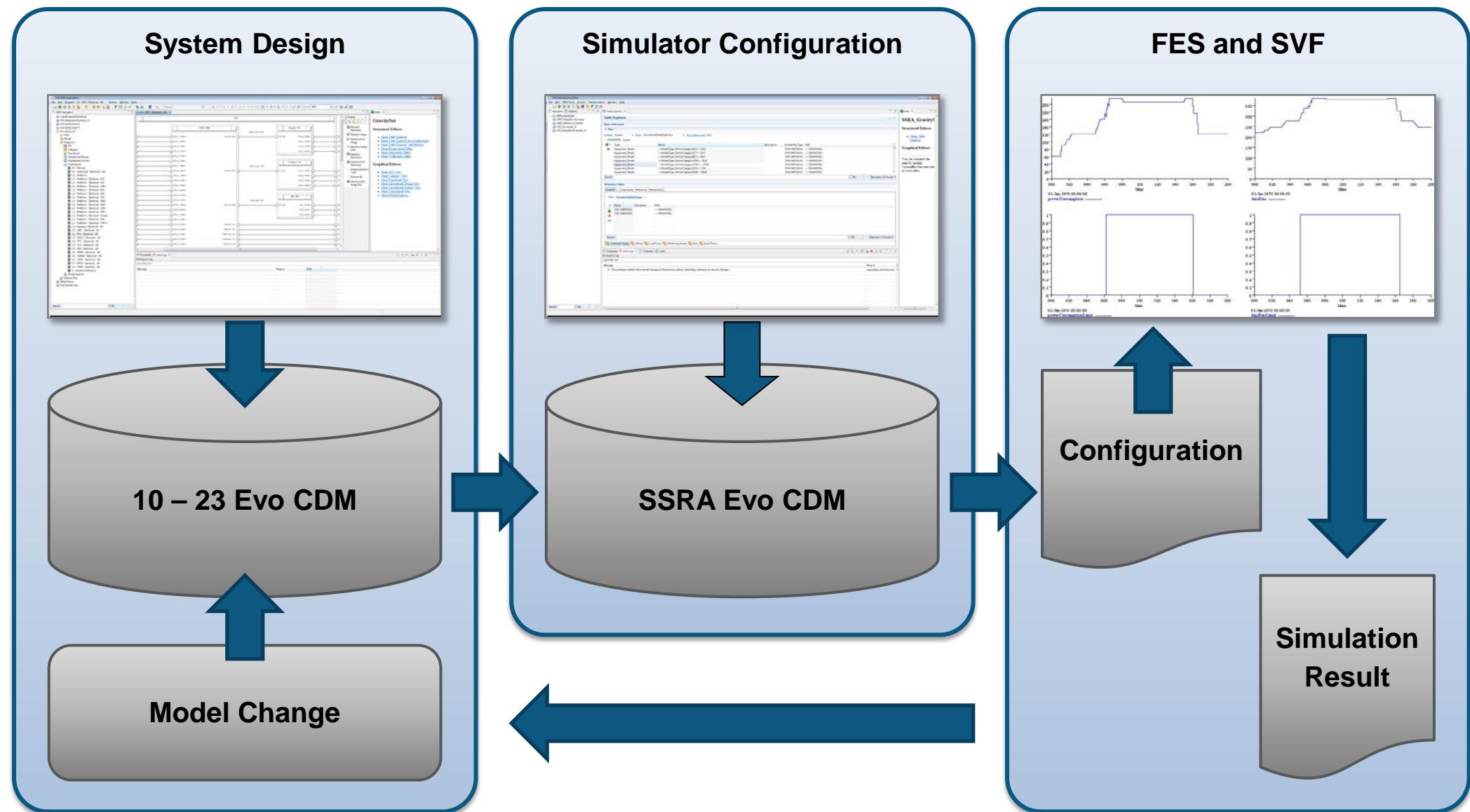


Data, Tools, Processes to uses System Data for Simulator Configuration

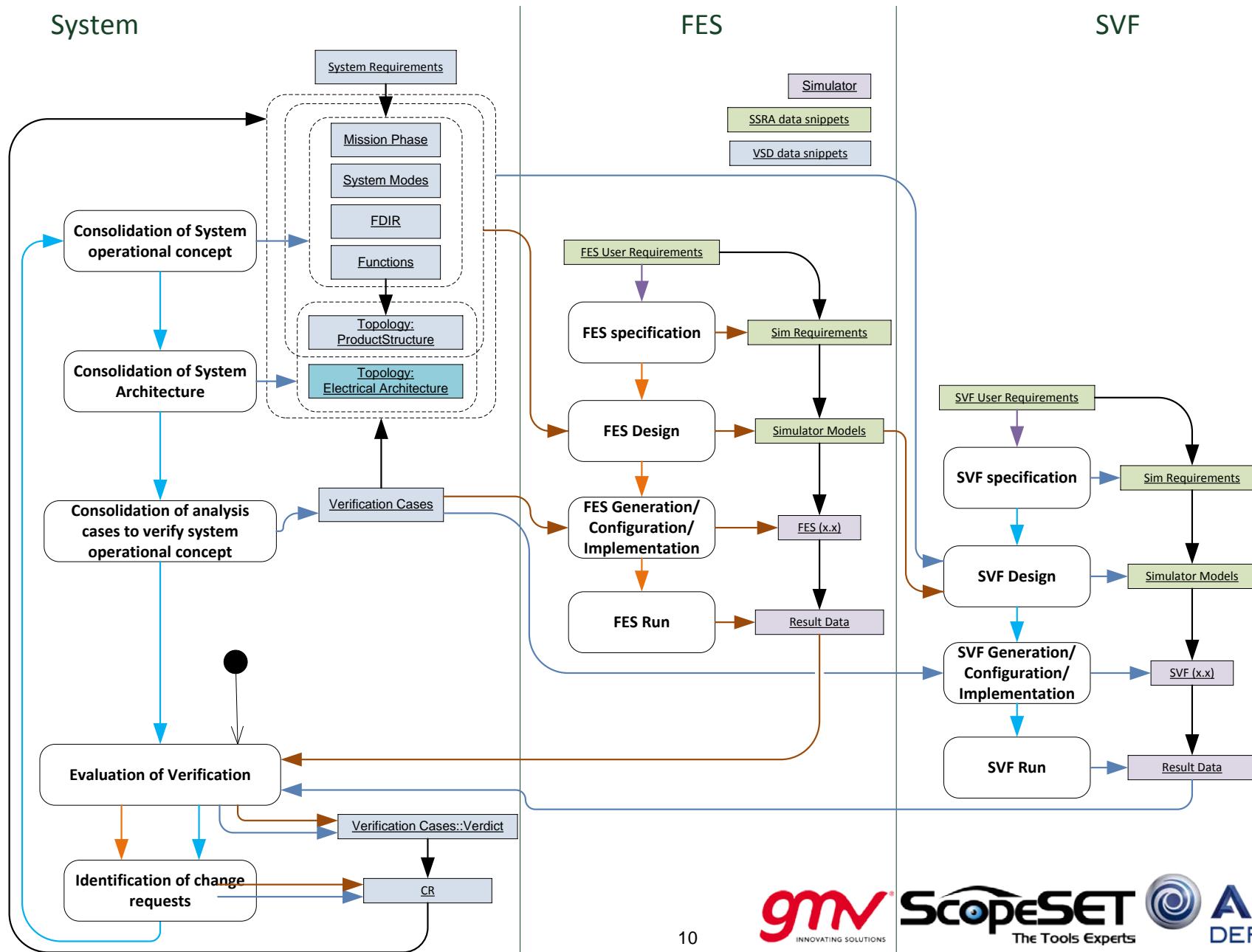


Functional System Simulation Process and Concepts

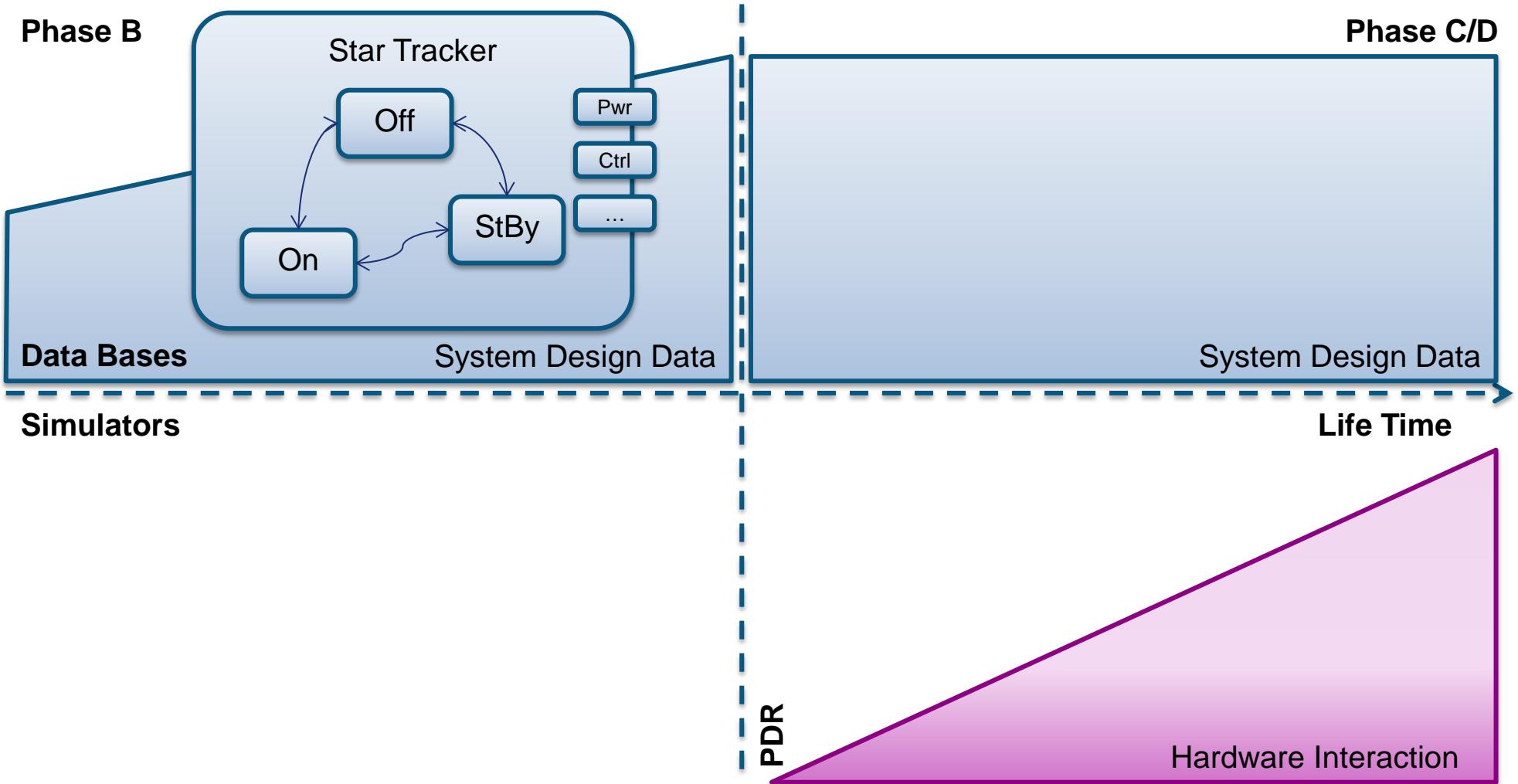
Overall Process of the Functional System Simulation



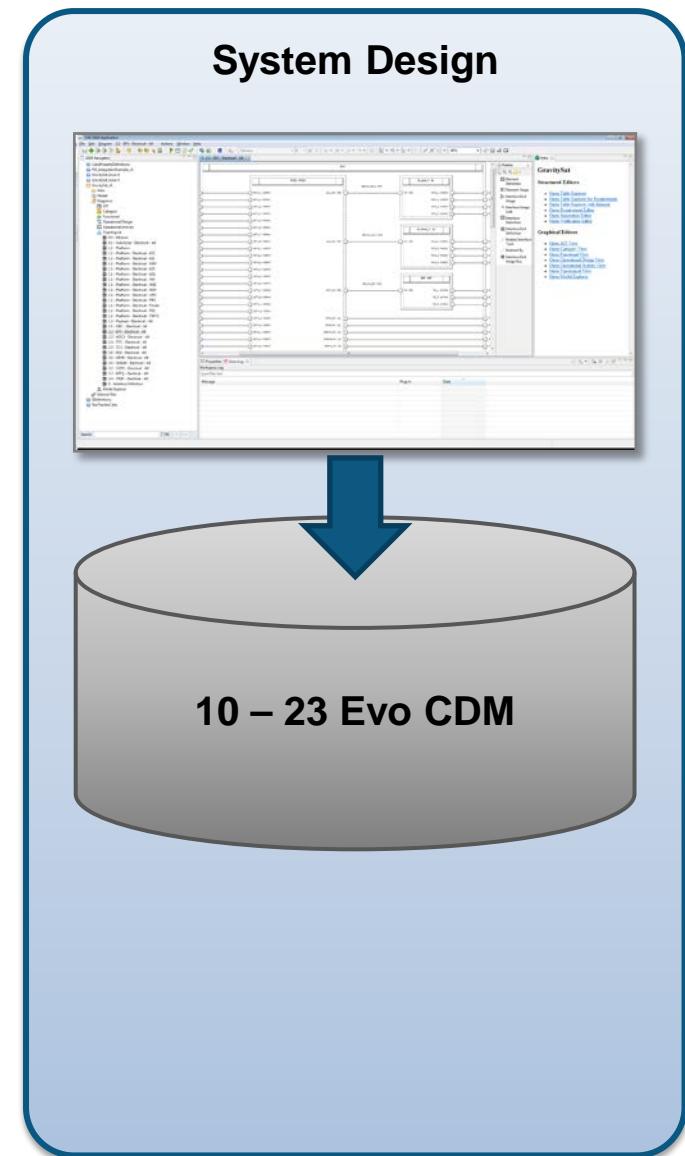
Functional System Simulation Process in Detail



Example: Modelling the Star Tracker in the System Design Data



Modelling System Design Data in 10-23 Evo using VSD



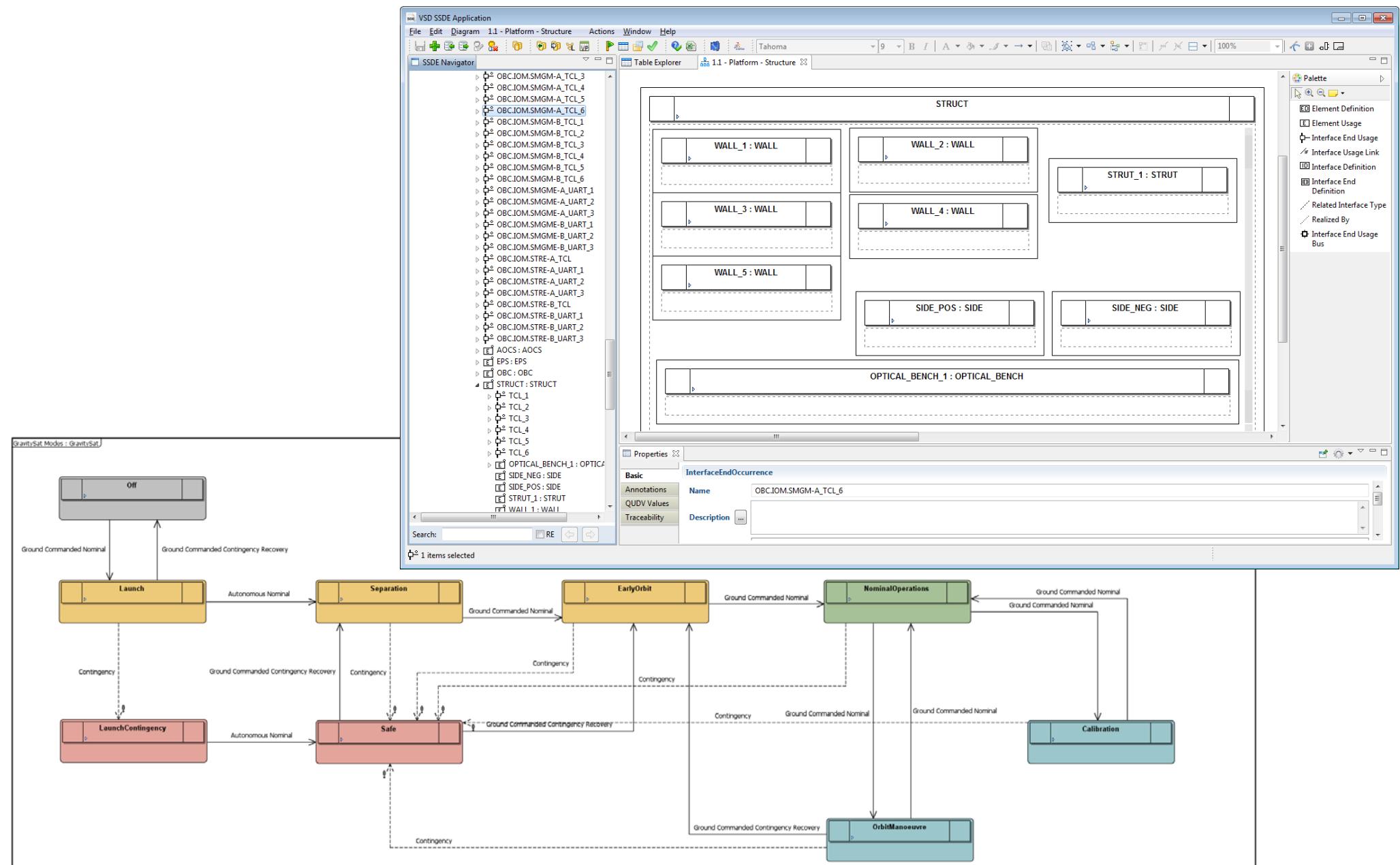
System Design Data is stored in an Evolution of 10 - 23

- Authoring of Data covered by VSD SSDE

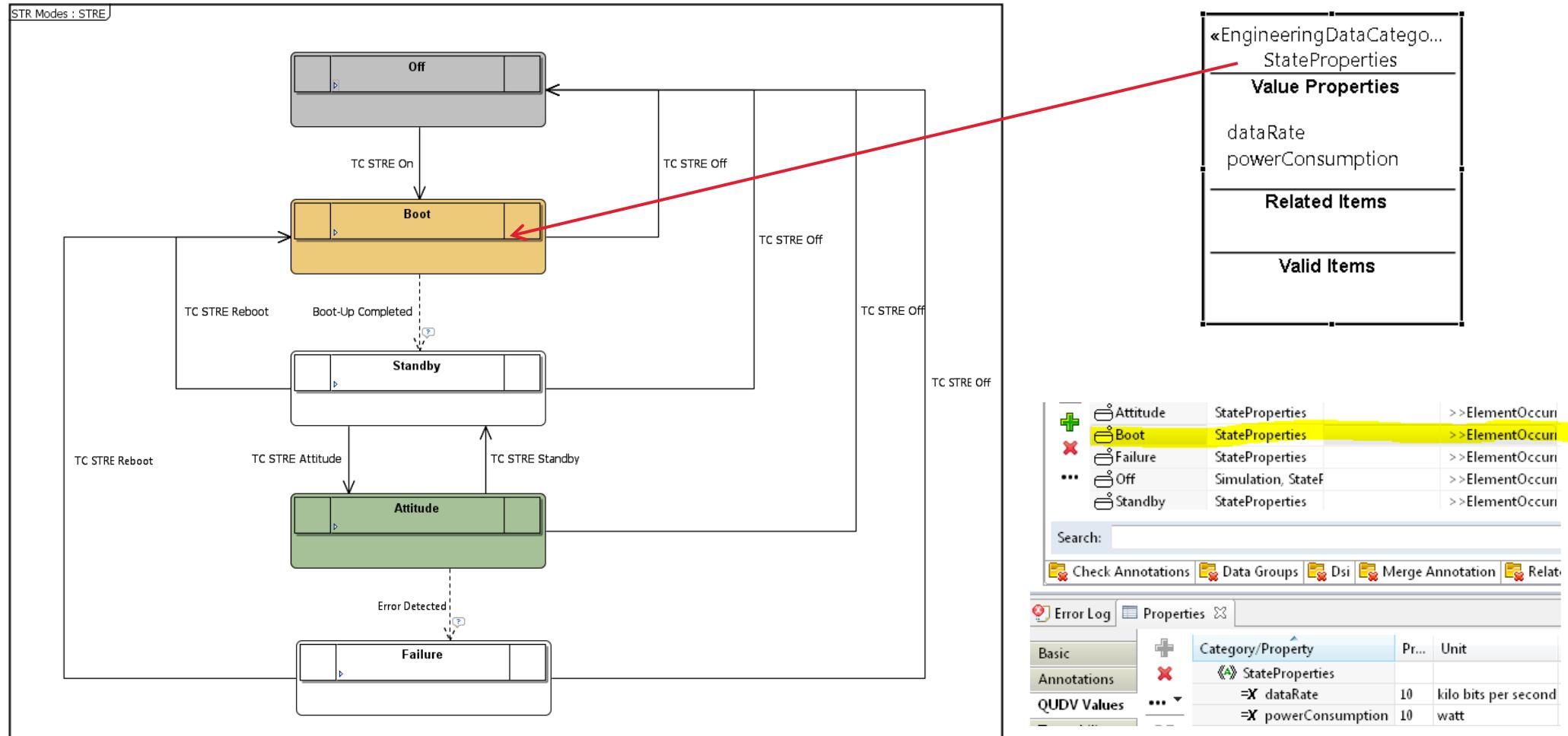
System Design Data content of a Sample Mission including

- Mission Specification
- System Specification
 - Related to later demonstration cases suchg as FDIR and Data Rates
- System Operational Concept
- System Modes including PUS Services
- System Architecture Definition
- System Verification with Analysis Cases

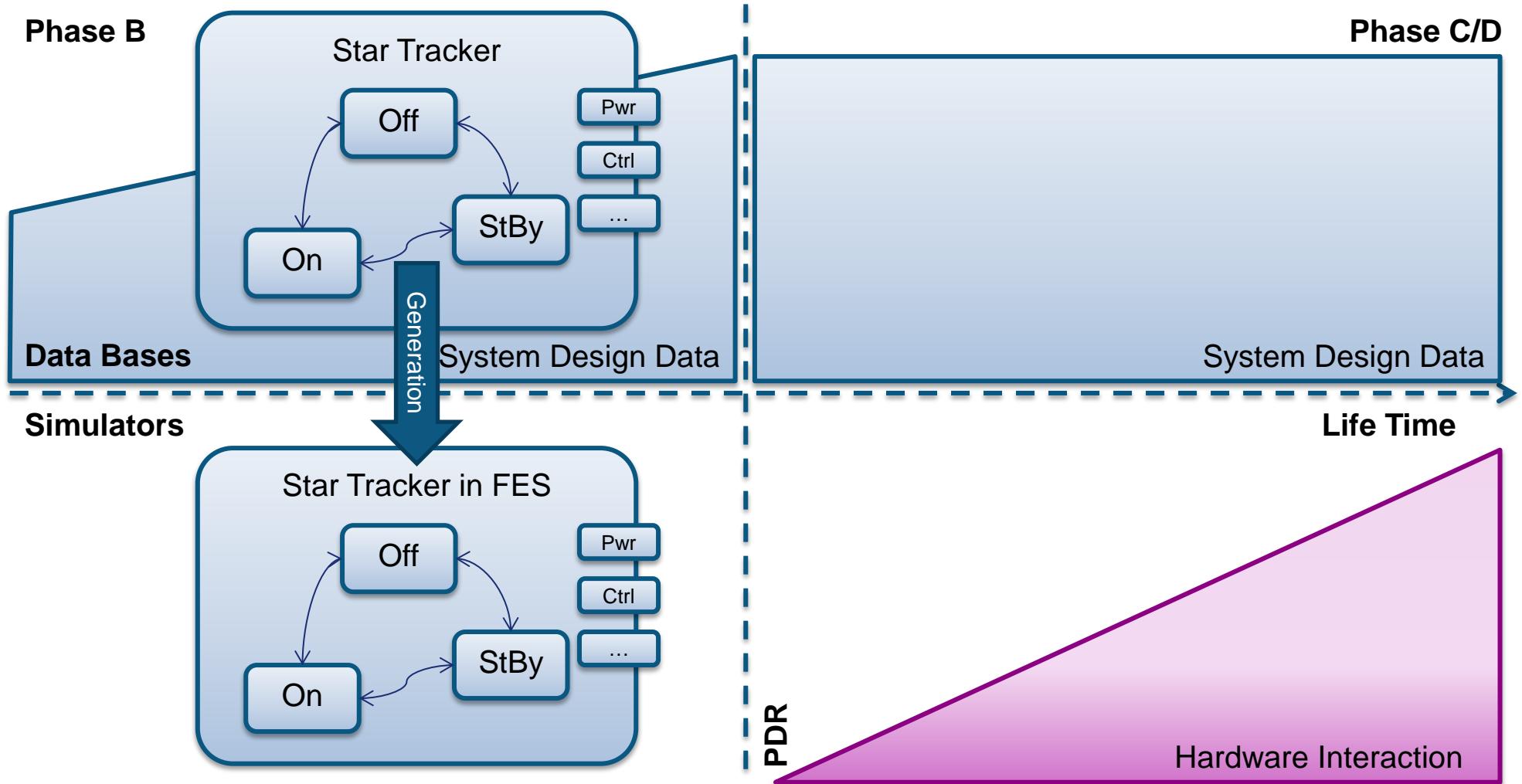
Modelling in VSD – Such as System Operational Concept



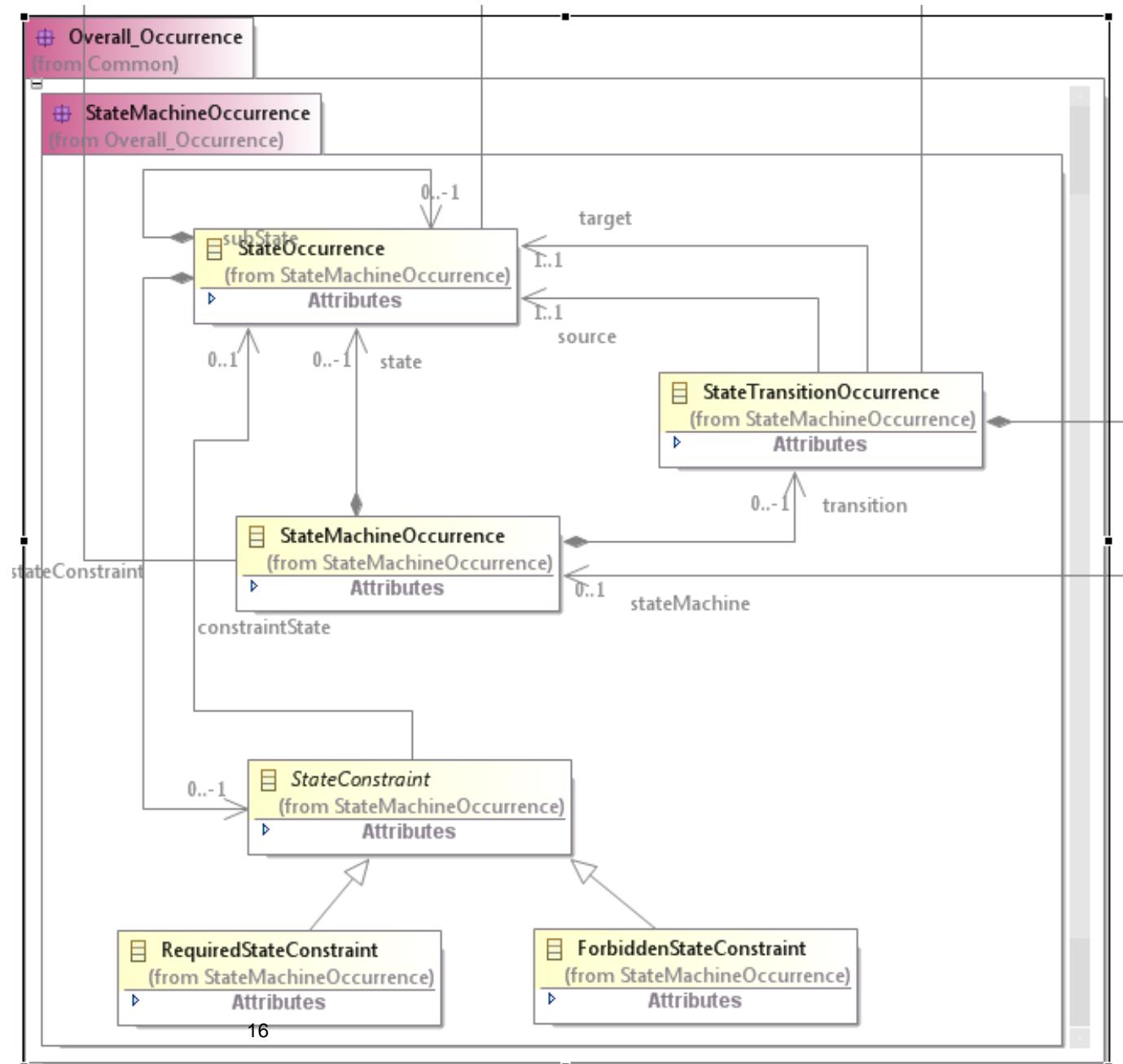
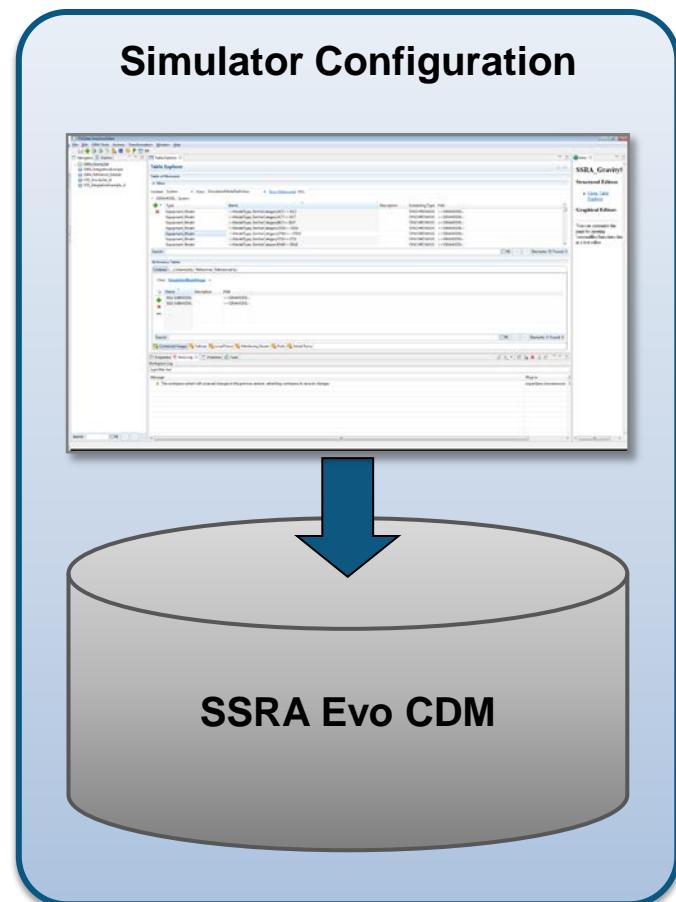
Example of the Equipment modes Extended by Categories



Example: Transferring the System Design into the FES Configuration



Managing Simulator Configuration Data in SSRA Evolution



Populating the SSRA Model from the System Model

System Design Data authored in SSDE

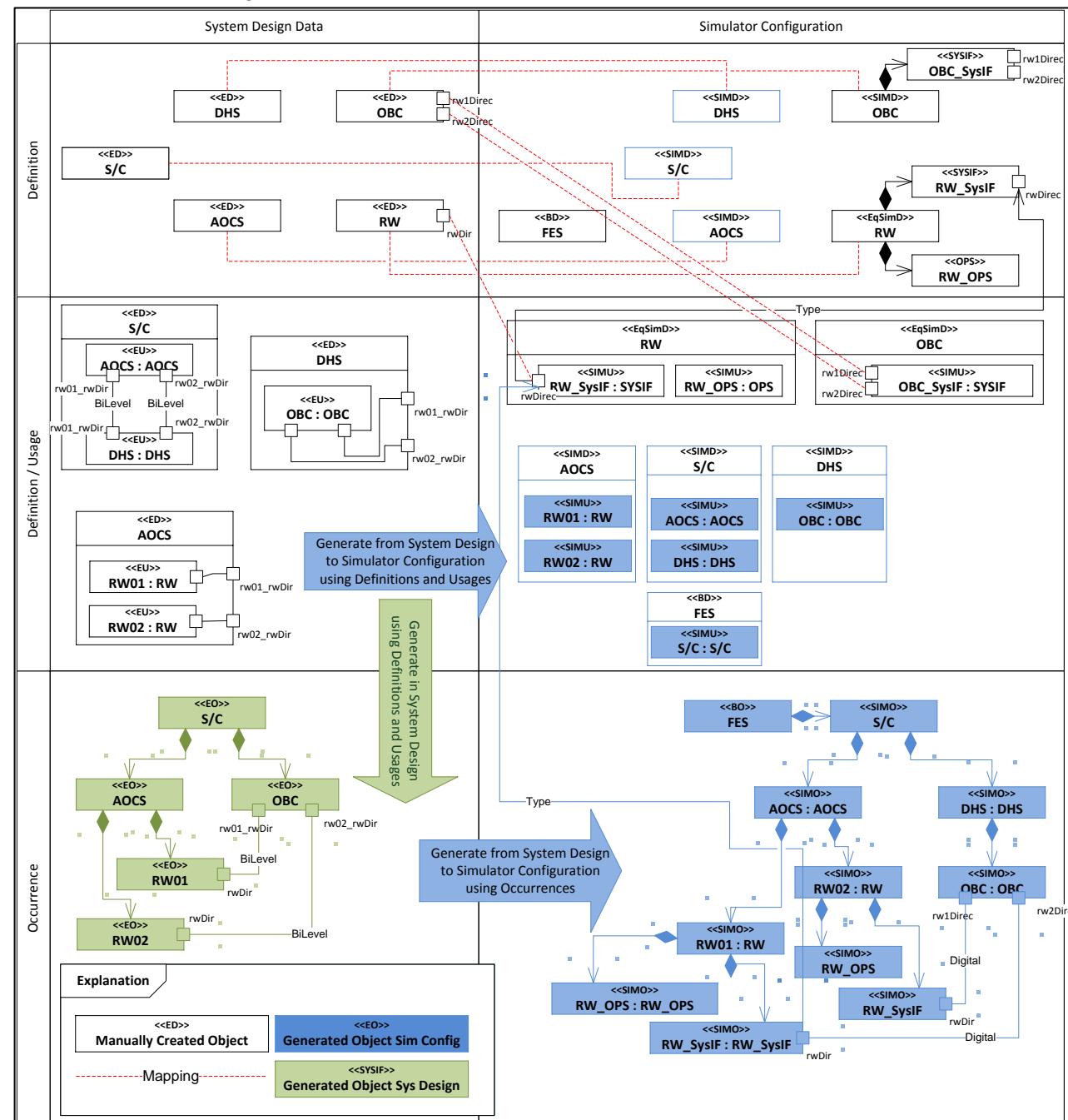
- Using Occurrence Generator in SSDDE

Simulator Configuration gets Generated

- Simulation Models imported from Library
- Manual Modifications Possible

Simulator Configuration Population

- Derived from System Model
- Generates all Missing Data such as:
 - Complete Product Structure
 - State Machines
 - Services



SSRA Configuration and DataSet Management

Default Configuration as Root for Others

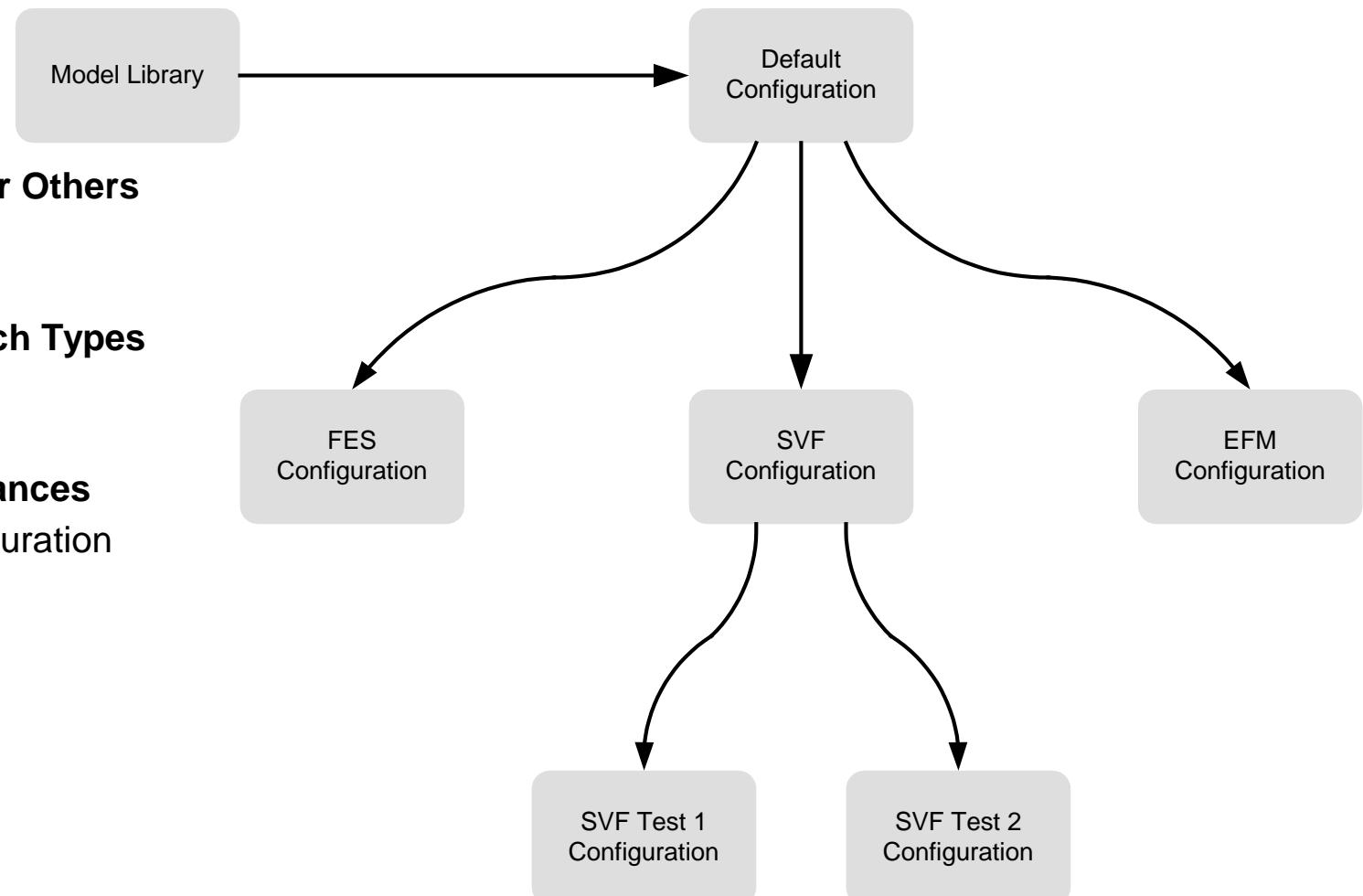
- Contains Common Information

Individual Modifications for Bench Types

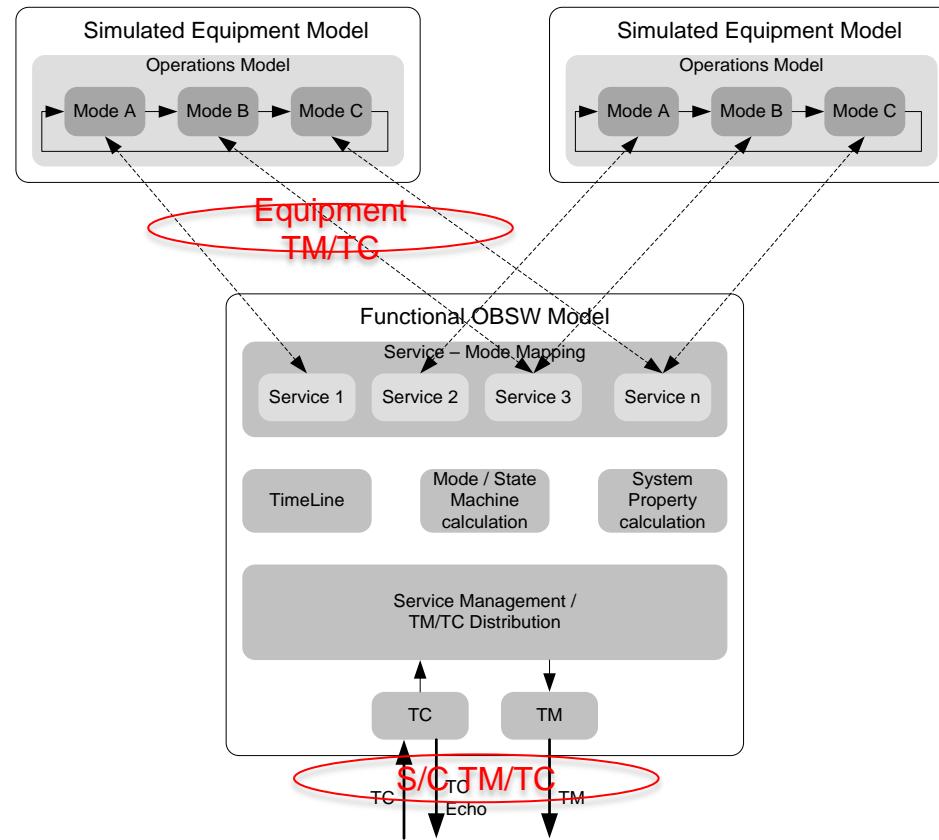
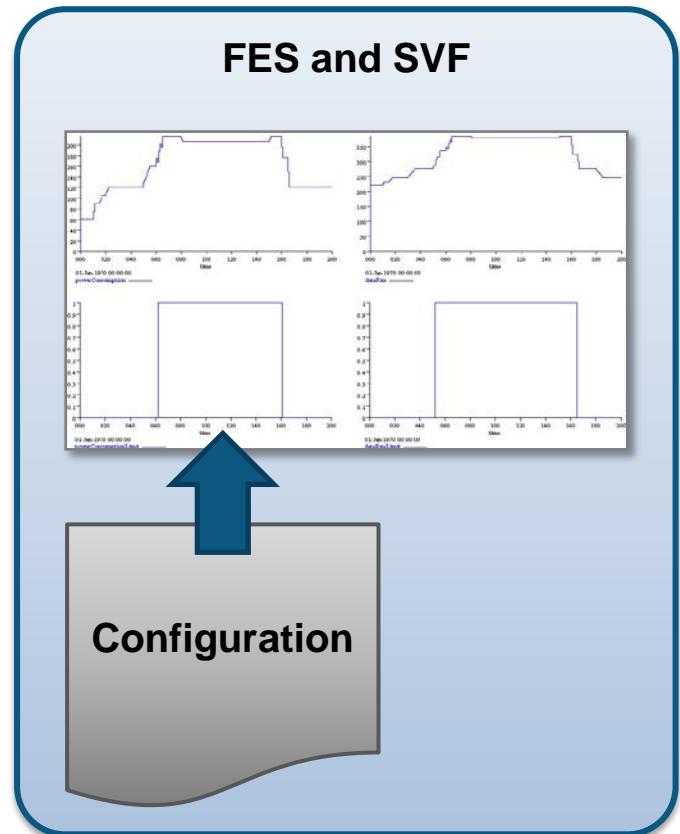
- Such as Interfaces for SVF

Individual Config for Bench Instances

- Contains Bench Specific Configuration



FES Architecture Communication and its Configuration



Communication based on equipment mode function calls

- Service to Mode Mapping

Functional OBSW Model triggers equipment modes

- Trigger of mode related functions

Configured by Excel Based Input

Mapping SSRA to FES Configuration

FES Configured by Excel File including

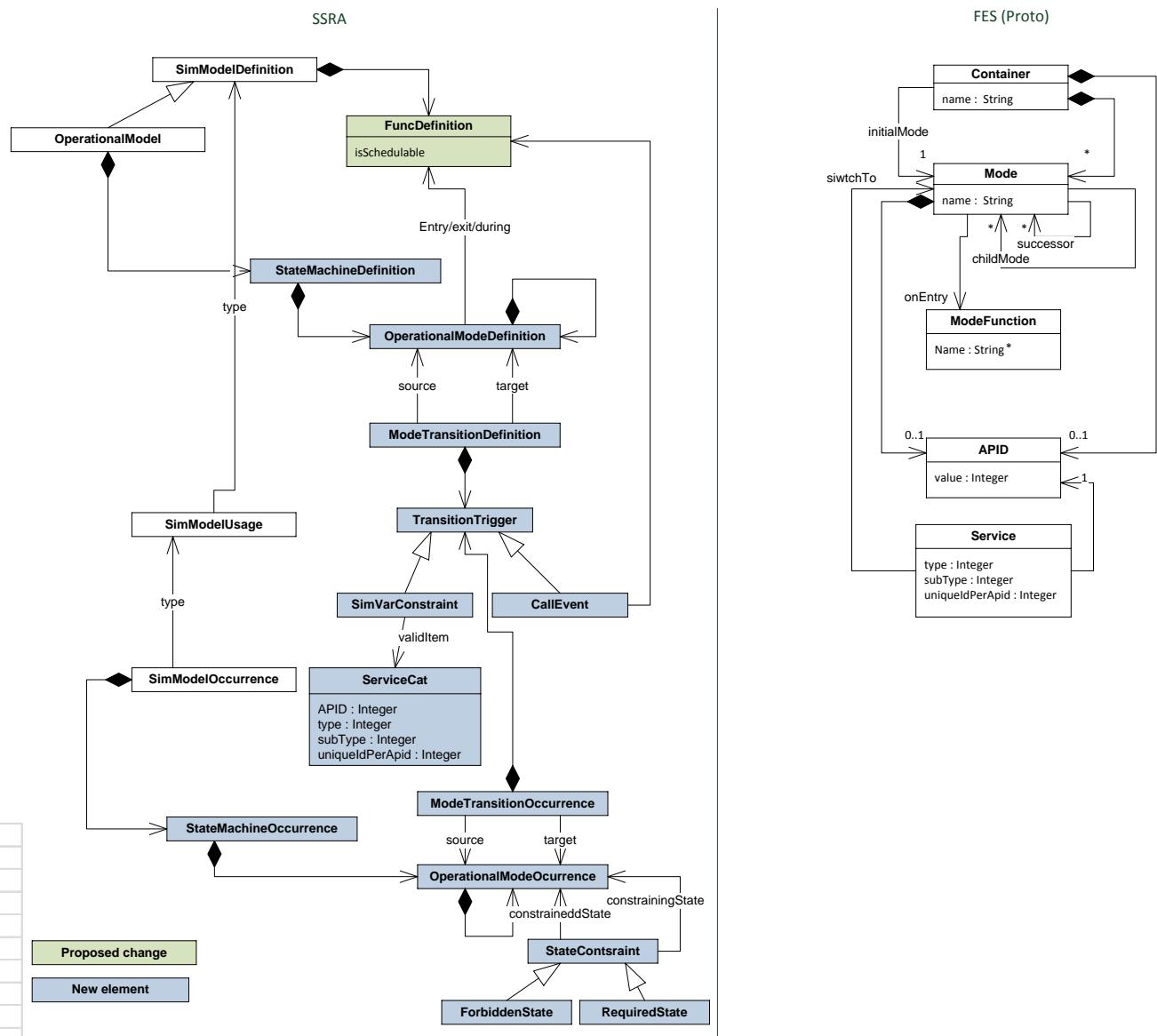
- Model Instantiation
- Scheduling
- State Machines
- Transitions
- Services

Need to Create Configuration from SSRA

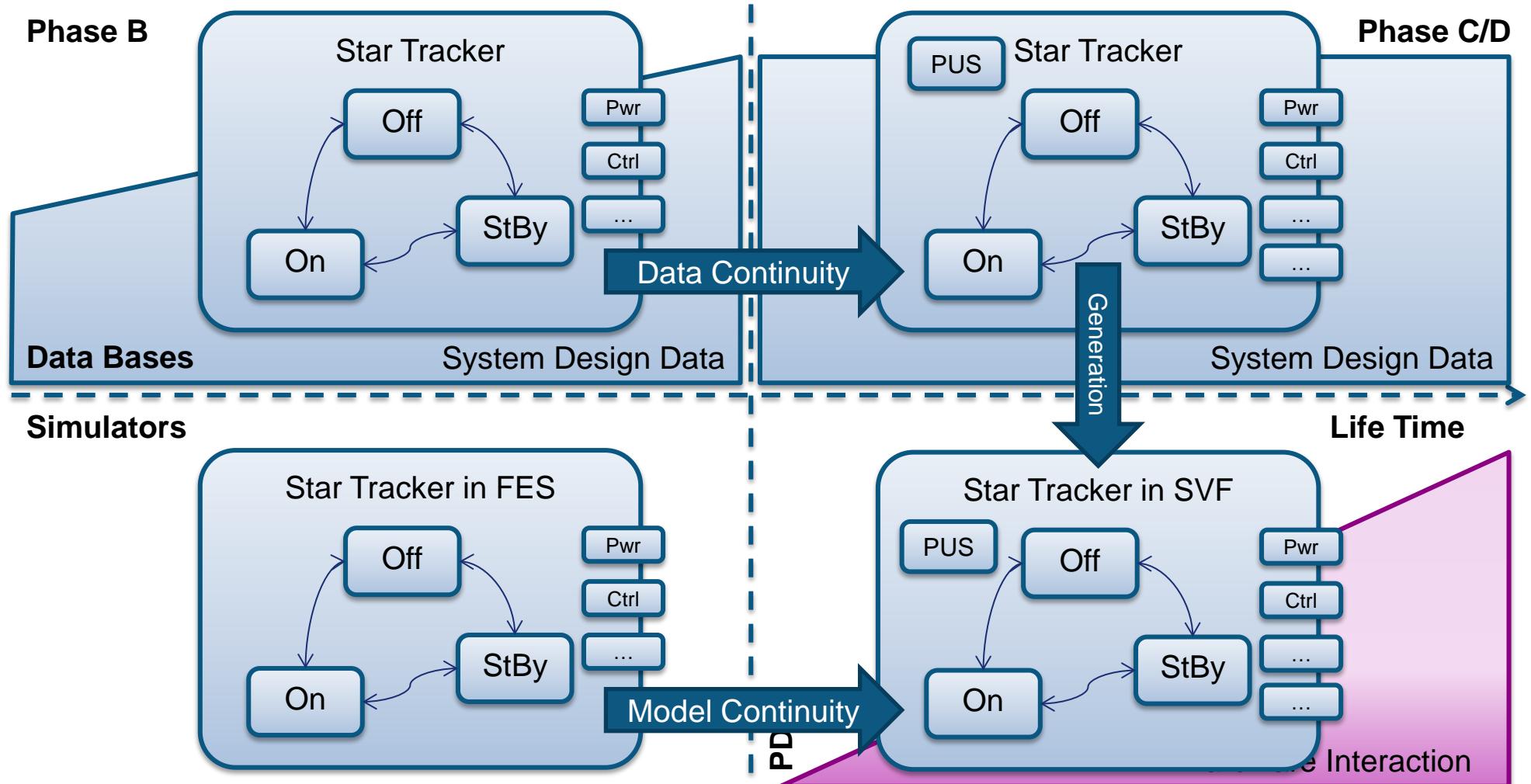
registerMode	GPSR_A	Off
registerMode	GPSR_A	Startup
registerMode	GPSR_A	Standby
registerMode	GPSR_A	Navigate
registerMode	GPSR_A	Failure

registerSuccessor	GPSR_A	Off	Startup
registerSuccessor	GPSR_A	Startup	Standby
registerSuccessor	GPSR_A	Startup	Off
registerSuccessor	Standby	Startup	Startup
registerSuccessor	Standby	Standby	Navigate
registerSuccessor	Standby	Standby	Off
registerSuccessor	Standby	Navigate	Standby
registerSuccessor	Standby	Navigate	Off
registerSuccessor	Standby	Navigate	Failure

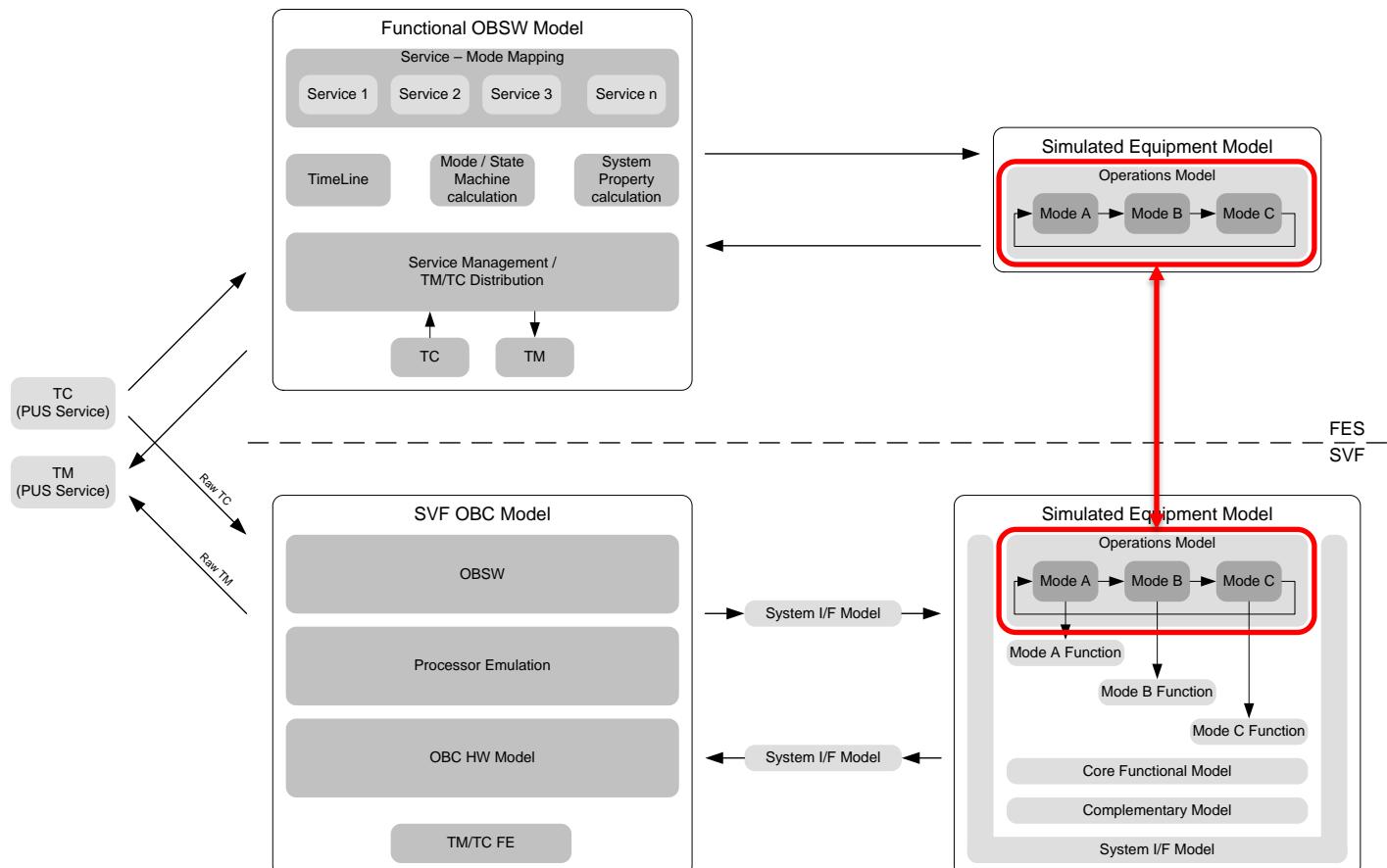
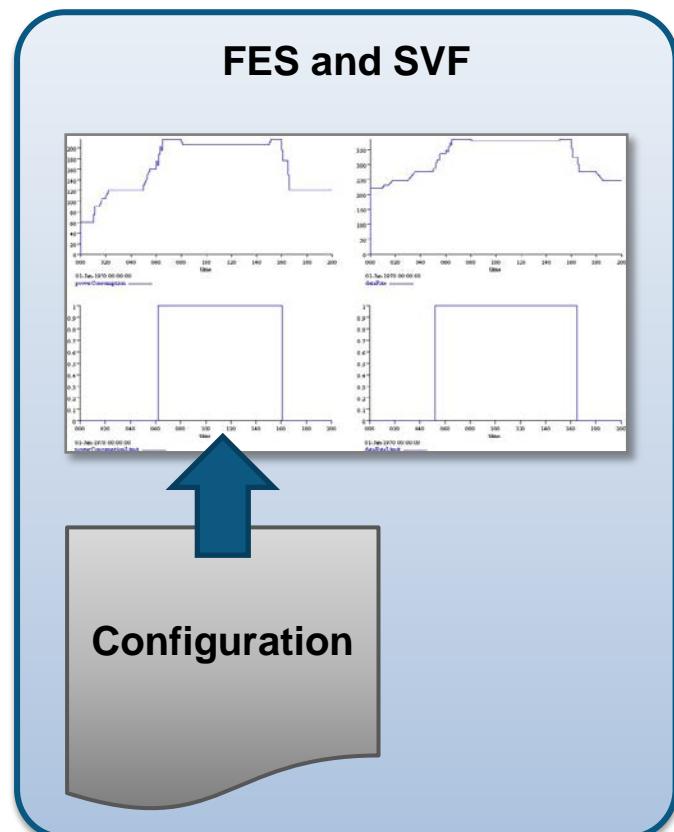
#registerChildMode	param1	param2	param3	param4	param5
registerChildMode	AOCS	STB	MGM_C	Off	
registerChildMode	AOCS	STB	CESS_1	Off	
registerChildMode	AOCS	STB	CGPS_A	Off	
registerChildMode	AOCS	STB	CGPS_B	Off	
registerChildMode	AOCS	STB	GPSR_B	Off	
registerChildMode	AOCS	STB	CESS_4	Off	
registerChildMode	AOCS	STB	GPSR_A	Off	
registerChildMode	AOCS	OCM	GPSR_A	Navigate	
registerChildMode	AOCS	OCM	MTQ_1	On	
registerChildMode	AOCS	OCM	STRE_B	Attitude	
registerChildMode	AOCS	OCM	STRE_A	Attitude	
registerChildMode	AOCS	OCM	MTQ_2	On	
registerChildMode	AOCS	OCM	CESS_6	On	
registerChildMode	AOCS	OCM	MGM_A	On	
registerChildMode	AOCS	OCM	GPSR_B	Navigate	



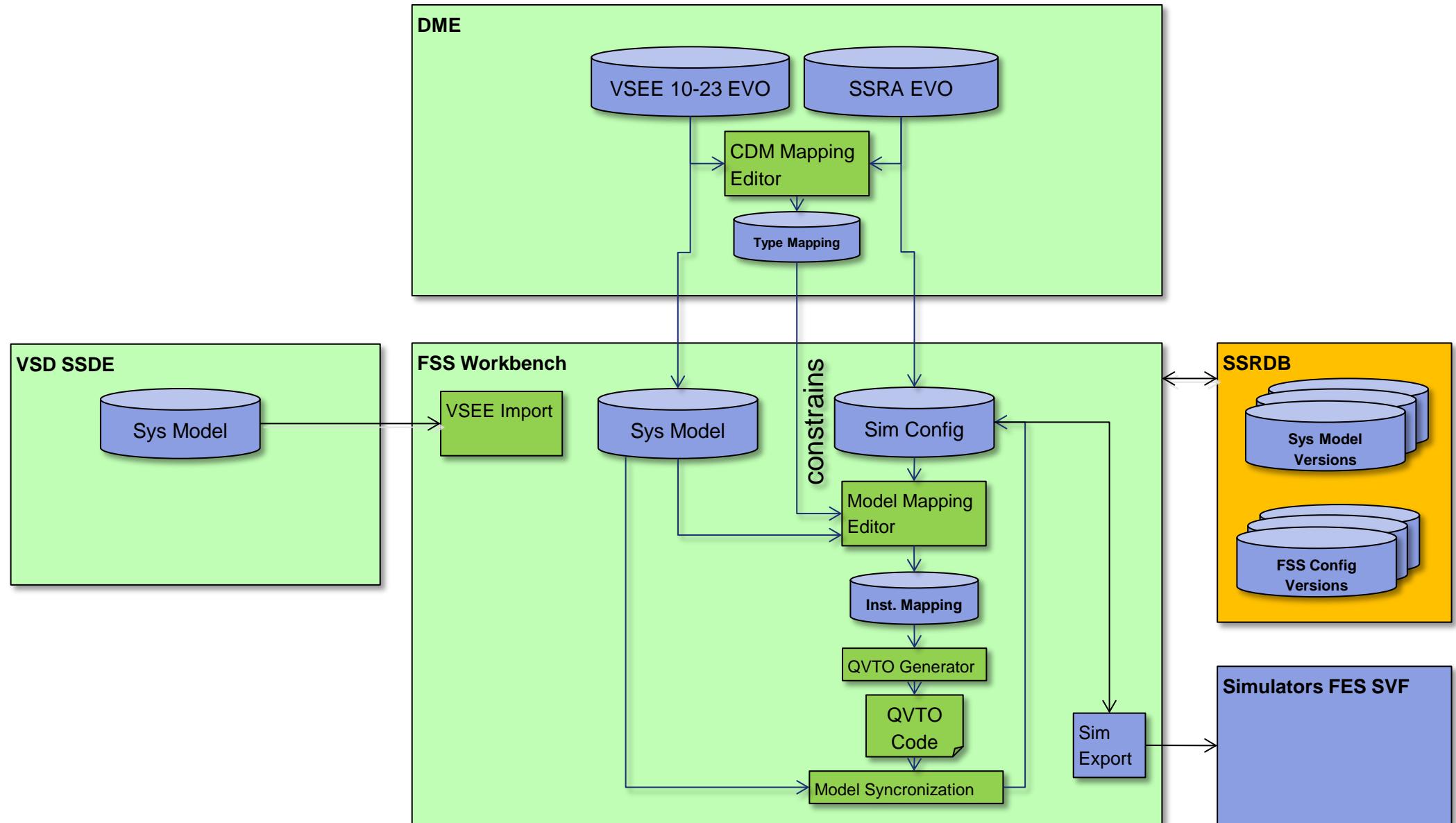
Example Common Components in System and Simulation Data



From an FES to SVF based on Common State Machine



Developed FSS Architecture and Tools

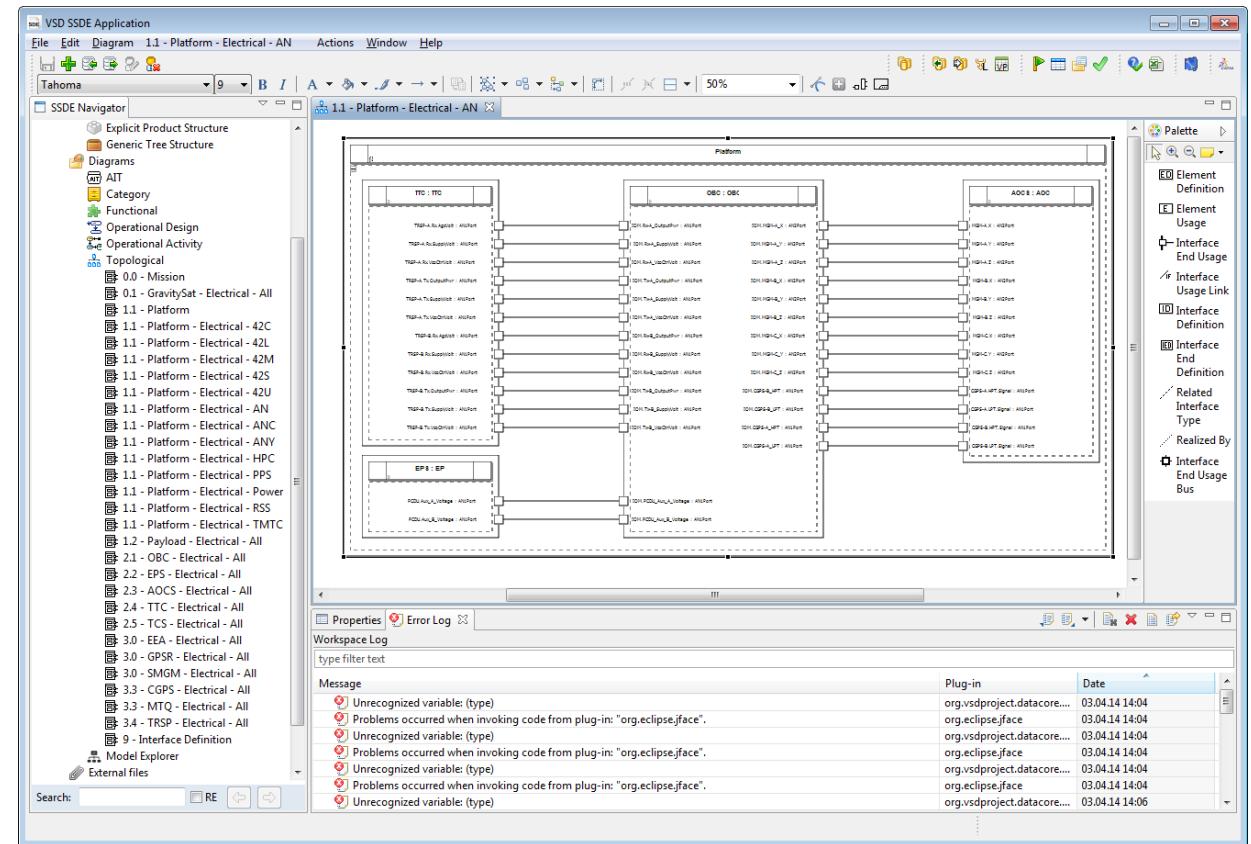


Demonstration and Evaluation Scenarios

Overview of Demonstration and Evaluation Scenarios

All Scenarios based on GravitySat

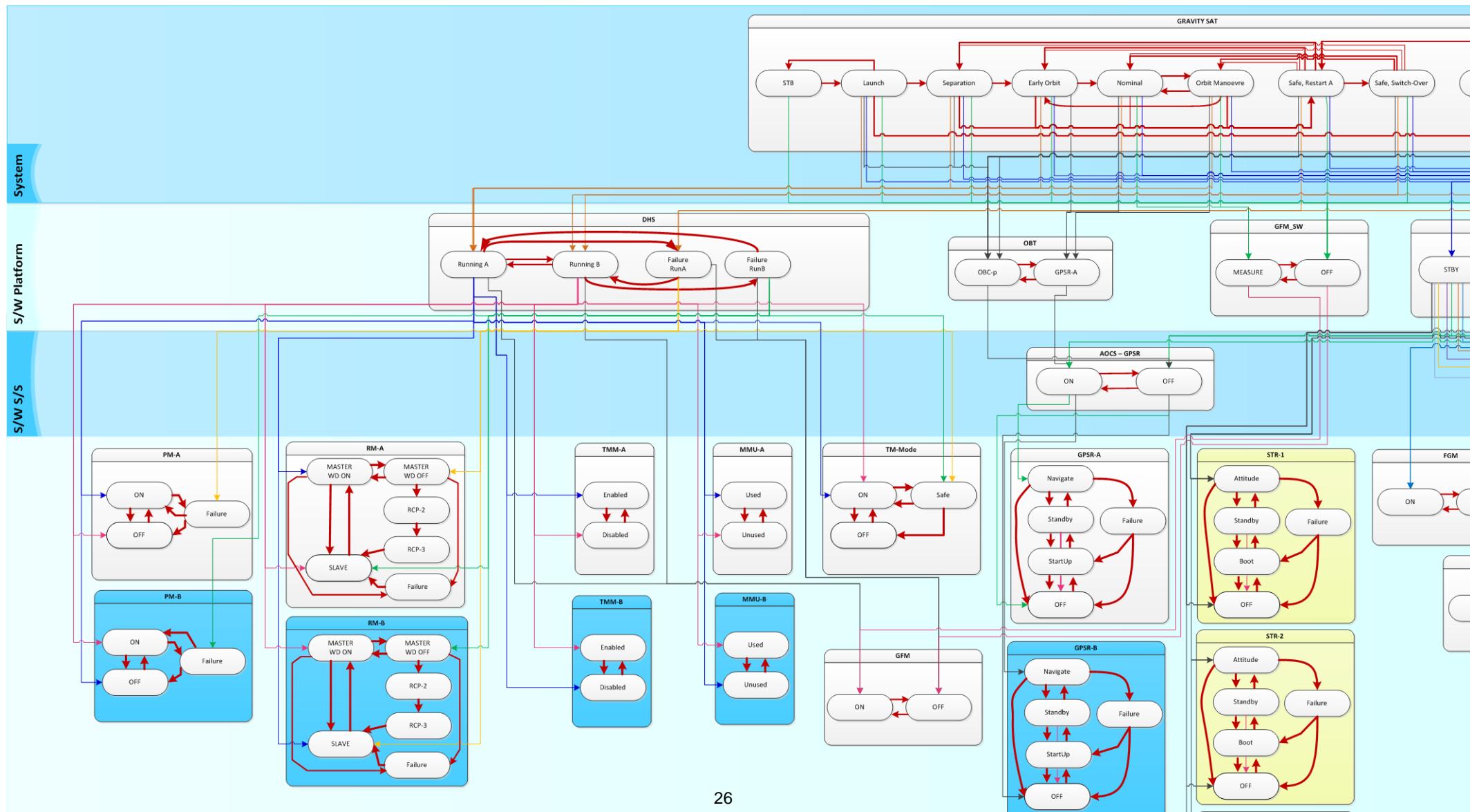
- based on lessons learned from real missions
- Data Set contains e.g.:
 - Complete Product Structure
 - Operational Design by State Machines
 - Complete Functional Electrical Architecture
- Around 6 SubSystems + Payload
- More than 60 individual Equipment



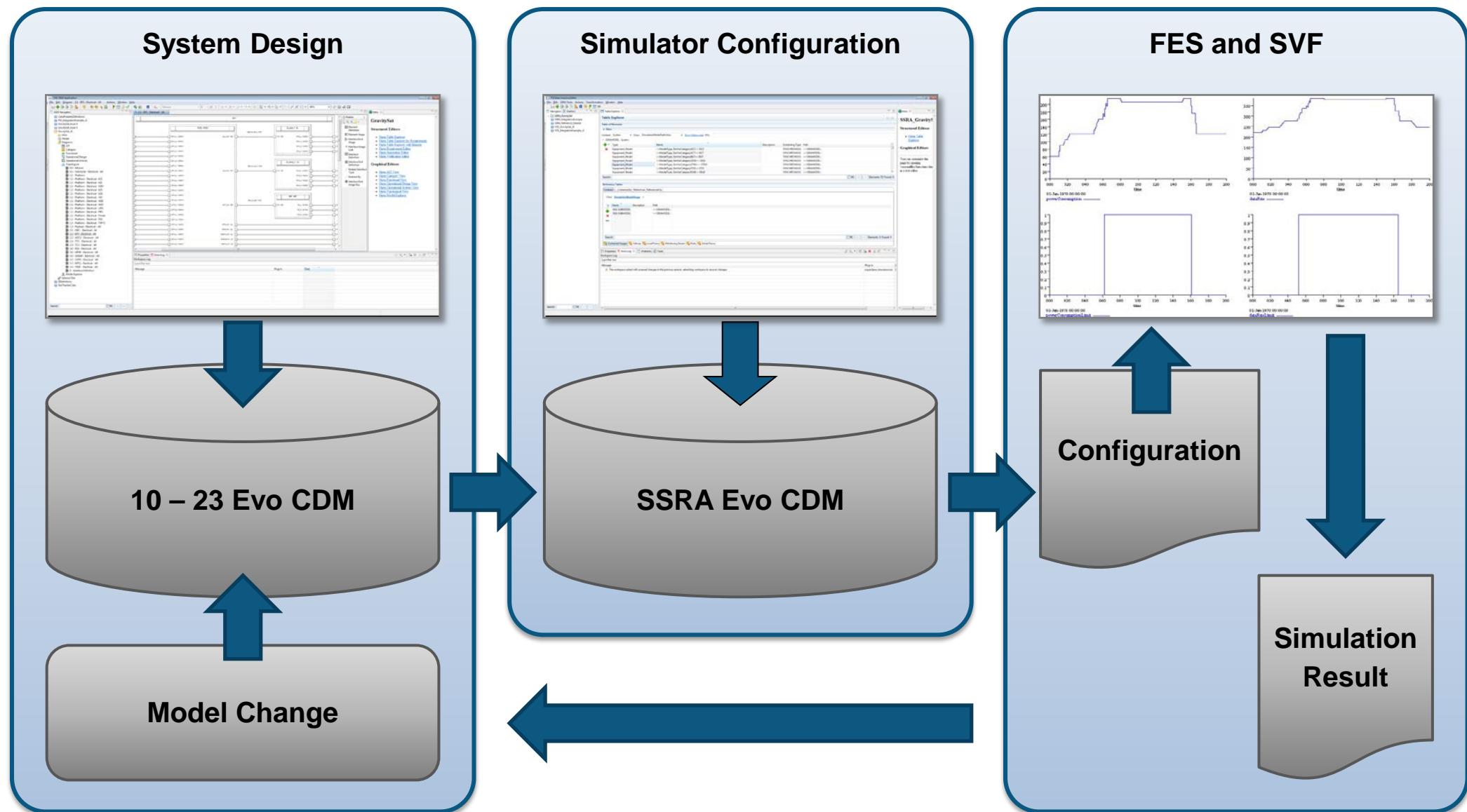
Scenarios Covered generation from System Data in various cases

- Complete FES configuration generation from System Design Data
 - Including FDIR Case with missing Mode in State Machines
 - Including FDIR Case with fixed Mode in State Machines
- Complete SVF configuration generation including Electrical Architecture

GravitySat System Model Overview and Complexity



Functional System Simulation Process Applied to GravitySat

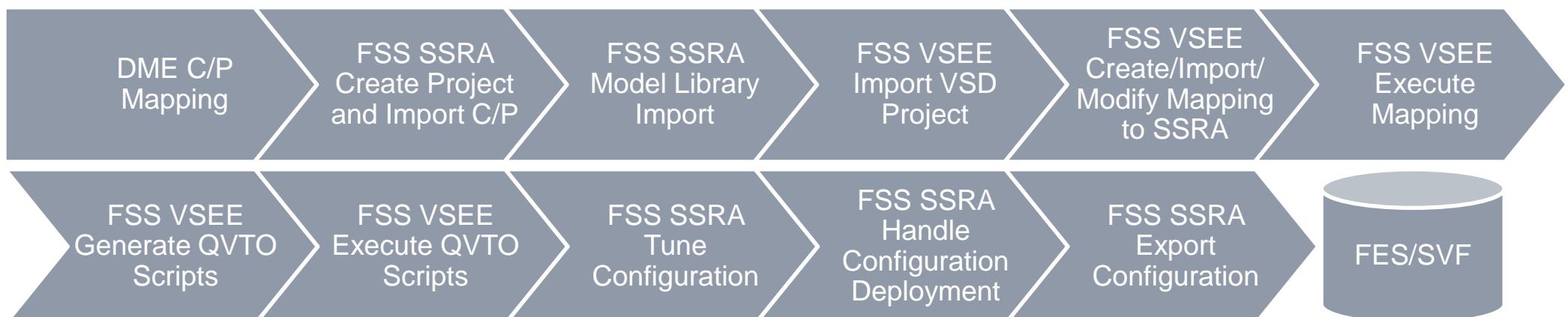


The FSS Process Mapped to Tool Interaction

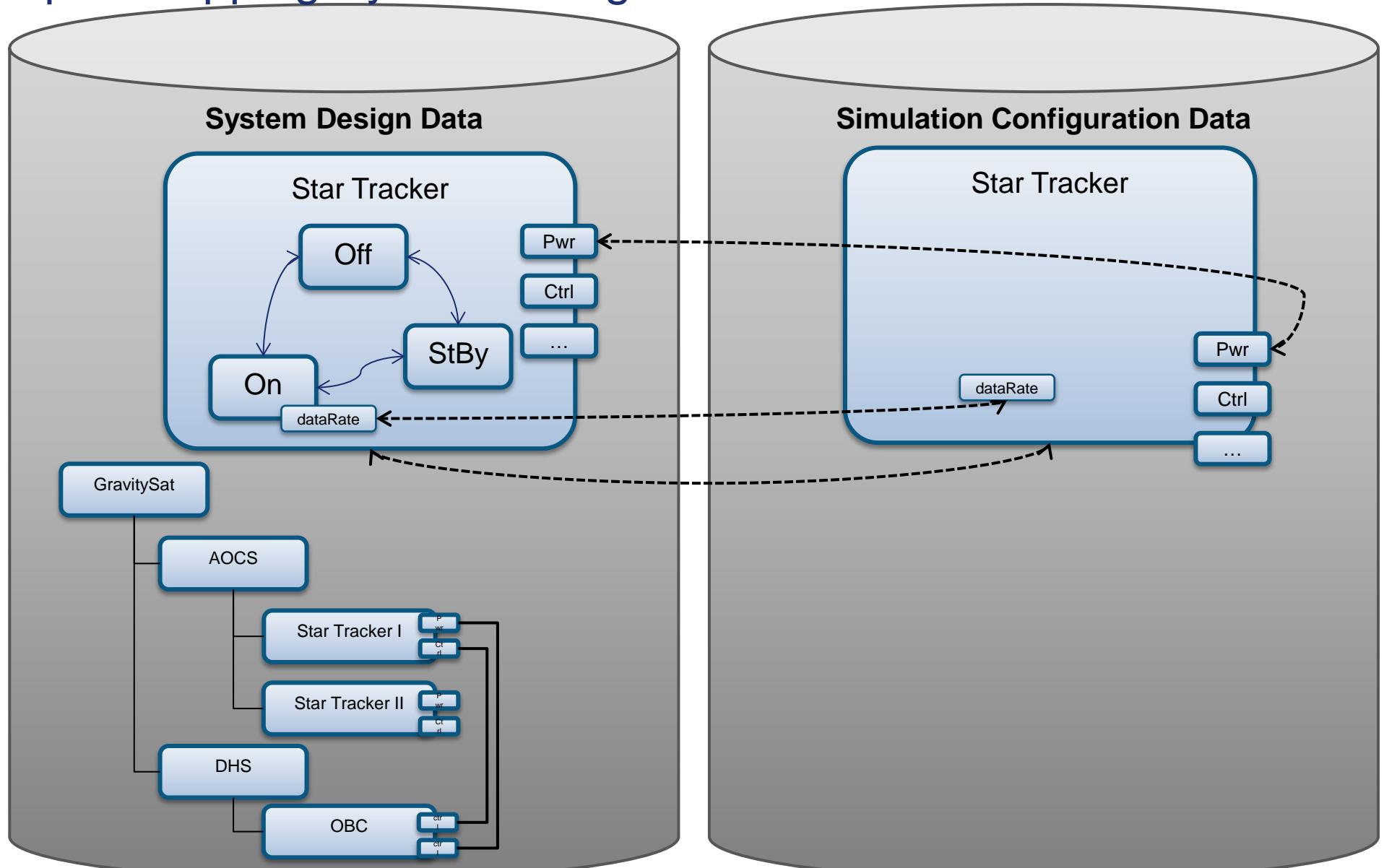
Applying the Functional System Simulation process to the developed tools means

- Precise and re-executable chain of steps to interact with tools and data
- Reuse of existing models and individual re-execution of individual steps

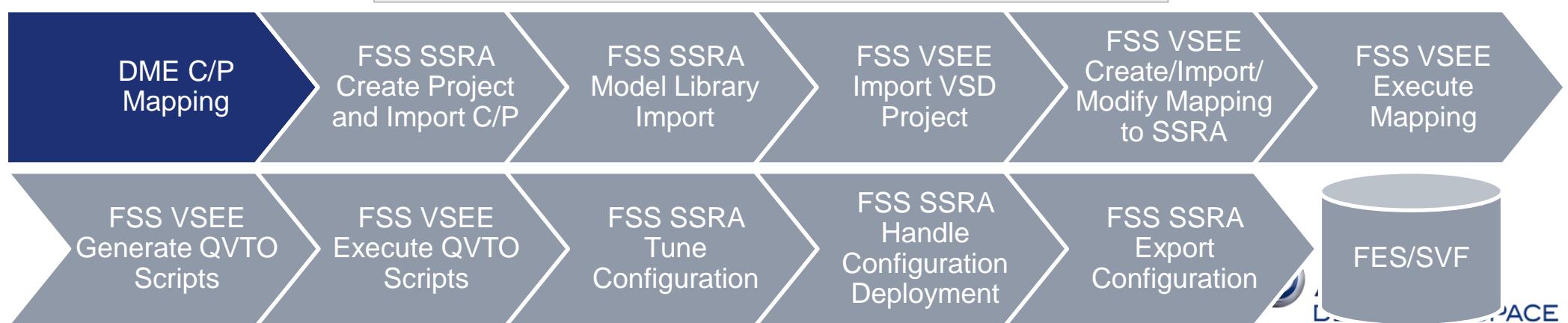
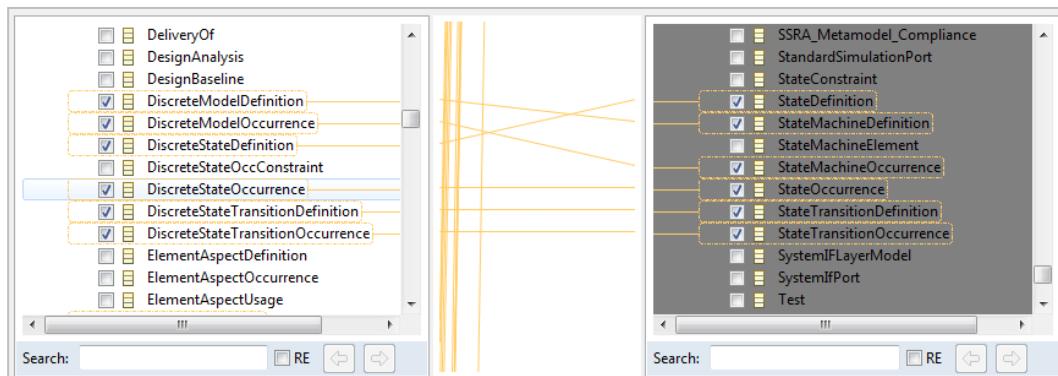
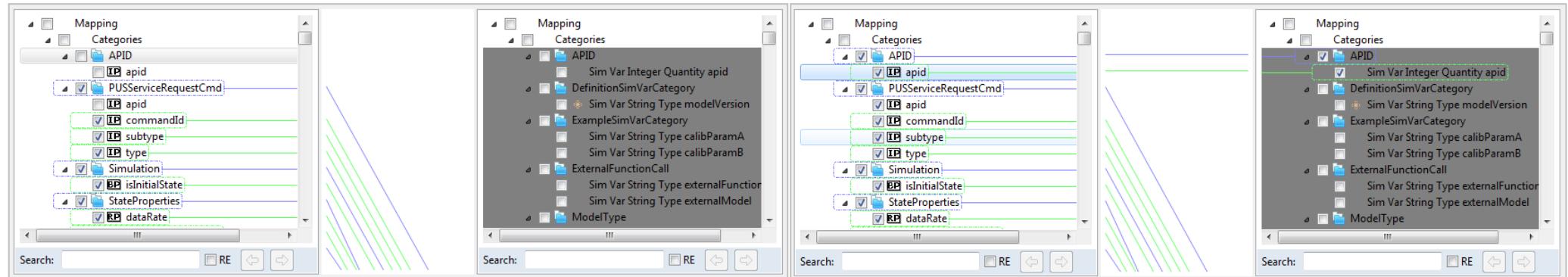
→ Time Saving ... Just several minutes to regenerate simulator configuration after change.



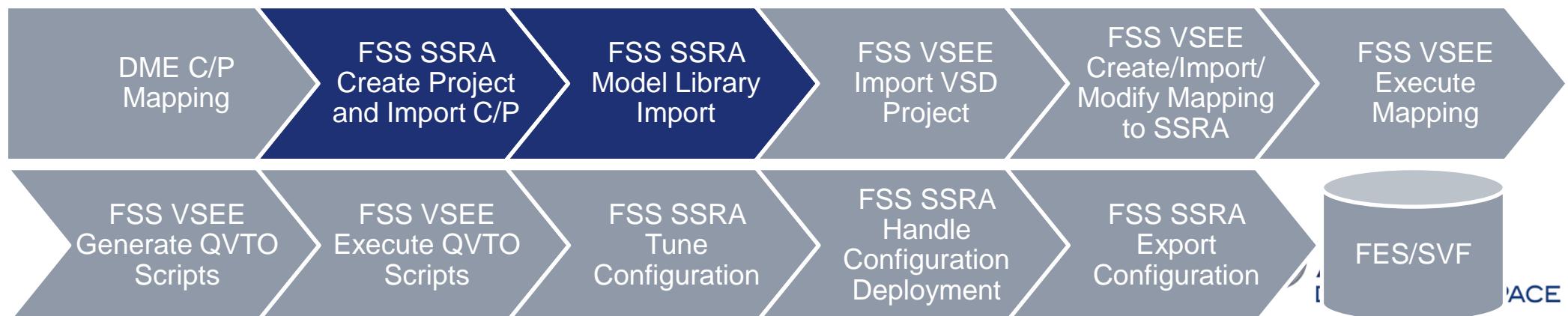
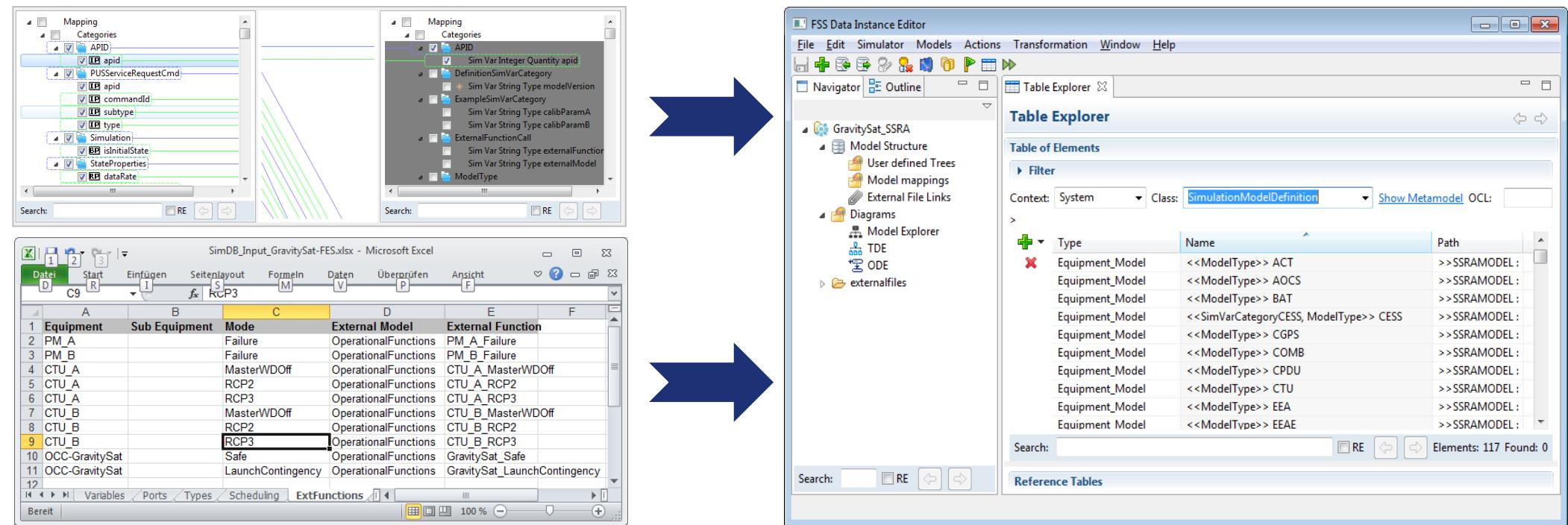
Example: Mapping System Design Information to Simulation Model



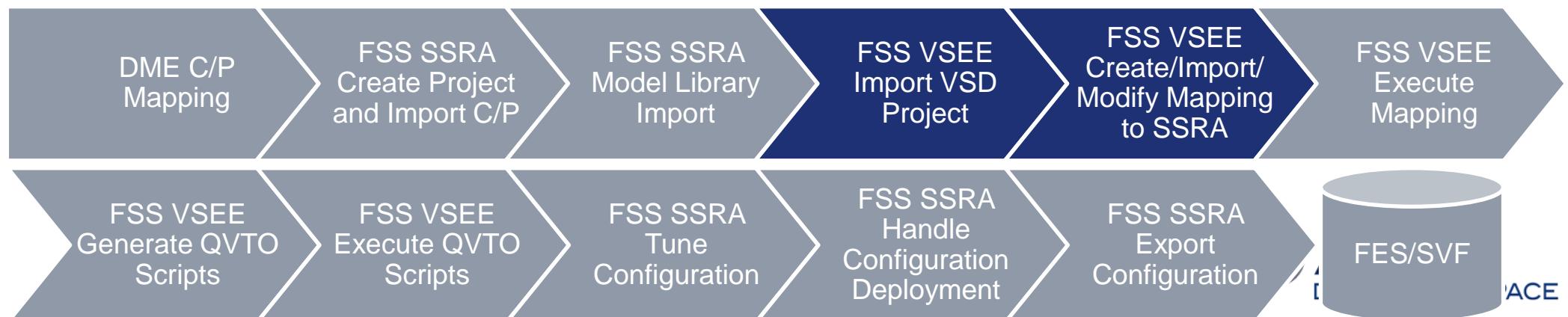
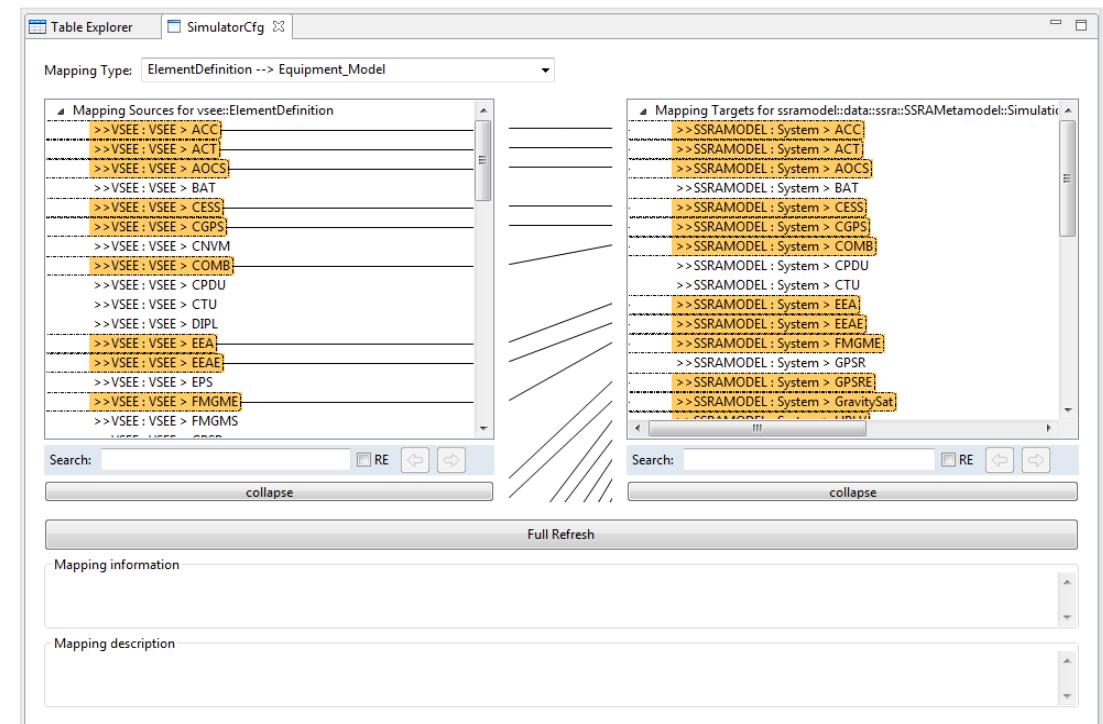
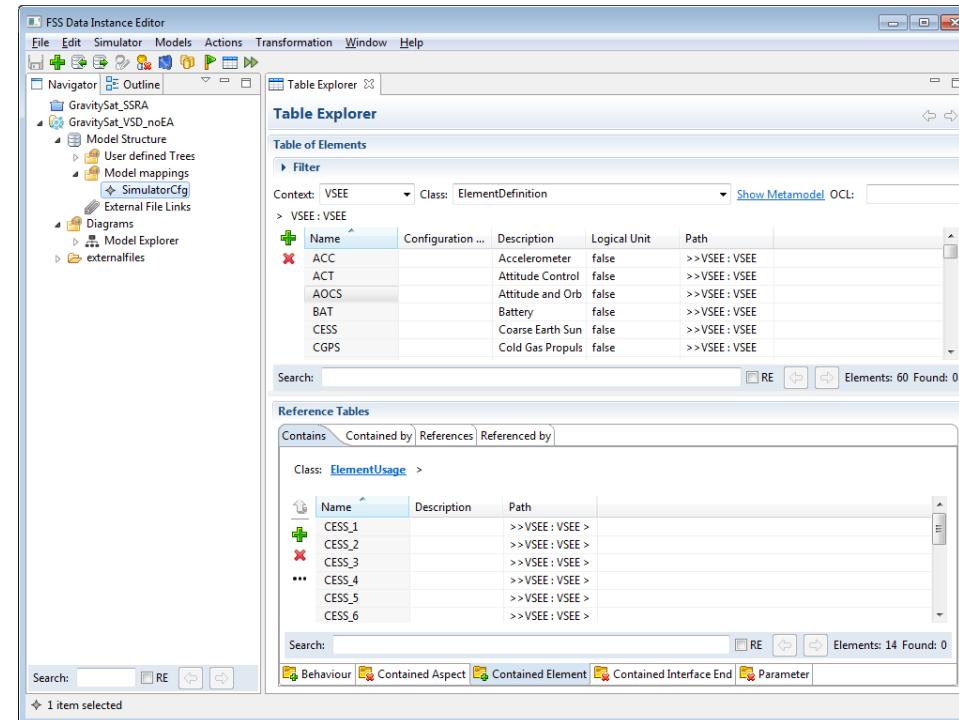
Mapping the CDM 10-23 Evo to SSRA Evo and Categories and Prop.



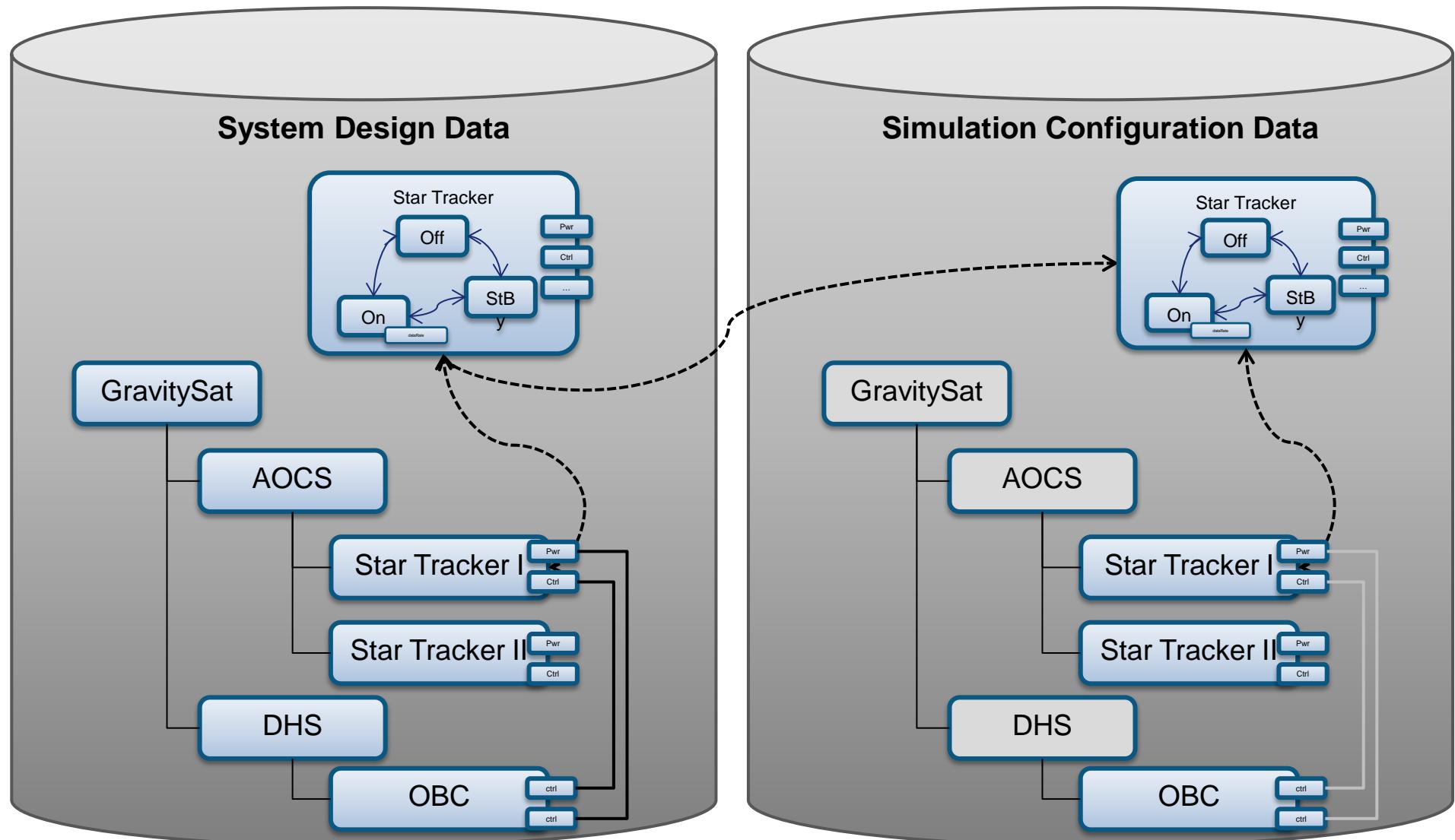
Initial Import of Simulation Models to Simulation Configuration Data



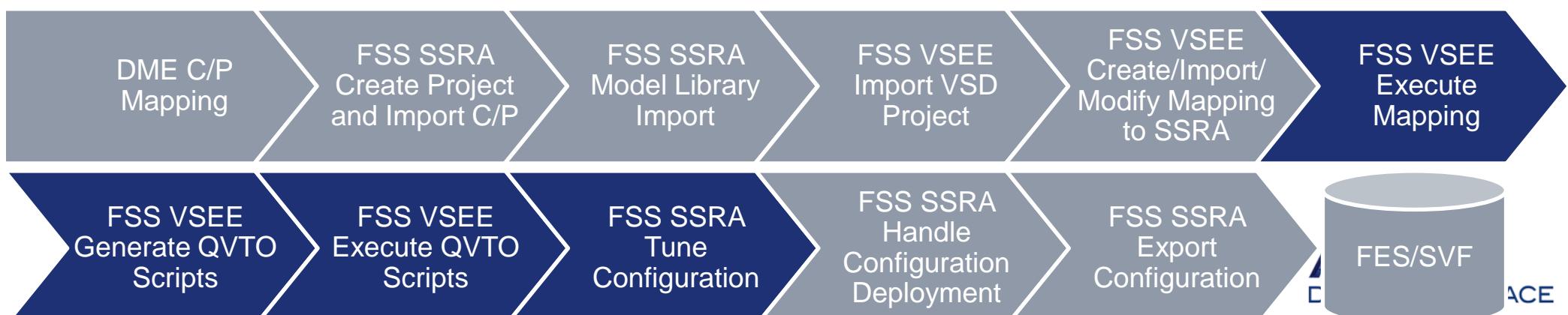
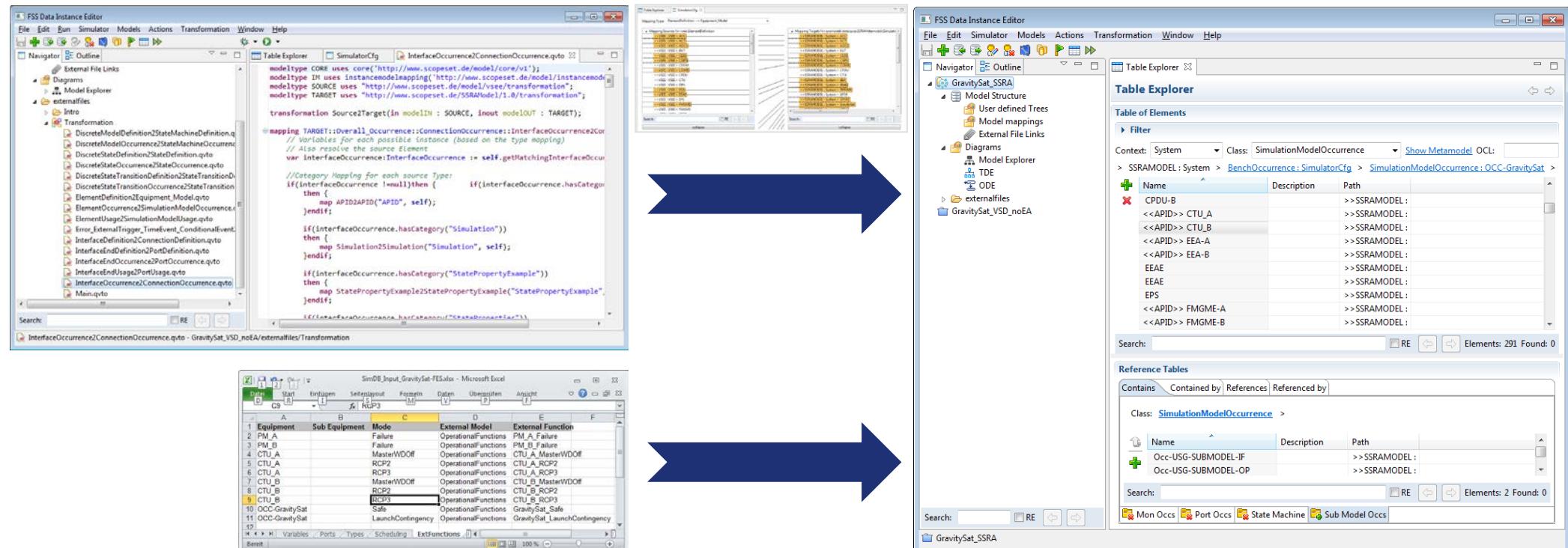
Import of VSD Authored Project and Mapping to Simulation Models



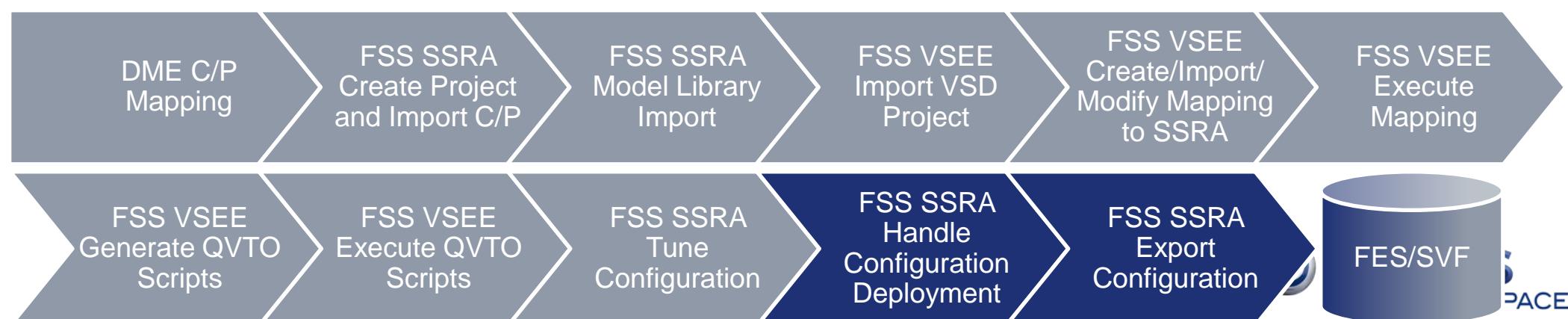
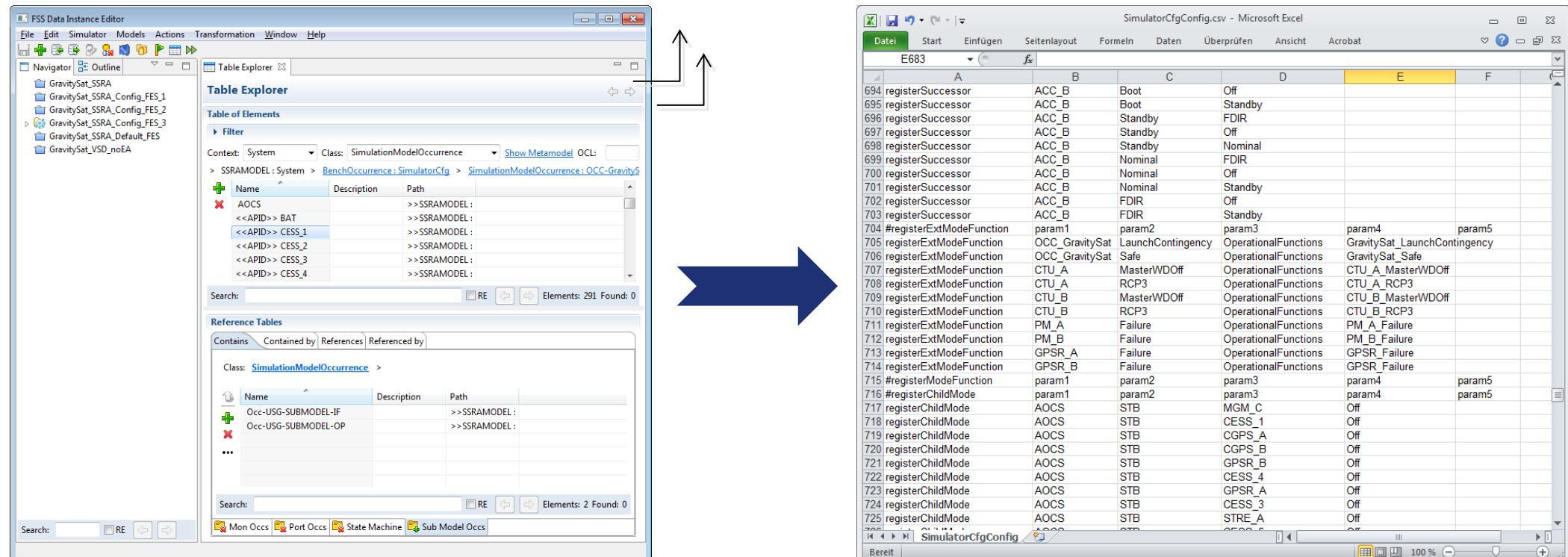
Example: Generating Simulator Configuration



Generate full SSRA Instance Model with Synchronization Tools



Manage Configuration Data and Execute Specific Export



Steps to Re-Execute when Introducing Missing State

SimulatorCfgConfig.csv - Microsoft Excel

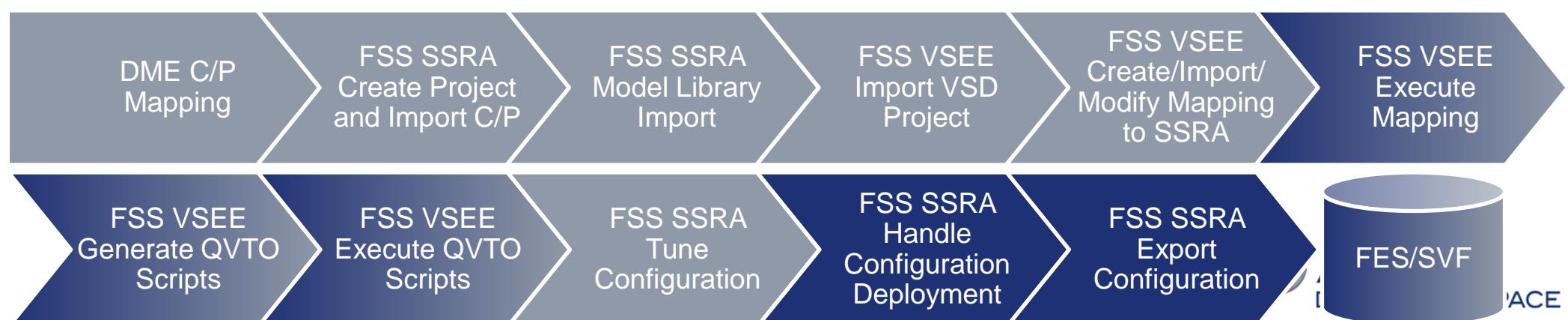
	A	B	C	D
565	registerSuccessor	OBC	FailRunA	Startup
566	registerSuccessor	OBC	FailRunB	RunA
567	registerSuccessor	OBC	FailRunB	Startup
568	registerSuccessor	CTU_A	MasterWDOn	MasterWDOFF
569	registerSuccessor	CTU_A	MasterWDOn	SLAVE
570	registerSuccessor	CTU_A	MasterWDOn	Failure
571	registerSuccessor	CTU_A	MasterWDOFF	Failure
572	registerSuccessor	CTU_A	MasterWDOFF	MasterWDOn
573	registerSuccessor	CTU_A	RCP3	SLAVE
574	registerSuccessor	CTU_A	SLAVE	MasterWDOn
575	registerSuccessor	CTU_A	Failure	SLAVE
576	registerSuccessor	CTU_A	MasterWDOFF	RCP2
577	registerSuccessor	CTU_A	RCP2	RCP3
578	registerSuccessor	CTU_B	MasterWDOn	MasterWDOFF
579	registerSuccessor	CTU_B	MasterWDOn	SLAVE
580	registerSuccessor	CTU_B	MasterWDOn	Failure
581	registerSuccessor	CTU_B	MasterWDOFF	Failure
582	registerSuccessor	CTU_B	MasterWDOFF	MasterWDOn
583	registerSuccessor	CTU_B	RCP3	SLAVE
584	registerSuccessor	CTU_B	SLAVE	MasterWDOn
585	registerSuccessor	CTU_B	Failure	SLAVE
586	registerSuccessor	CTU_B	MasterWDOFF	RCP2
587	registerSuccessor	CTU_B	RCP2	RCP3
588	registerSuccessor	MM_TM_A	Enabled	Disabled
589	registerSuccessor	MM_TM_A	Disabled	Enabled
590	registerSuccessor	MM_TM_B	Enabled	Disabled
591	registerSuccessor	MM_TM_B	Disabled	Enabled

SimulatorCfgConfig.csv - TortoiseMerge

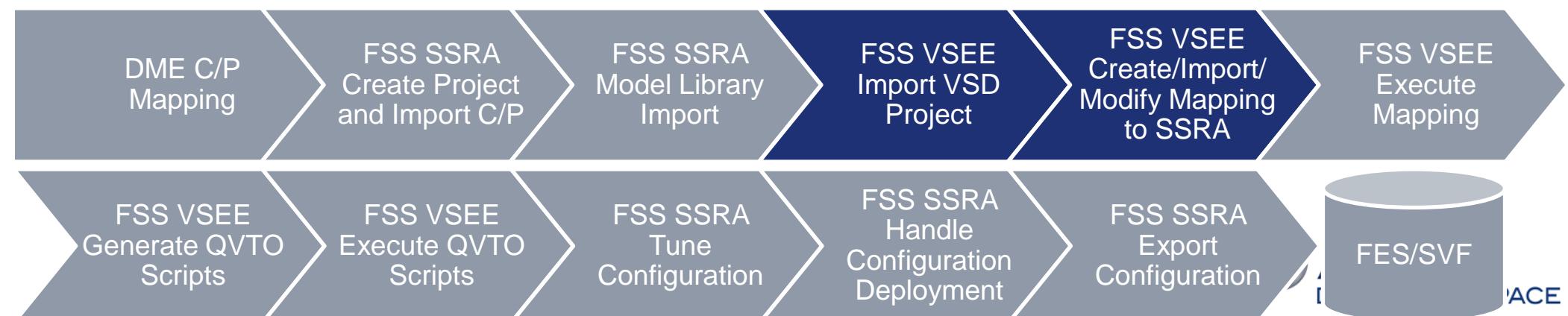
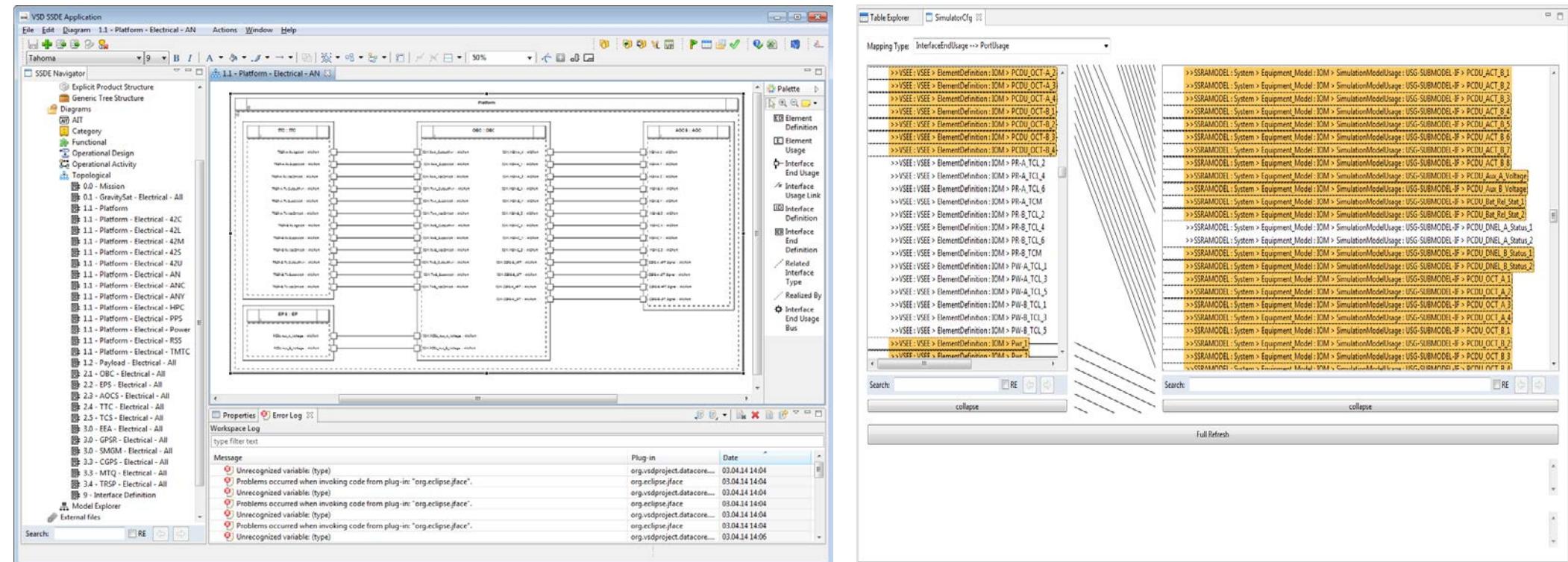
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Main
File Edit Navigate View Style Help
Open Save Save as Enable Edit Use Blocks Create patch file Previous difference Next difference Previous conflict Next conflict Previous inline difference Next inline difference Show Whitespaces Wrap long lines Inline diff Inline diff word-wise
SimulatorCfgConfigFix.csv
571 registerSuccessor;CTU_A;MasterWDOff;Failure;;;
572 registerSuccessor;CTU_A;MasterWDOff;MasterWDOn;;
573 registerSuccessor;CTU_A;RCP3;SLAVE;;
574 registerSuccessor;CTU_A;SLAVE;MasterWDOn;;
575 registerSuccessor;CTU_A;Failure;SLAVE;;
576 registerSuccessor;CTU_A;MasterWDOff;RCP2;;
577 registerSuccessor;CTU_A;RCP2;RCP3;;
578 registerSuccessor;CTU_B;MasterWDOn;MasterWDOff;;
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580 registerSuccessor;CTU_B;MasterWDOn;Failure;;
581 registerSuccessor;CTU_B;MasterWDOff;Failure;;
582 registerSuccessor;CTU_B;MasterWDOff;MasterWDOn;;
583 registerSuccessor;CTU_B;RCP3;SLAVE;;
584 registerSuccessor;CTU_B;SLAVE;MasterWDOn;;
585 registerSuccessor;CTU_B;Failure;SLAVE;;
586 registerSuccessor;CTU_B;MasterWDOff;RCP2;;
587 registerSuccessor;CTU_B;RCP2;RCP3;;
588 registerSuccessor;MM_TM_A;Enabled;Disabled;;
589 registerSuccessor;MM_TM_A;Disabled;Enabled;;
590 registerSuccessor;MM_TM_B;Enabled;Disabled;;
591 registerSuccessor;MM_TM_B;Disabled;Enabled;;
registerSuccessor;CTU_A;MasterWDOff;RCP2;;
registerSuccessor;CTU_A;MasterWDOff;RCP3;;
For Help, press F1. Scroll horizontally with Ctrl-Scrollwheel
Left View: ASCII CRLF / -16 Right View: ASCII CRLF / +4 Conflicts: 0 CAP NUM
SimulatorCfgConfig.csv
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567 registerSuccessor;CTU_A;RCP3;SLAVE;;
568 registerSuccessor;CTU_A;SLAVE;MasterWDOn;;
569 registerSuccessor;CTU_A;Failure;SLAVE;;
570 registerSuccessor;CTU_A;MasterWDOff;RCP3;;
571 registerSuccessor;CTU_B;MasterWDOn;MasterWDOff;;
572 registerSuccessor;CTU_B;MasterWDOn;SLAVE;;
573 registerSuccessor;CTU_B;MasterWDOn;Failure;;
574 registerSuccessor;CTU_B;MasterWDOff;Failure;;
575 registerSuccessor;CTU_B;MasterWDOff;MasterWDOn;;
576 registerSuccessor;CTU_B;RCP3;SLAVE;;
577 registerSuccessor;CTU_B;SLAVE;MasterWDOn;;
578 registerSuccessor;CTU_B;Failure;SLAVE;;
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580 registerSuccessor;MM_TM_A;Enabled;Disabled;;
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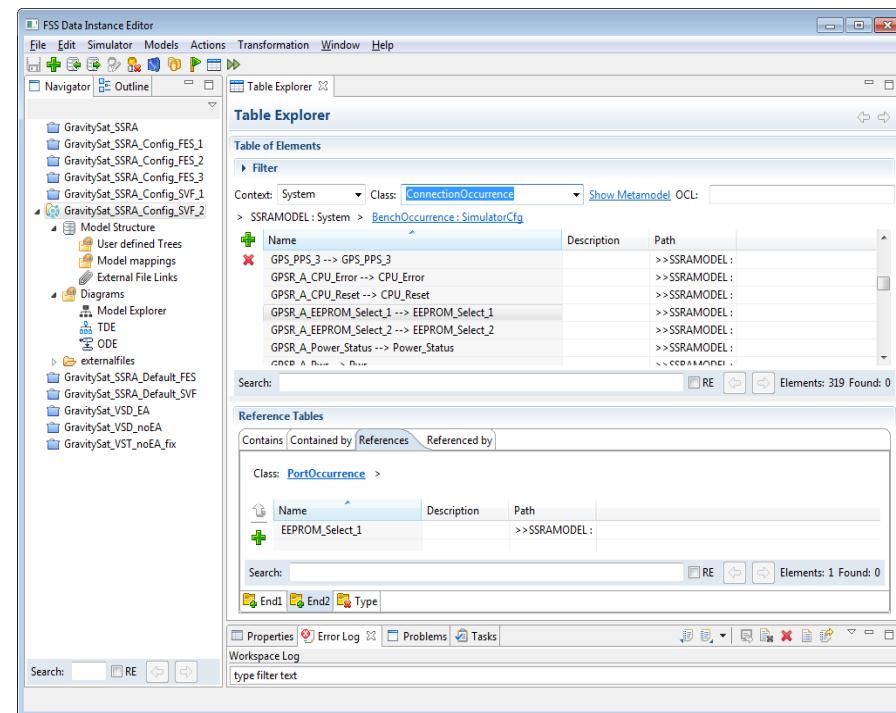
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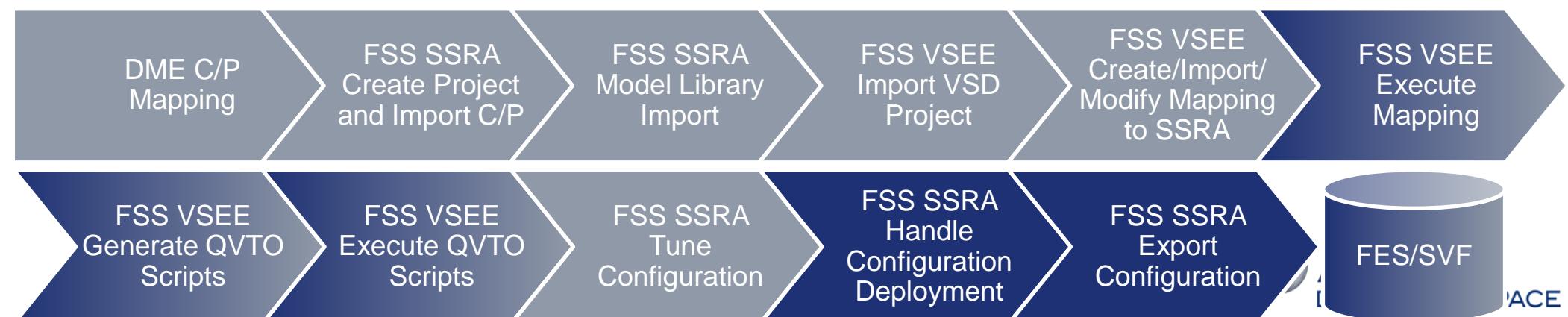
Extending the FES Mapping to Work for SVF Configurations



Steps to Re-Execute to Fix Issues on Electrical Architecture

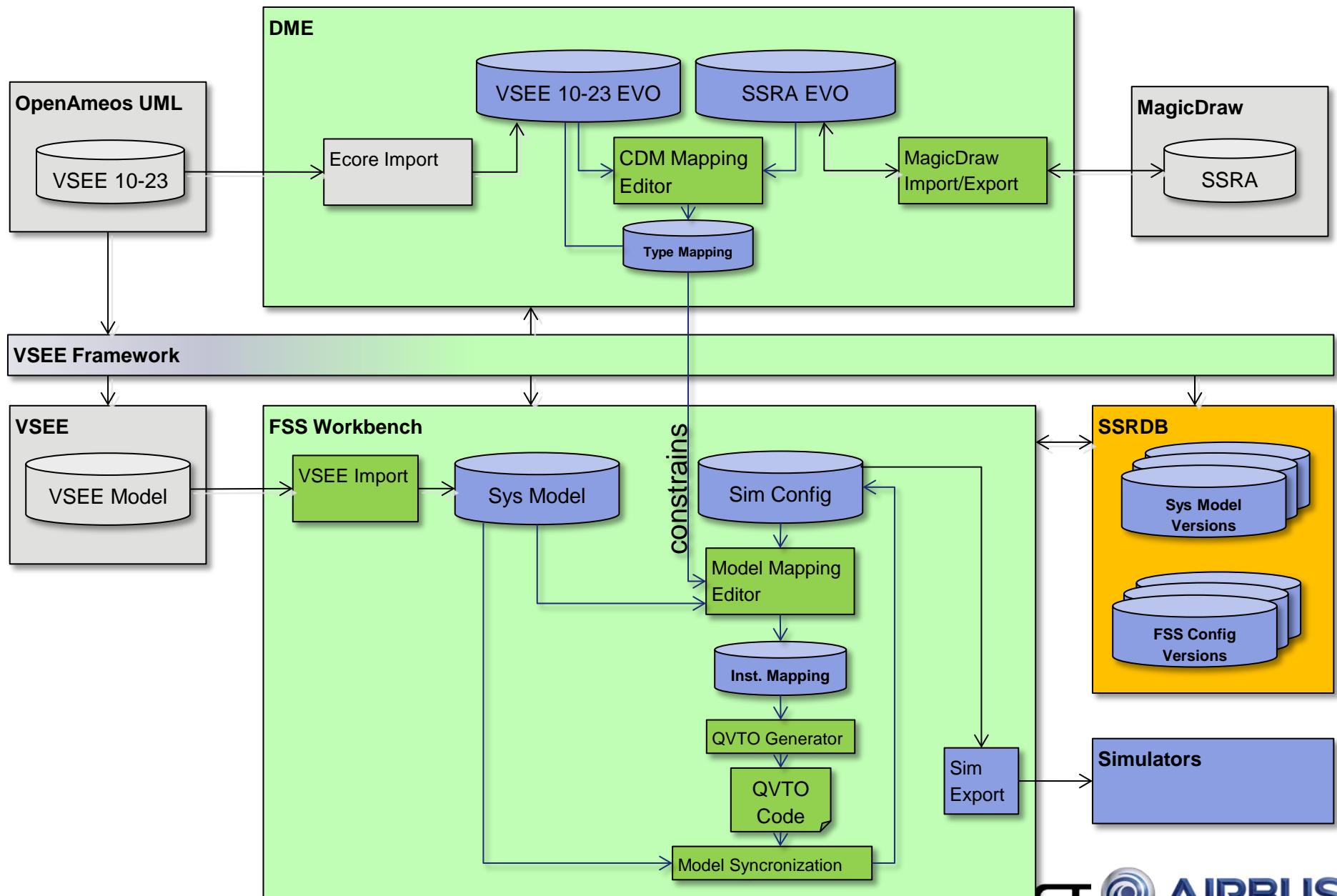


	A	B	C	D	E	F
	Name	Description	Type	Source	Target	Slot
1	Spalte1		Spalte2	Spalte3	Spalte4	Spalte5
246	ACC_PPS_to_SYS_PPS		HPC	OBC_CTL_B_ACC_PPS	ACC_B_SYS_PPS	
247	STRE_PPS_to_SYS_PPS		HPC	OBC_CTL_B_STRE_PPS	STRE_B_SYS_PPS	
248	SMGM_PPS_to_SYS_PPS		HPC	OBC_CTL_B_SMGM_PPS	SMGM_B_SMGMG_SYS_PPS	
249	EAA_PPS_to_SYS_PPS		HPC	OBC_CTL_B_EEAE_PPS	EAA_B_EEAE_SYS_PPS	
250	FMCME_PPS_to_SYS_PPS		HPC	OBC_CTL_B_FMCME_PPS	FMCME_B_SYS_PPS	
251	GPS_PPS_1_to_GPS_PPS_1		HPC	OBC_CTL_B_GPS_PPS_1	GPSR_B_GPSRE_GPS_PPS_1	
252	GPS_PPS_2_to_GPS_PPS_2		HPC	OBC_CTL_B_GPS_PPS_2	GPSR_B_GPSRE_GPS_PPS_2	
253	GPS_PPS_3_to_GPS_PPS_3		HPC	OBC_CTL_B_GPS_PPS_3	GPSR_B_GPSRE_GPS_PPS_3	
254	GPSRE_On_1_to_On_1		HPC	OBC_CTL_B_GPSRE_On_1	GPSR_B_GPSRE_On_1	
255	GPSRE_On_2_to_On_2		HPC	OBC_CTL_B_GPSRE_On_2	GPSR_B_GPSRE_On_2	
256	ACC_Off_1_to_Off_1		HPC	OBC_CTL_B_ACC_Off_1	ACC_B_Off_1	
257	ACC_Off_2_to_Off_2		HPC	OBC_CTL_B_ACC_Off_2	ACC_B_Off_2	
258	ACC_On_1_to_On_1		HPC	OBC_CTL_B_ACC_On_1	ACC_B_On_1	
259	ACC_On_2_to_On_2		HPC	OBC_CTL_B_ACC_On_2	ACC_B_On_2	
260	EEAE_Off_1_to_Off_1		HPC	OBC_CTL_B_EEAE_Off_1	EAA_B_EEAE_Off_1	
261	EEAE_Off_2_to_Off_2		HPC	OBC_CTL_B_EEAE_Off_2	EAA_B_EEAE_Off_2	
262	EEAE_On_1_to_On_1		HPC	OBC_CTL_B_EEAE_On_1	EAA_B_EEAE_On_1	
263	EEAE_On_2_to_On_2		HPC	OBC_CTL_B_EEAE_On_2	EAA_B_EEAE_On_2	
264	GPSRE_Off_1_to_Off_1		HPC	OBC_CTL_B_GPSRE_Off_1	GPSR_B_GPSRE_Off_1	
265	GPSRE_Off_2_to_Off_2		HPC	OBC_CTL_B_GPSRE_Off_2	GPSR_B_GPSRE_Off_2	
266	EEA_B_Boot_Loader_Select_to_Boot_Loader_Select		Digital	OBC_IOM_EEA_B_Boot_Loader_Select	EAA_A_EEAE_Boot_Loader_Select	
267	EEA_B_Boot_Loader_Select_to_Boot_Loader_Select		Digital	OBC_IOM_EEA_B_Boot_Loader_Select	EAA_A_EEAE_Boot_Loader_Select	
268	EEA_B_Watchdog_Status_to_Watchdog_Status		Digital	OBC_IOM_EEA_A_Watchdog_Status	EAA_A_EEAE_Watchdog_Status	
269	EEA_B_Watchdog_Status_to_Watchdog_Status		Digital	OBC_IOM_EEA_B_Watchdog_Status	EAA_B_EEAE_Watchdog_Status	
270	GPSR_A_CPU_Error_to_CPU_Error		Digital	OBC_IOM_GPSR_A_CPU_Error	GPSR_A_GPSRE_CPU_Error	
271	GPSR_A_CPU_Reset_to_CPU_Reset		Digital	OBC_IOM_GPSR_A_CPU_Reset	GPSR_A_GPSRE_CPU_Reset	
272	GPSR_A_Power_Status_to_Power_Status		Digital	OBC_IOM_GPSR_A_Power_Status	GPSR_A_GPSRE_Power_Status	
273	GPSR_B_CPU_Error_to_CPU_Error		Digital	OBC_IOM_GPSR_B_CPU_Error	GPSR_B_GPSRE_CPU_Error	
274	GPSR_B_CPU_Reset_to_CPU_Reset		Digital	OBC_IOM_GPSR_B_CPU_Reset	GPSR_B_GPSRE_CPU_Reset	
275	GPSR_B_Power_Status_to_Power_Status		Digital	OBC_IOM_GPSR_B_Power_Status	GPSR_B_GPSRE_Power_Status	
276	ACC_A_UART_1_to_UART_1		Serial	OBC_IOM_ACC_A_UART_1	ACC_A_UART_1	
277	ACC_A_UART_2_to_UART_2		Serial	OBC_IOM_ACC_A_UART_2	ACC_A_UART_2	
278	ACC_A_UART_3_to_UART_3		Serial	OBC_IOM_ACC_A_UART_3	ACC_A_UART_3	

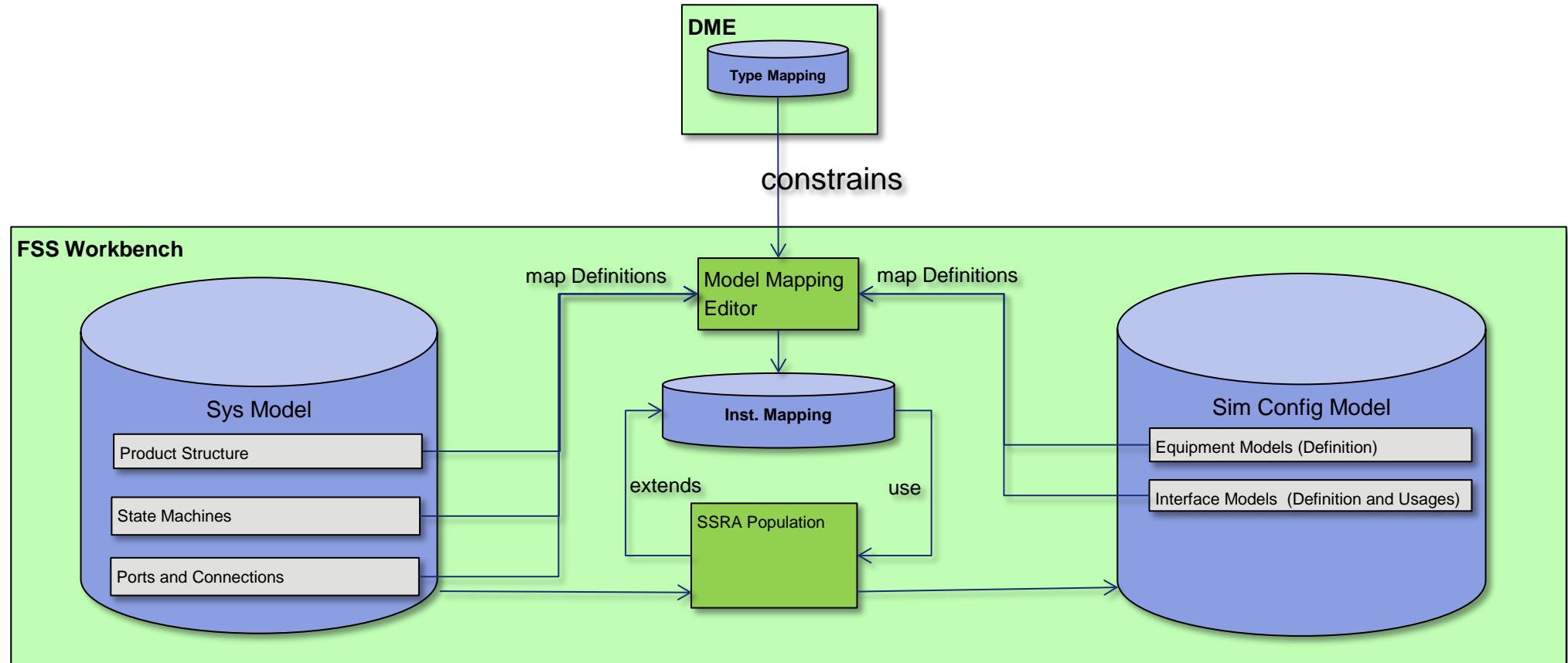


Tools and Technical Backbone of the Study

Complete Tools Overview as in Functional System Simulation



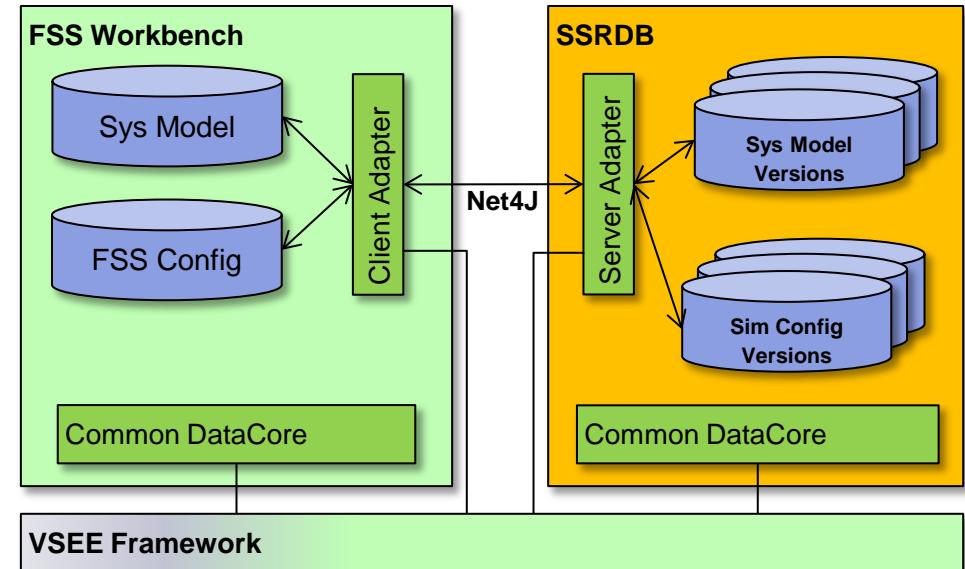
Type Mapping and Instance Mapping for Model Population



SSRDB as Configuration Control Tool for both Models

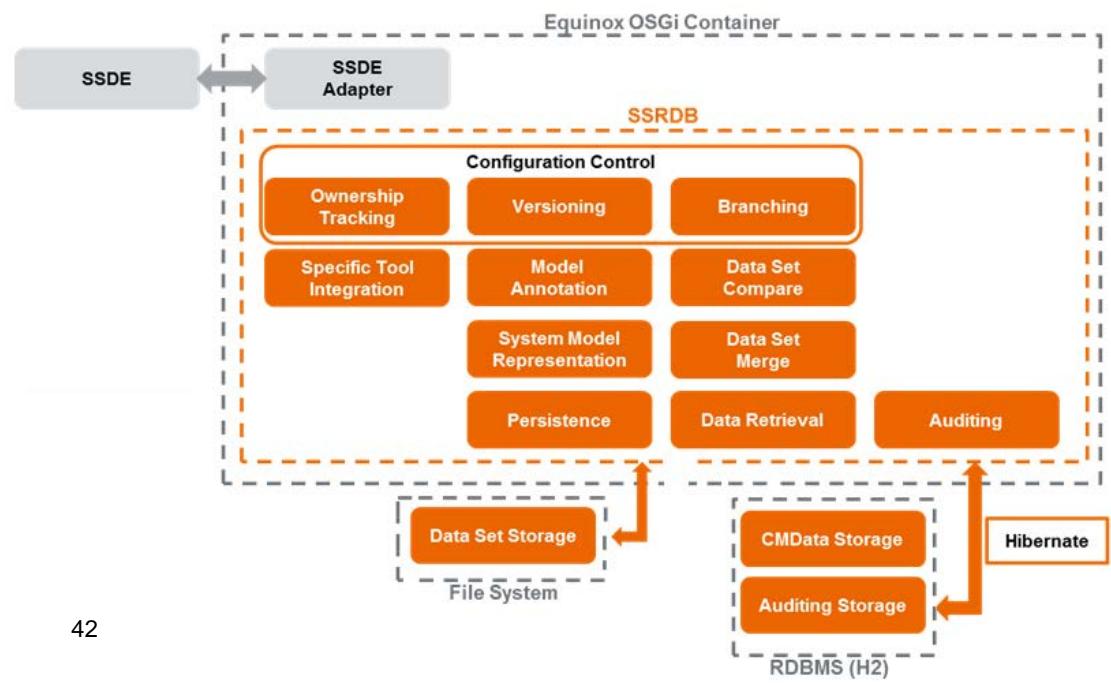
SSRDB as heritage from VSD has to evolve

- Has to handle two data models for 10-23 Evo and SSRA Evo
- Different Approaches have been discussed:
 - Solution: one SSRDB Instance maintaining both models



Tools Integration and Infrastructure

- Editors provide Adapters to SSRDB interface
- Harmonized Infrastructure using Eclipse (OSGi)
 - allows easy deployment
- Main SSRD plugins independant from data model



Summary

First step jumping the gap of system model and functional simulation

- (Semi-) automated transformation of data from system model to functional simulation model
 - Based on the different CDMs (system and simulation) the both representations can be properly related
 - The relation / mapping can be used to derive transformation scripts
 - Complementary data needed for simulation can be integrated on simulation database
→ Dependency management needed for ownership tracking and impact analysis
- Functional OBC / FSW model allow the automated configuration from system model
 - Functional OBC model can be populated from system model with i.e. the operational concept
→ More work needed to further advance functional OBC model allow to identify shortcomings in spec
- Co-management of system data and simulation data along the life-cycle
 - Decomposition of data into data sets, per managed process - equivalent functionally available for each data set
 - Modularization of data models which can be managed
 - “Growing” of simulator from FES into SVF is ensured since FES is derived from SVF
→ Update of simulation model structure needed
- Closing the loop from system model, simulation execution, run evaluation, derivation of required changes, system model update
 - The chain from system model into simulation model is closed and automated
→ The link back requires improved representation of the decision making process → annotations, tickets

End of Presentation