TEC-SW Final Presentation Days 2014

OBC Simulator Architectures and Interfaces to System Test Benches / leonSVF

GSTP + StrIn + Lab Investment

Technical Officer : Mauro CALENO (TEC-SW)
Prime : Grégory QUERE (AIRBUS Defence & Space, Toulouse France)
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Consultant : Ingespace SARL (Toulouse France)

9th December 2014

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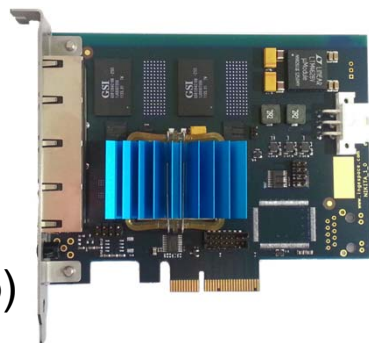# Leon Emulator Board: a hybrid processor emulator

Satellite simulation in SW:
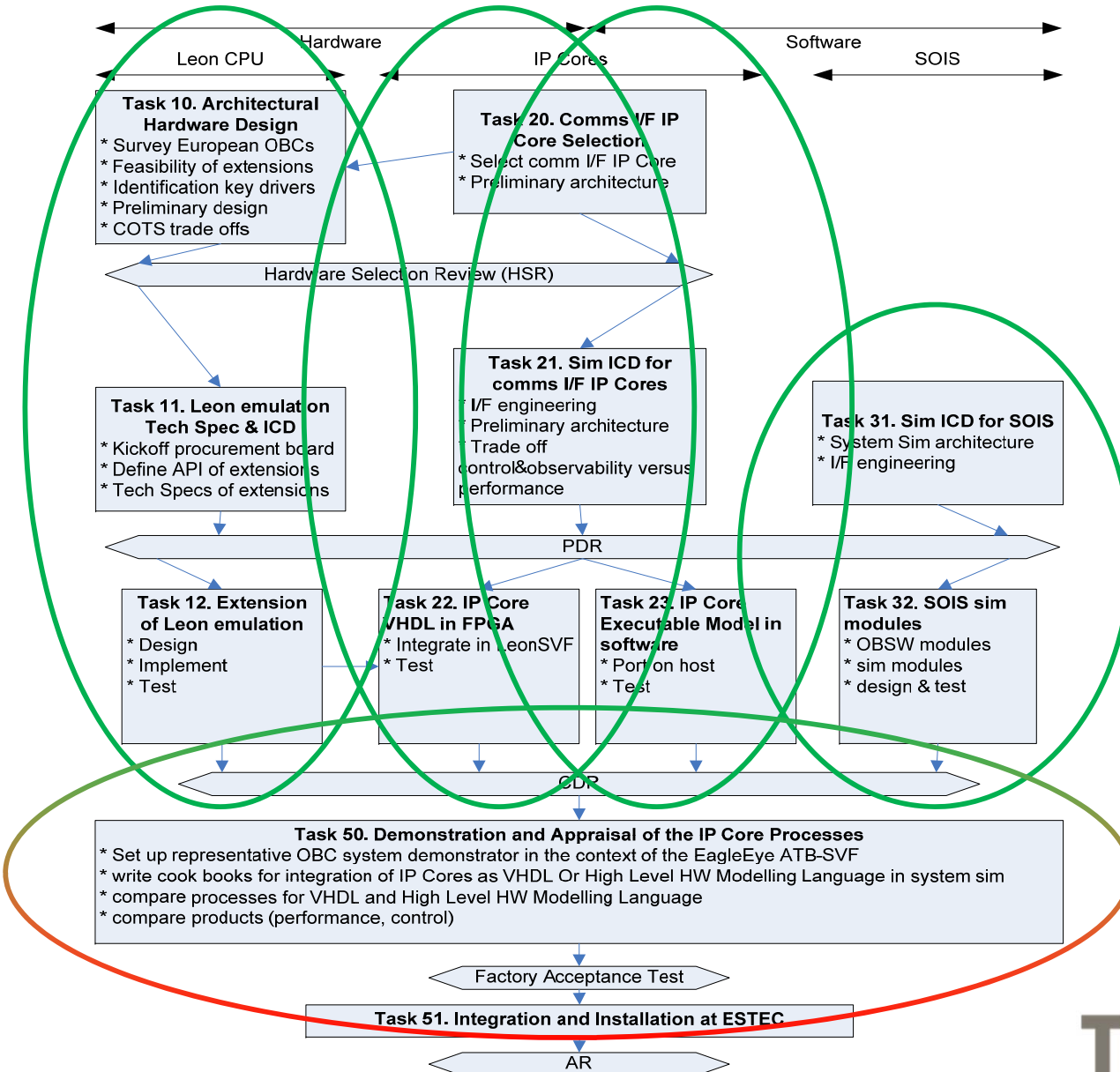- S/C Dynamics
- Units
- OBC
- Leon peripherals

Leon emulation in FPGA

(real VHDL → HW in the loop)

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Project work logic

Hardware — Leon CPU — IP Cores — Software — SOIS

Task 10. Architectural Hardware Design
* Survey European OBCs
* Feasibility of extensions
* Identification key drivers
* Preliminary design
* COTS trade offs

Task 20. Comms I/F IP Core Selection
* Select comm I/F IP Core
* Preliminary architecture

Hardware Selection Review (HSR)

Task 21. Sim ICD for comms I/F IP Cores
* I/F engineering
* Preliminary architecture
* Trade off control&observability versus performance

Task 31. Sim ICD for SOIS
* System Sim architecture
* I/F engineering

Task 11. Leon emulation Tech Spec & ICD
* Kickoff procurement board
* Define API of extensions
* Tech Specs of extensions

PDR

Task 12. Extension of Leon emulation
* Design
* Implement
* Test

Task 22. IP Core VHDL in FPGA
* Integrate in LeonSVF
* Test

Task 23. IP Core Executable Model in software
* Port on host
* Test

Task 32. SOIS sim modules
* OBSW modules
* sim modules
* design & test

CDR

Task 50. Demonstration and Appraisal of the IP Core Processes
* Set up representative OBC system demonstrator in the context of the EagleEye ATB-SVF
* write cook books for integration of IP Cores as VHDL Or High Level HW Modelling Language in system sim
* compare processes for VHDL and High Level HW Modelling Language
* compare products (performance, control)

Factory Acceptance Test

Task 51. Integration and Installation at ESTEC

AR

Hybrid Processor Emulation

Hybrid System on Chip Emulation (some IP Cores of SoC in HW)

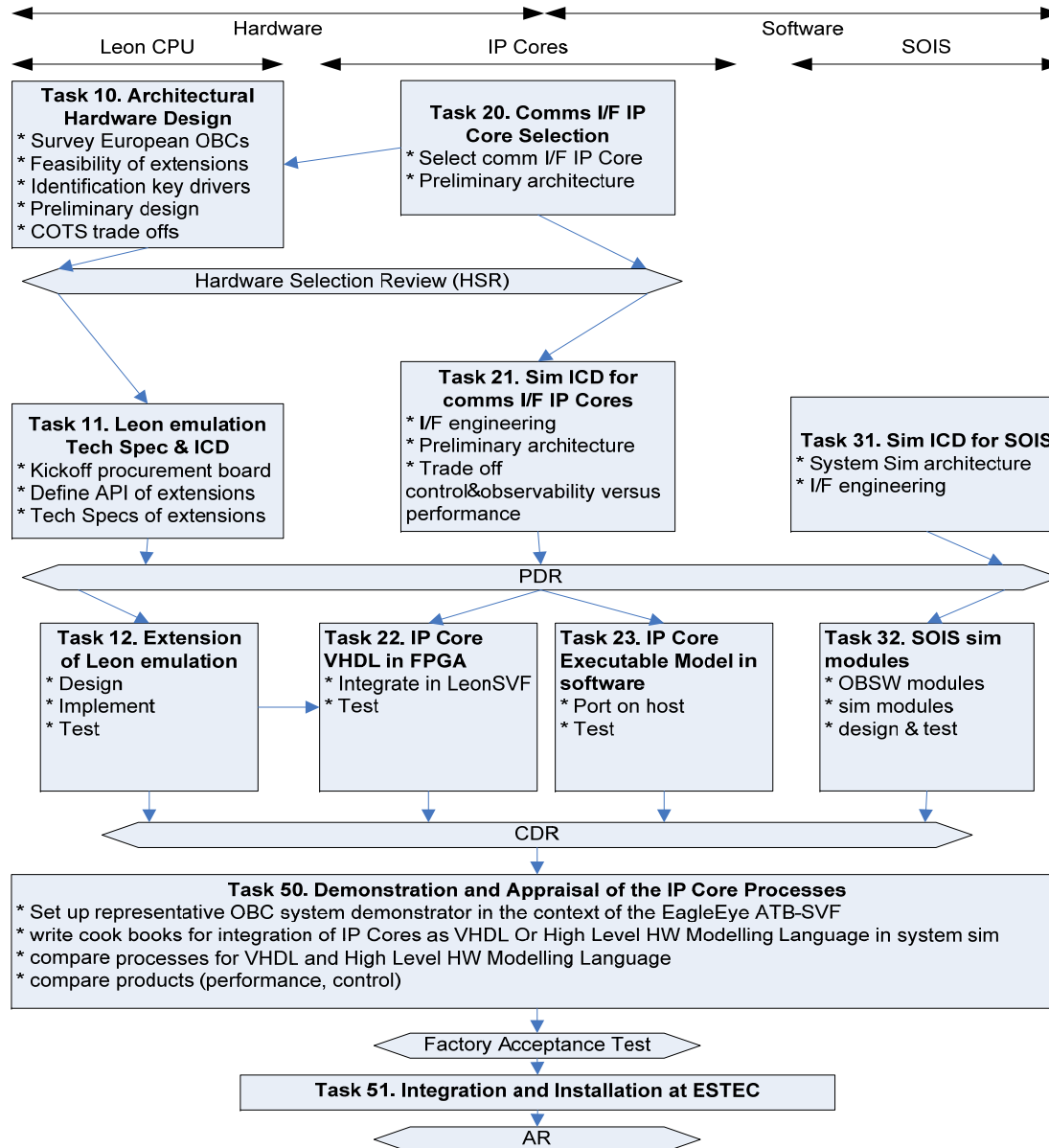Hybrid SoC Emulation (IP Cores of SoC in SW Via HW/SW co-engineering)

No IP Cores of SoC: abstracted at SOIS level

Demonstration:
- EagleEye@Eurosim/SMP2
- SPOT6(SCOC3)@SimTG

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Project work logic

Hardware | **Software**

Leon CPU | IP Cores | SOIS

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Hybrid Processor Emulation

Hybrid System on Chip Emulation
(some IP Cores of SoC in HW)

Hybrid SoC Emulation
(IP Cores of SoC in SW
Via HW/SW co-engineering)

No IP Cores of SoC:
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- EagleEye@Eurosim/SMP2
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Skipping to conclusion : Leon Emulation Board (LEB)

The LEB : a new System on Chip Emulator

- LEON2 & LEON3 emulation

- 100% representative

- Real time OBC Simulation at 60 Mhz+

- Easy to integrate in SVF, FV & Operational simulator

- Easy to Operate

- Works in Eurosim by Airbus DS NL and in the simTG by Airbus DS FR and soon in SIMSAT by Vega

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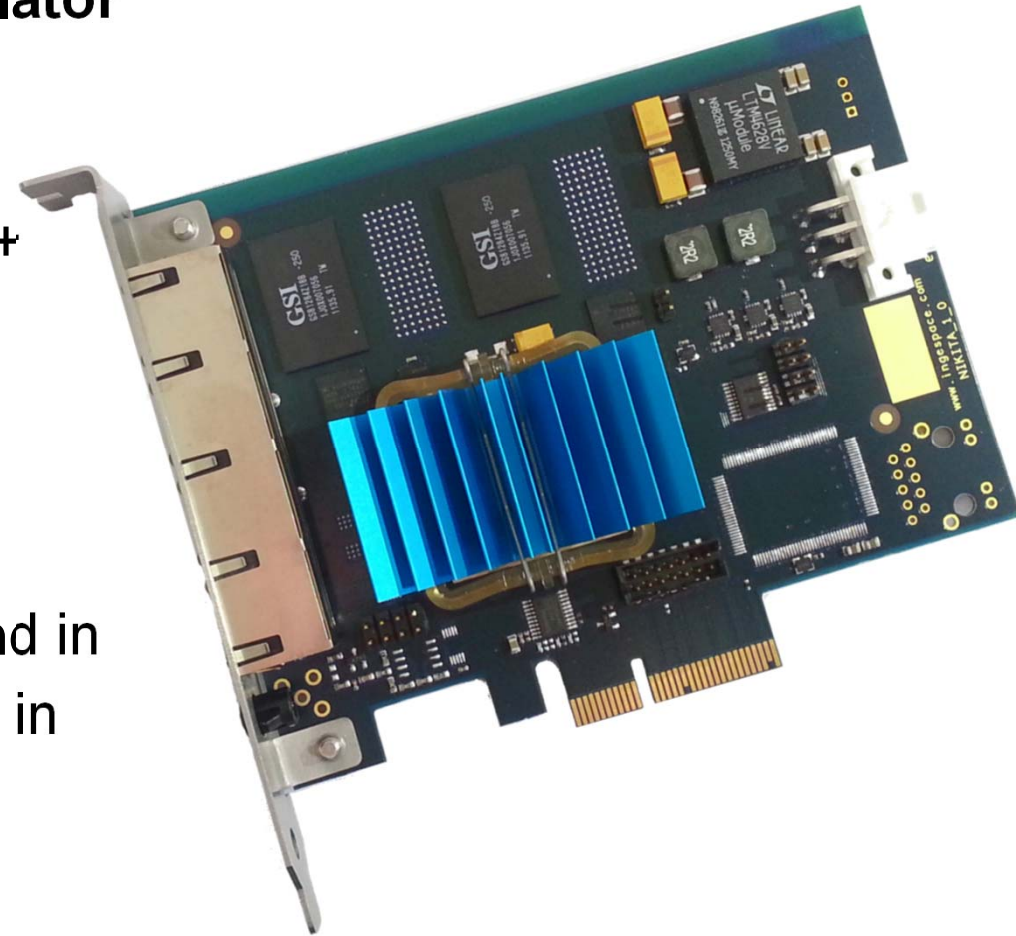
Skipping to conclusion : Leon Emulation Board (LEB)

LEON2 configuration	LEON3 configuration	Airbus SCOC3-inspired configuration (extension of LEON3 design)	Another SoC ?
- Leon2FT@100Mhz - GRFPU	- Leon3@100Mhz - GRFPU	- Leon3@100Mhz - GRFPU - SpW packets ←→ Simulation SW - 2 Amba buses	Leon2FT ? Leon3 ? …

- SRAM & SDRAM Support
- Fast simulation of I/O mapped memories
- SW Simulation on I/O and AMBA bus (APB and AHB)
- LEON UART characters ←→ Simulation SW
- LEON pins ←→ Simulation SW

- Scheduler and Timed Events
- GDB Server
- Save and Restore of simulation contexts
- API TSIM compliant
- Runs in Eurosim, SimTG and SIMSAT (ongoing), on RedHat and SUSE

Eurosim by Airbus DS NL; SimTG by Airbus DS FR; SIMSAT by Telespazio/Vega

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Agenda

1. Context

2. Processor/SoC emulation State of the Art

3. Study History

4. Fundamental principle of Operation

5. Product features

6. Product qualification

7. Performance

8. Product demonstration on EagleEye@EuroSim/SMP2

9. Conclusions

10. How to get an LEB

1. Context

SoC/Processor emulation into Satellite simulation
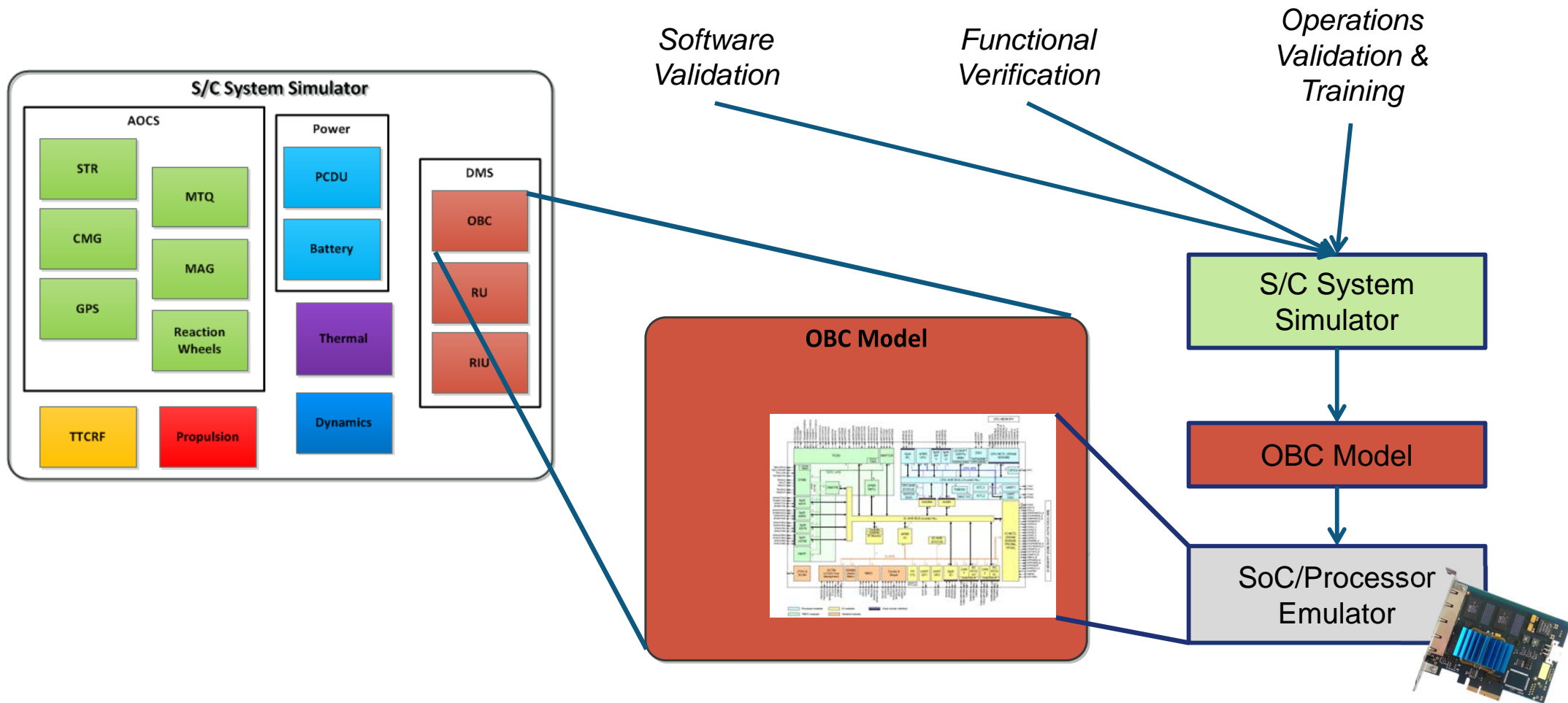
1. Context: LEB in a SW-development team

Unit Testing	Validation	Qualification (Functional Verification)	Acceptance
Dev 1: Luke S.			
Dev 2: O-W K..	...		
...		ATB/RTB/AVM	FM
Dev N: Dart V.			
SDEs with SW emu (TSIM?)	Mixture of SVFs with LEB and SW simulators (e.g. QERX/SimLeon/...)		
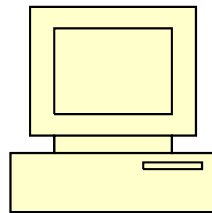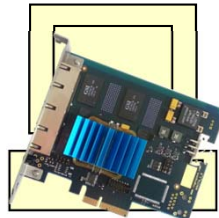
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2. Processor/SoC emulator State of the Art

Facilities based on full Numerical Simulation :

- Instructions Set Simulator (Aeroflex-Gaisler TSIM, Airbus DS Simleon, ...)
- Dynamic Translator/ Just-in-time (SciSys QERx, Airbus DS Simleon, ...)

Hybrid simulation with High emulation accuracy

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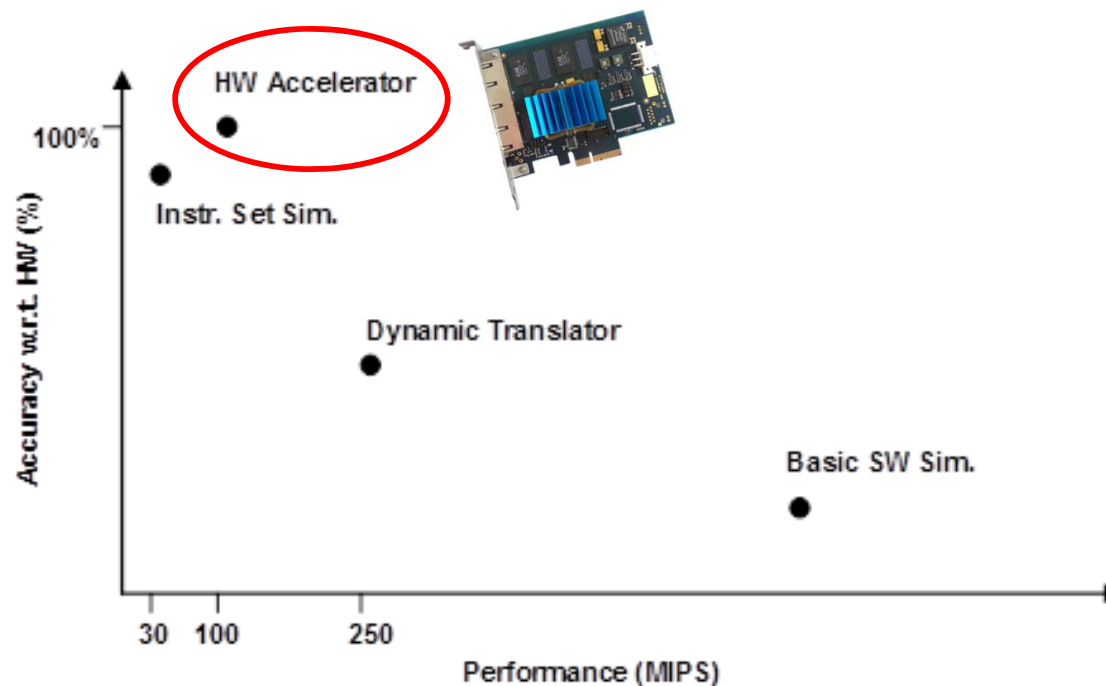
2. Comparison between H/W and S/W emulators

Items	SW	HW	Reason
Representativity	-	+	If HW is dedicated to a target SoC or looks like it -> perfect; otherwise HW deviates from flight OBC or HW needs tailoring. SW Simulation has a limited representativity, for example : FPU, Functional blocks, Cache, Pipelines , …
Memory map	+	-	Overall memory map is frozen in HW versus flexible in SW Simulation. If real IP Core embedded in HW, its HW/SW ICD is fixed. If HW is dedicated to or looks like a target SoC -> perfect; otherwise OBSW & simulations need remapping or HW needs tailoring
Speed of FPU simulation	-	+	SW Sim uses FPU of host (inaccurate) or a SW library (slow). Synch IU <--> FPU fuzzy. HW 100% accurate
Speed of LEON instructions simulation	+	+	HW faster at high CPU loading, SW faster at low CPU loading because SW Sim can skip time (e.g. wait states or power down)
Speed of Functional blocks simulation	+	-	Communication with simulated blocks : LEB : PCIe bus overhead (slow) SW Sim : internal function calls (fast)
Cost	Similar		
Leon CPU speed	+	+	Speed of SW Sim / HW emulators increases with new workstations and new FPGAs

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3. Study History

From the LEB in the "leonSVF" ESA Study in 2005:

- FPGA Board based on Virtex 5 and PCIx
- LEON2 running at 100Mhz
- SRAM only supported at 1 wait state

…to the new LEB in 2014 :

- Support both LEON2 & LEON3 @ 100Mhz
- **SoC oriented**
  - Simulate IP Cores on AMBA bus APB/AHB
  - 2nd Amba bus implementation
  - SpaceWire link embedded in the FPGA
- Based on Ingespace NIKITA Board with
  - Virtex 6 FPGA & PCI Express x4 Gen1
  - 32 Mbytes of SRAM with 0 wait states
  - 64 Mbytes SDRAM

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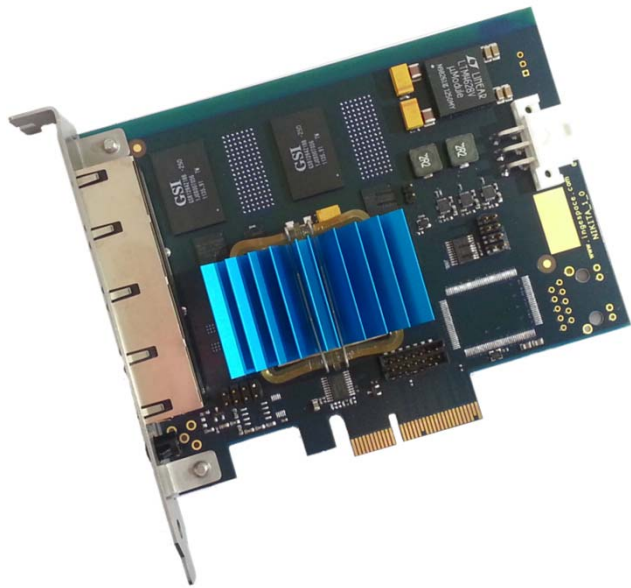
4. Fundamental Principle of Operation

- Simulated Real Time counter (SRT) ←→ Leon clock
- Leon clock & SRT are suspended/frozen when:
    - OBSW accesses I/O
    - OBSW accesses AMBA
    - SoC Tx/Rx a SpW packet / UART character / toggles PIO pin
    - Simulation Time Events expires
- LEB calls back simulation SW via the PCI express bus (comm overhead)
- Simulation SW do their work:
    - provides data to / retrieves data from SoC (I/O, AMBA, RAM...)
    - Raise interrupts…
- Leon clock & SRT are resumed and so on…

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5. Product features (1/4)

- **LEB Configurations :**
  - LEON2 Configuration: ATMEL AT697F + GR FPU
  - LEON3 Configuration similar to Aeroflex UT699
  - LEON3 Configuration inspired from SCOC3

LEON3 memory mapping

Address	Denomination	SW simulations
0x0000 0000	PROM CS0 (4MB)	No
0x1000 0000	PROM CS1 (4MB)	No
0x2000 0000	IO (2*4MB Exclusion Areas)	Yes (Except for exclusion areas)
0x4000 0000	RAM (16MB)	No
0x8000 0000	MCTRL	No
0x8000 0100	APBUART	No
0x8000 0200	IRQMP	No
0x8000 0300	GPTIMER	No
0x8000 0400	**BRIDGES APB SLAVE**	**Yes**
0x8000 0600	GRGPIO	No
0x8000 0700	DSU3 (Debug UART)	No
0x8000 0800	**BRIDGES APB SLAVE**	**Yes**
0x8000 0F00	AHBSTAT	No
0x8000 1000+	Not mapped	No
0x800F F000	**APB PnP AREA**	**Configurable**
0x8010 0000+	Not mapped	No
0x9000 0000	DSU	No
0xA000 0000	**BRIDGE AHB SLAVE**	**Yes**
0xFF00 0000	AHB PnP AREA	No

Embedded IP Core

Connection of Simulated IP Cores

Configurable Plug & Play Areas

Connection of Simulated IP Cores

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5. Product features (2/4)

LEON3 Configuration inspired to the SCOC3 by Airbus DS :
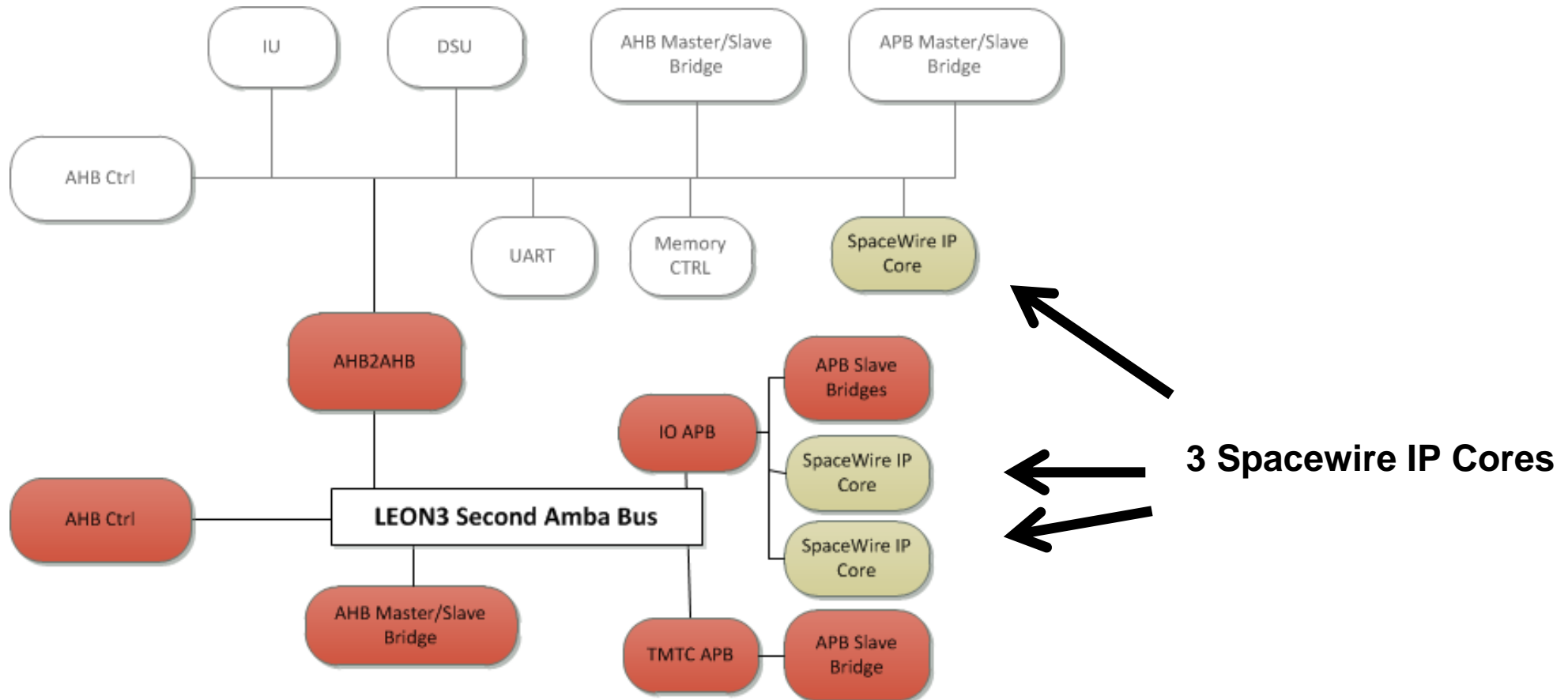
3 Spacewire IP Cores

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5. Product features (3/4)

Building a custom LEB Configuration using reusable building blocks

The LEB design can easily be tailored!
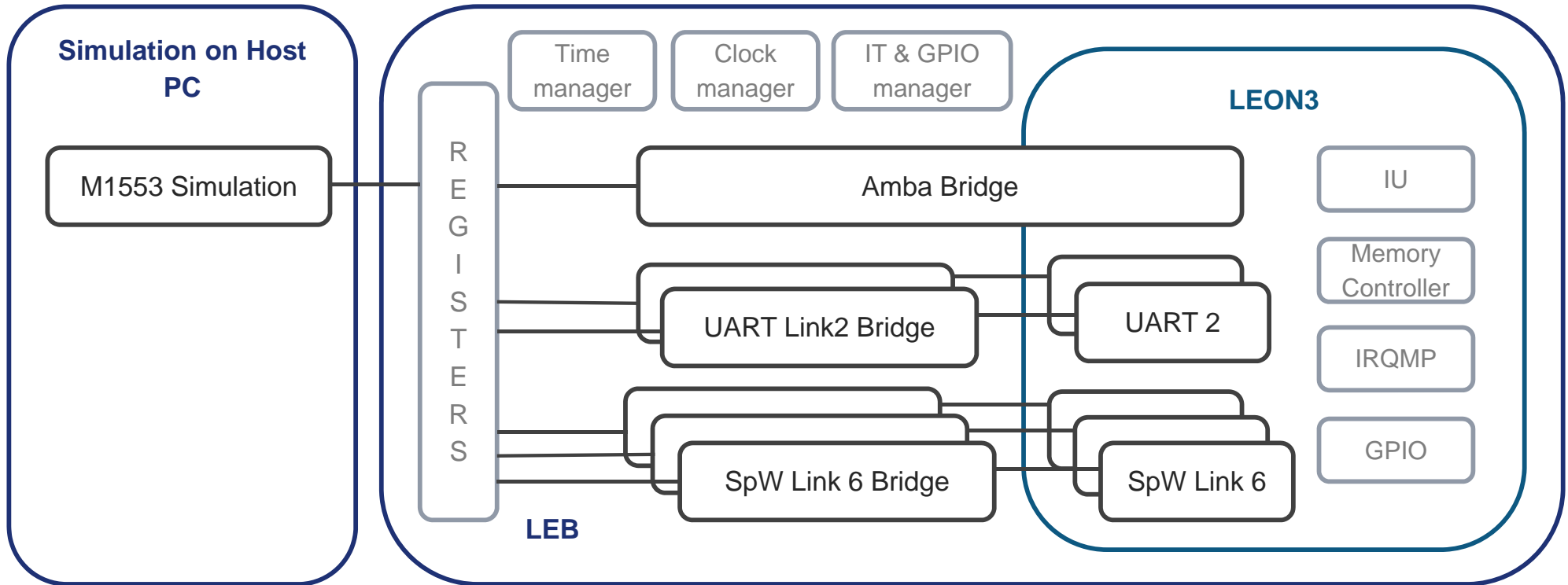
Simulation on Host PC

M1553 Simulation

LEON3

R E G I S T E R S

Time manager

Clock manager

IT & GPIO manager

Amba Bridge

UART Link2 Bridge

UART 2

SpW Link 6 Bridge

SpW Link 6

IU

Memory Controller

IRQMP

GPIO

LEB

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5. Product features (4/4)

The LEB + Control SW is a single Product

CONTROL SOFTWARE

+
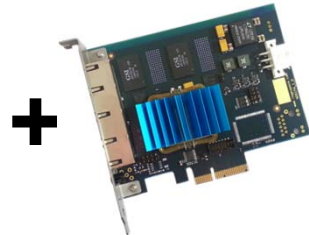
▪ **GDB Server** allows to debug the OBSW
   Breakpoint, patch & dump memory, Ctrl-C
   management …

▪ **Embedded Scheduler**

▪ **Save and Restore** (LEON and Simulation)

▪ **Spacewire** Packet transfers

▪ **I/O & Amba Simulations** interfaces

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6. Product qualification (1/2)

LEB Unit Tests :

- LEON2 & LEON3 IU and FPU tests : Paranoia, Stanford
- All features fully tested and working (Timed Events, S/W Simulation connected to LEON Amba bus using Amba APB/AHB Bridge, GDB Server, Interrupt control, …)

LEB integration into OBC Simulations :

- Integration into the full Airbus DS SCOC3 OBC Simulator
- Integration into ESA EagleEye System running on EuroSim Platform (Airbus DS NL)

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6. Product qualification (2/2)

<u>SpW Stress Test</u> using Airbus DS SCOC3 Simulation running SPOT6 based OBSW

Suspend Cause	Using SPW IP Core Average number of occurrences per second SRT	Using SPW Functional Model Average number of occurrences per second SRT
Read into I/O Suspend Area (8MB/s)	3421	3391
Write into I/O Suspend Area (17MB/s)	860	852
Amba Slave APB read	65	253
Amba Slave APB write	65	144
UART Byte sending	2	2
Timed event trigs	67	7470
SPW packet emission	**7404**	0
Time Windows	128	128

SPW Registers accesses simulation

SPW packets Emission simulation

Simulated OBC Frequency (Mhz)	Real time ratio	Real time ratio
50 Mhz	1,29	**1,02**
60 Mhz	**1,04**	0,89
100 Mhz	0,69	0,53

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7. Performance

Performance scenario based on Airbus DS SCOC3 Simulation running realistic OBSW

Host PC Configuration: Core-i5 3.0 Ghz, 6MB L1Cache, 4GB DDR-SDRAM on RHEL 6 32bits

Simulated OBC Frequency (Mhz)	50			70			100		
Suspend/Freeze Number per Seconds	5 000	10 000	20 000	5 000	10 000	20 000	5 000	10 000	20 000
Real time ratio	1,6	1,4	1,12	1,2	1,07	0,90	0,89	0,83	0,72

Predicted SPOT6 Normal Mode Scenario		
Simulated OBC Frequency (Mhz)	32 Mhz	55Mhz
Suspend/Freeze Number (per Seconds)	20 000	21 000
Real time ratio	1,36	1,0

PCIe + Simulation overhead per suspend : 10-60 us

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8. Product demonstration on EagleEye@EuroSim/SMP2

1. EagleEye demonstrator
   a) static architecture
   b) dynamic architecture / schedule
   c) Performance LEB versus TSIM

2. Spacewire

3. Spacecraft Onboard Interface Services (SOIS)

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8.1 EagleEye demonstrator: overview

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8.1 EagleEye demonstrator: SMP2

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8.1 EagleEye demonstrator: OBC model structure

Separation of concern:

+ **SMP2 Frontend: model interface issues**

+ **Model: functional behaviour**
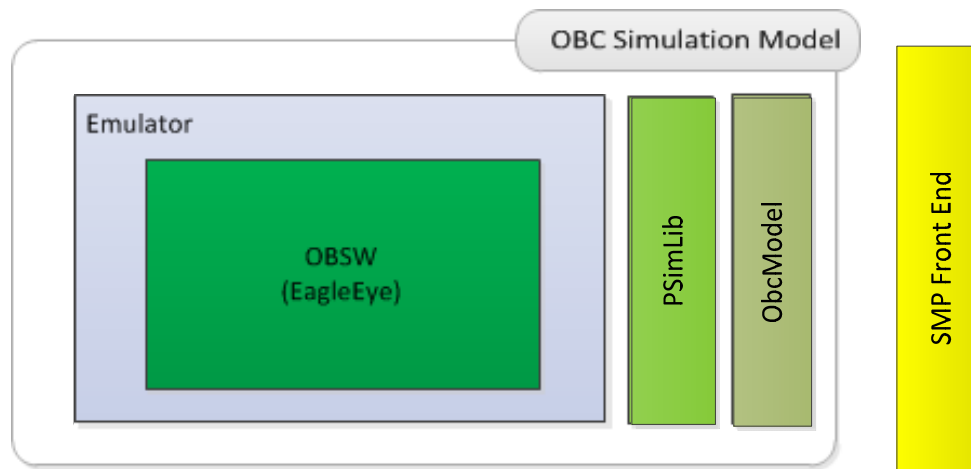
8.1 EagleEye demonstrator: Processor Simulation Library

Emulators:
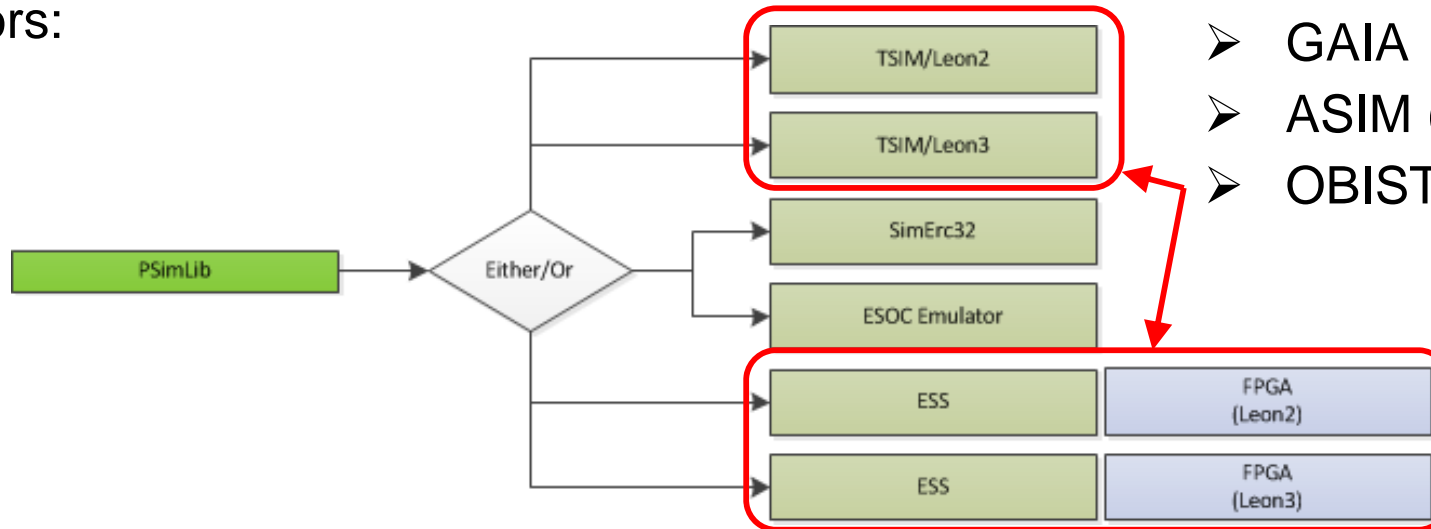
PSimLib deployments:
- ➢ GAIA
- ➢ ASIM (ISS Payload)
- ➢ OBIST/LeonSVF

PSimLib functions:

- ➢ Generic Interface to Processor Emulators/Simulator
- ➢ I/O Events on processor read/write on individual addresses
- ➢ Periodic time events
- ➢ Relative time events
- ➢ Multiple handlers on events
- ➢ Allows for 'plug-n-play' simulation models

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8.1 EagleEye demonstrator: simulation schedule
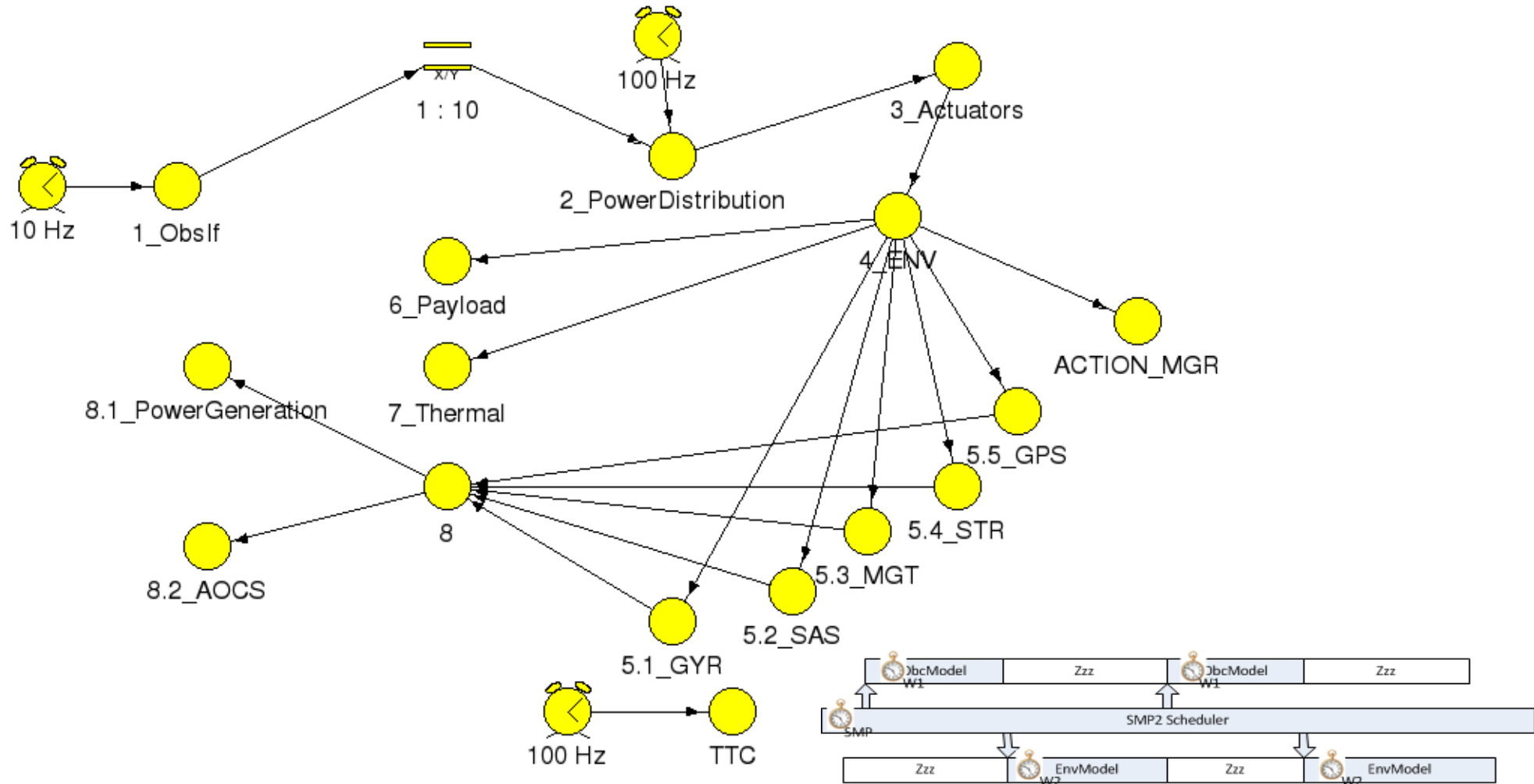
8.1 EagleEye demonstrator: performance LEB vs TSIM

TSIM
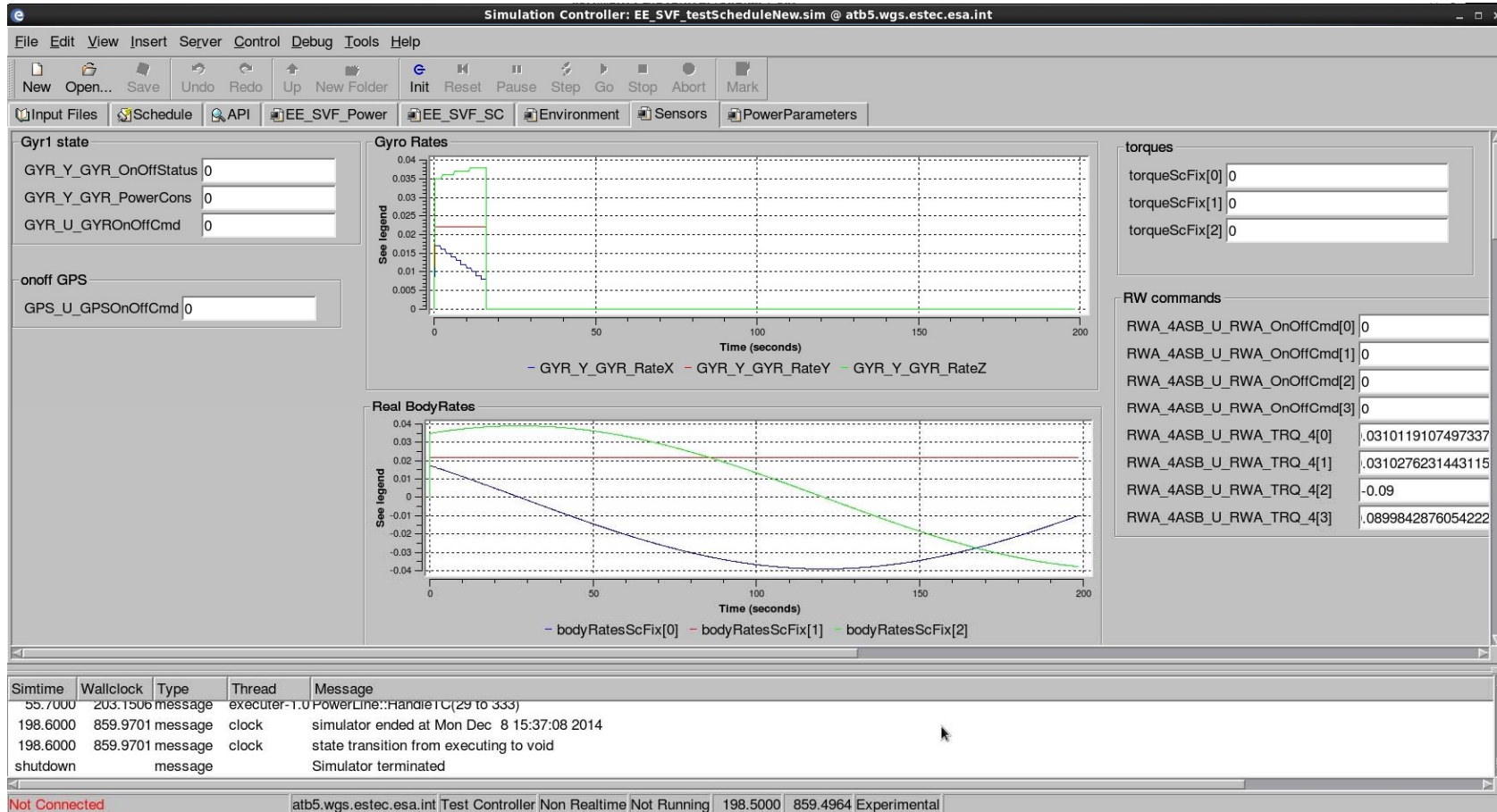
1 : 4.34

DELL, XPS M1710, Intel core, T7200@2.00 GHz (two of those)

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8.1 EagleEye demonstrator: performance LEB vs TSIM

LEB
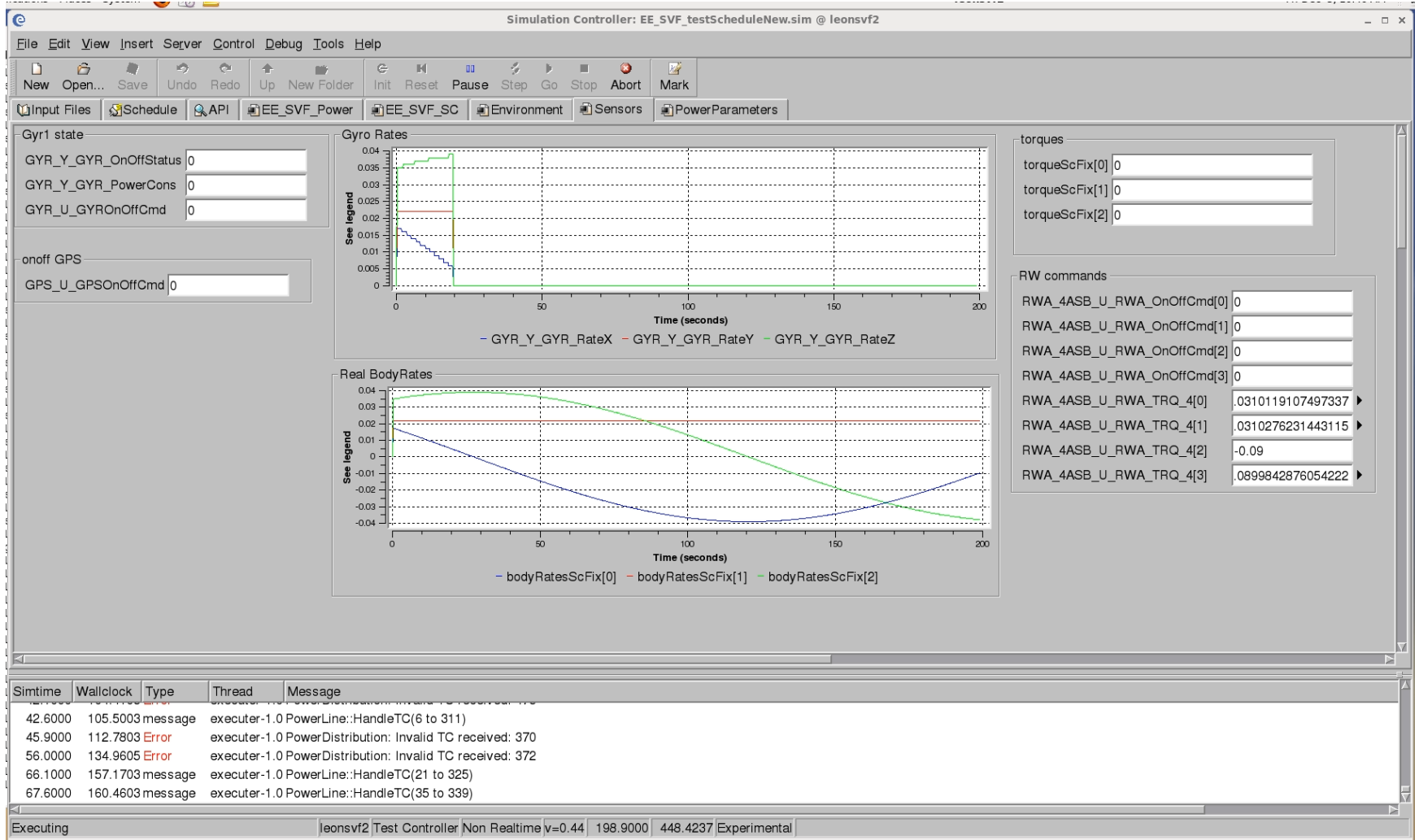
1 : 2.25

Intel i5-3300 @3.00GHz (four of those).

8.2 Spacewire (1/2)

SpW Support added into EagleEye:

➢ **Payload communication:**
Spacewire, SOIS Packet Service, SOIS Device Access Service services

➢ **Platform communication:**
MIL1553, SOIS Memory Access Service
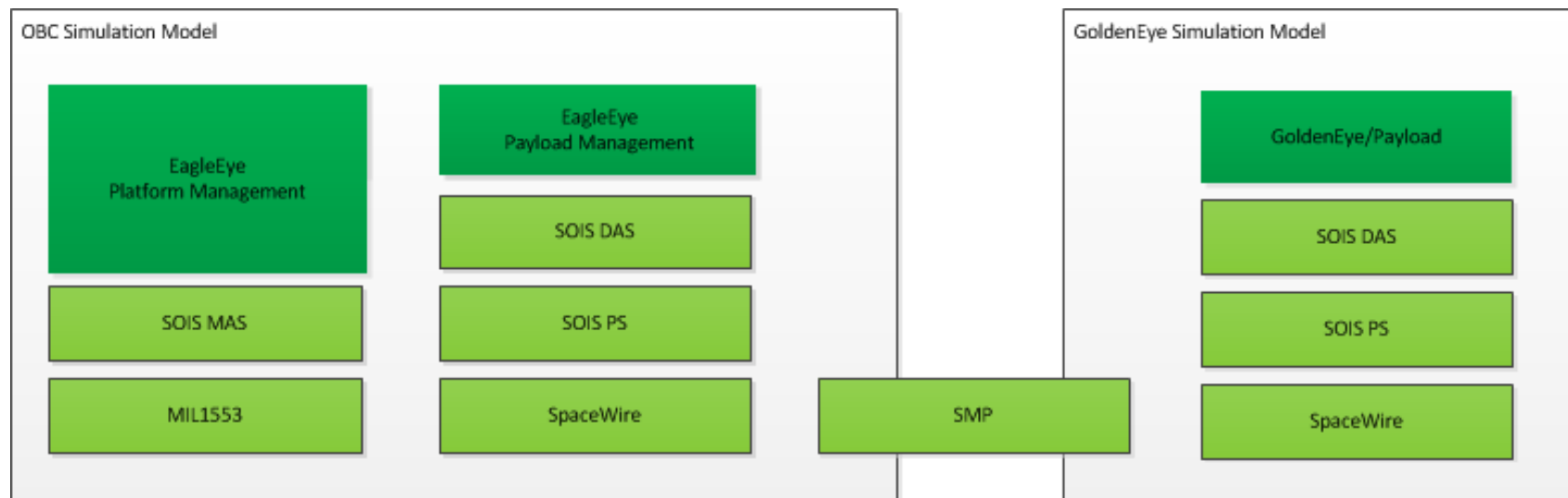
8.2 Spacewire (2/2)

Spacewire – hw/sw co-engineering

Idea:
- SW- and HW-engineers using the same model (System C) in their simulators
- plug-n-play between SystemC spacewire model and FPGA spacewire model

Used pre-existing SpaceWire SystemC/Transaction Level Model, however:
- Generic / not representing the actual SpW IP Core we used
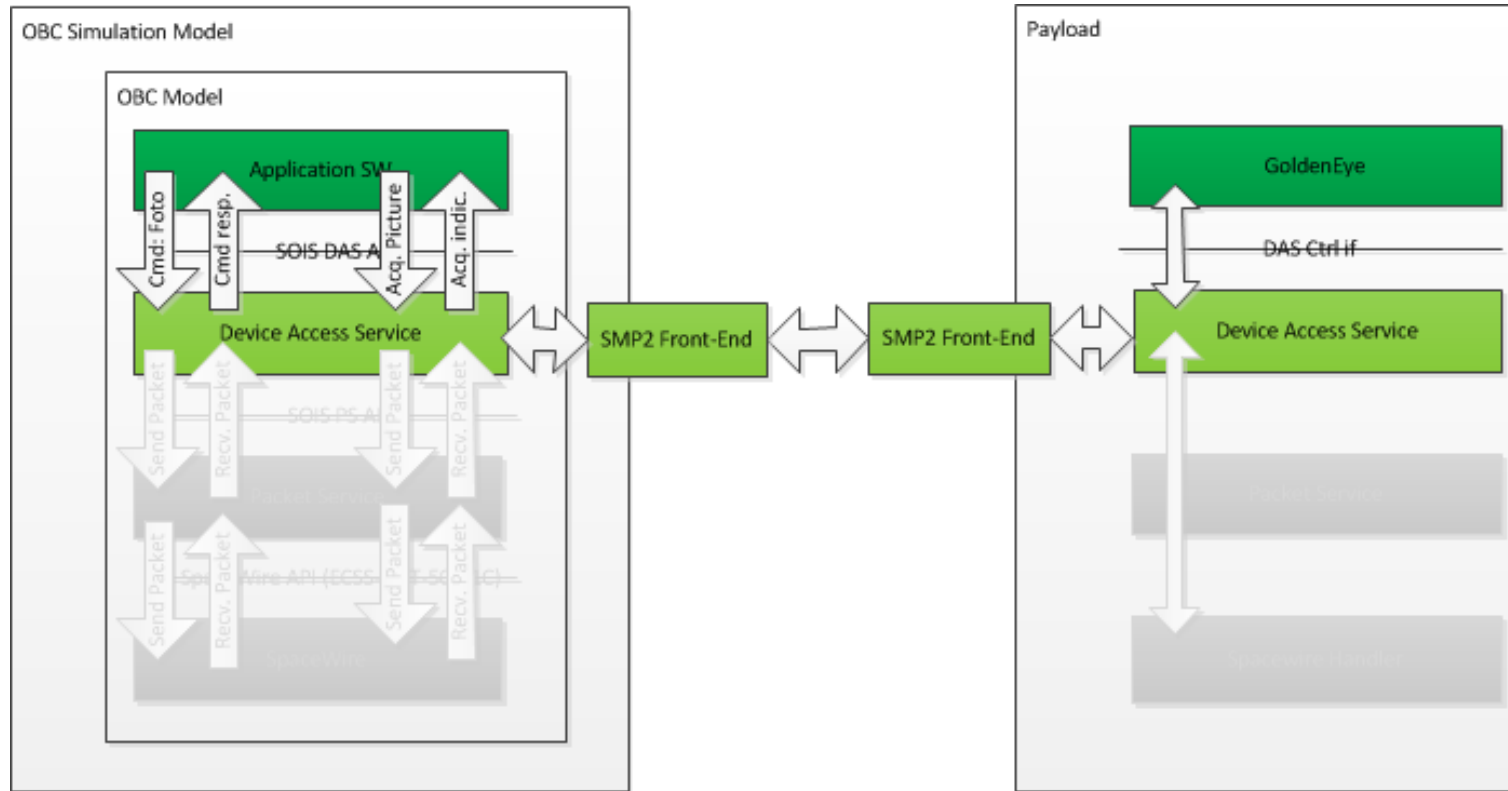- HW/SW interface missing

Conclusion and way-forward:
- For this project:
    - abandon this specific SysC/TLM model in this project
    - keep SpW in FPGA & traditional SpW model
- Ensure consistency between HW/SW interfaces
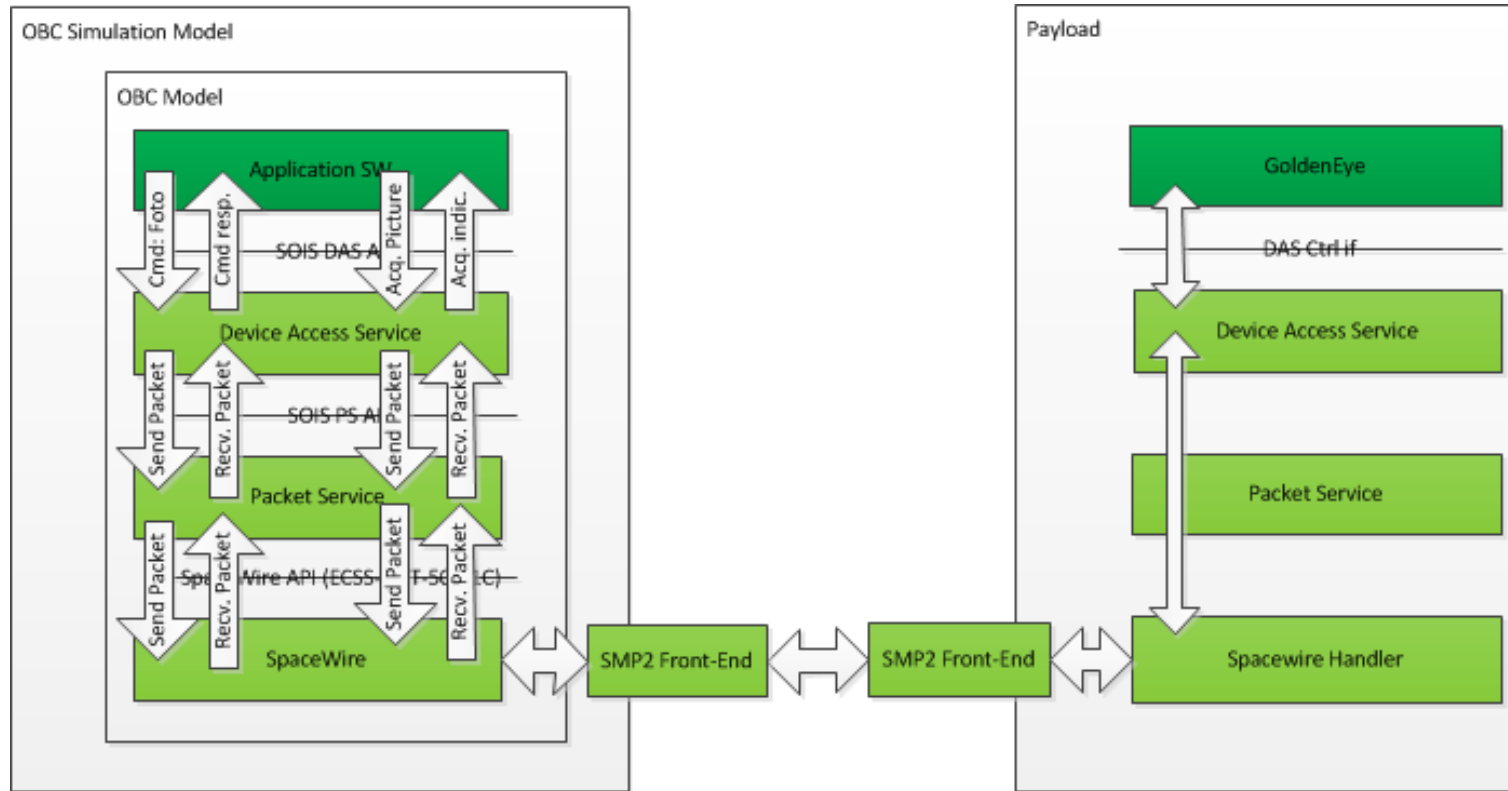- Re-try with both goals in mind, HW-engineering, SW-engineering

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8.3 SOIS: benefit in simulations (1/2)

8.3 SOIS: benefit in simulations (2/2)

9. Conclusion

The LEB is :

1. A mature product using reusable blocks to tailor specific target SoC
2. A Building block for system simulators (SVF, FV and Operational Simulators)
3. Representative (real Leon VHDL)
4. High-performance: 60 MHz in real time in representative load

Outcomes of Integration into EagleEye:

1. Easy 'plug-n-play' exchange of LEB and TSIM
2. LEB performance approximately 2x TSIM
3. FPGA&TSIM demonstrated EagleEye/Eurosim/SMP2 and Airbus DS SimTG
4. Spacewire integration in progress - tested and stressed on LEB level
5. SOIS replacement demonstration on going

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10. How to get an LEB

LEB FPGA[1] and support
(Ingespace and/or Airbus DS)

LEB
license
(ESA)
(admin costs)

license
Leon2FT
(ESA)
(admin costs)

license
Leon3
& FPU
(Aeroflex)

purchase

request

use or
modify SW

request

purchase

you tailor VHDL
of LEB or Leon
for your SoC
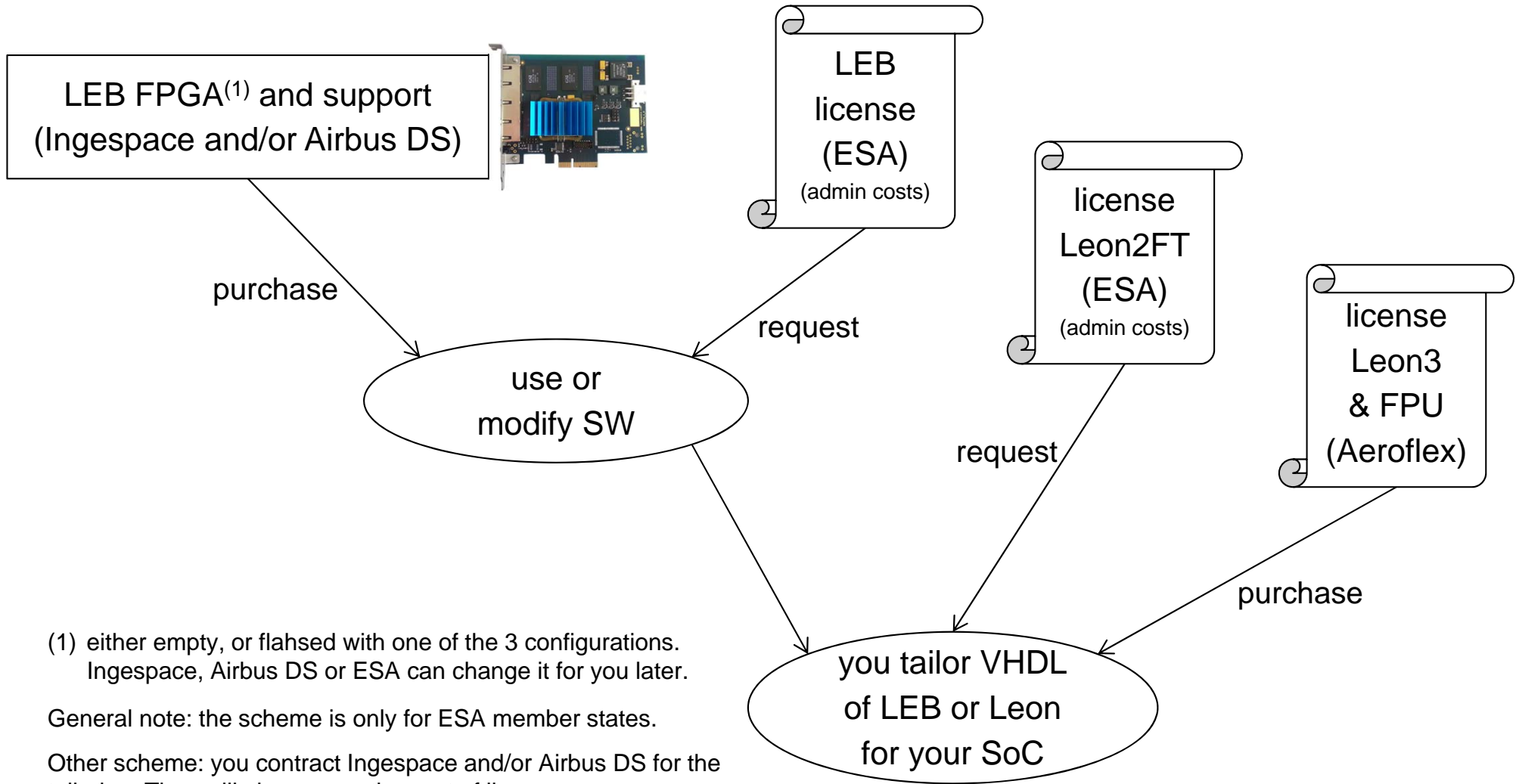
(1) either empty, or flahsed with one of the 3 configurations.
     Ingespace, Airbus DS or ESA can change it for you later.

General note: the scheme is only for ESA member states.
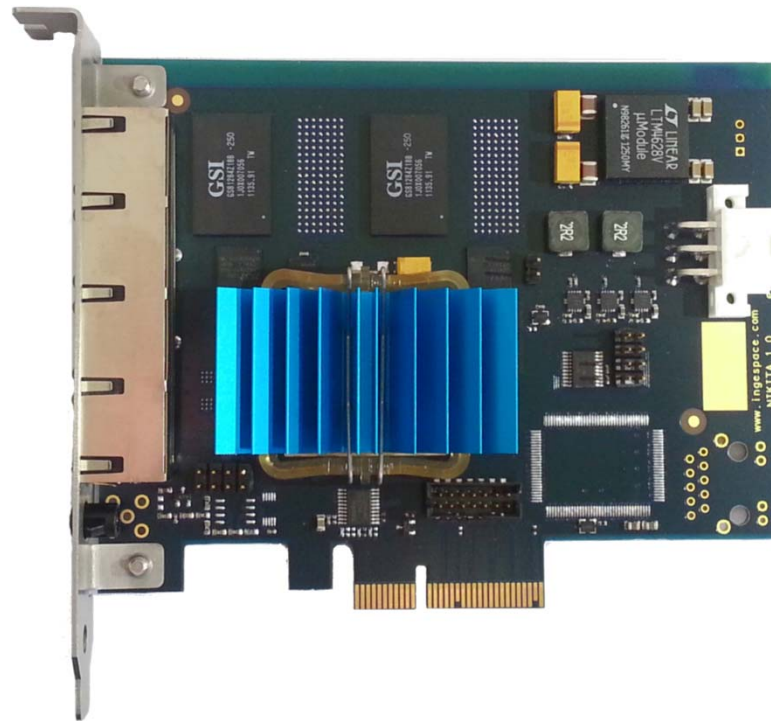
Other scheme: you contract Ingespace and/or Airbus DS for the
tailoring. They will charge you the cost of licenses.

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Any questions?

Please contact us if you want to test it in your project

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Extra slides

Focus on the LEON Memory Mapping

Address	Denomination	SW simulations
0x0000 0000	PROM CS0 (4MB)	No
0x1000 0000	PROM CS1 (4MB)	No
0x2000 0000	IO (2*4MB Exclusion Areas for fast emulation of I/O mapped memory)	Yes (Except for exclusion areas)
0x4000 0000	RAM* (16MB)	No
0x8000 0000	MEM CTRL	No
0x8000 000C	FALAR/FALSR	No
0x8000 0014	CACHE CTRL REG	No
0x8000 0018	IDLE REG	No
0x8000 001C	WRITE PROTECT	No
0x8000 0024	PRODUCT CONFIG REG	No
0x8000 0028	**BRIDGE APB SLAVE**	**Yes**
0x8000 0040	TIMERS	No
0x8000 0070	APB UART 1	No
0x8000 0080	APB UART 2	No
0x8000 0090	INTERRUPT CTRL	No
0x8000 00A0	I/O PORT	No
0x8000 00B0	**BRIDGE APB SLAVE**	**Yes**
0x8000 00C0	DSU UART	No
0x8000 00D0	WRITE PROTECT	No
0x8000 00E0	**BRIDGE APB SLAVE**	**Yes**
0x8000 0400 +	Not mapped	No
0x9000 0000	DSU	No
0xA000 0000	**BRIDGE AHB SLAVE**	**Yes**

LEON2 memory mapping

Address	Denomination	SW simulations
0x0000 0000	PROM CS0 (4MB)	No
0x1000 0000	PROM CS1 (4MB)	No
0x2000 0000	IO (2*4MB Exclusion Areas)	Yes (Except for exclusion areas)
0x4000 0000	RAM (16MB)	No
0x8000 0000	MCTRL	No
0x8000 0100	APBUART	No
0x8000 0200	IRQMP	No
0x8000 0300	GPTIMER	No
0x8000 0400	**BRIDGES APB SLAVE**	**Yes**
0x8000 0600	GRGPIO	No
0x8000 0700	DSU3 (Debug UART)	No
0x8000 0800	**BRIDGES APB SLAVE**	**Yes**
0x8000 0F00	AHBSTAT	No
0x8000 1000+	Not mapped	No
0x800F F000	APB PnP AREA	Configurable
0x8010 0000+	Not mapped	No
0x9000 0000	DSU	No
0xA000 0000	**BRIDGE AHB SLAVE**	**Yes**
0xFF00 0000	AHB PnP AREA	No

LEON3 memory mapping

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Focus on the UART and SpW Links Implementations

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