OBC Simulator Architectures and Interfaces to System Test Benches / LeonSVF

Activity: GSTP (FR + DK) + StrIn (DK) + Lab investment

Prime contractor: Airbus DS Toulouse ~ Presenter: Gregory Queré (Airbus DS), Poul Hougaard (Terma)

ESA TO: Mauro Caleno

Abstract:

The goal of the project “OBC Simulator Architectures and Interfaces to System Test Benches” is to define architectures and interfaces for simulators of on-board computers based on Leon 2 and Leon 3 System on Chips (SoC). The primary output of the activity is a PCIe FPGA Leon Emulation Board (LEB) together with a number of reusable VHDL and software simulation components to tailor the FPGA to a specific target SoC. The LEB executes the actual Leon VHDL code thus enabling hardware-in-the-loop (HIL) emulation of Leon SoC’s. The LEB designed for Linux workstations and is controlled via an API compatible with TSIM by Aeroflex-Gaisler. The LEB was integrated in the EagleEye of the Avionics Test Bench on Eurosim with SMP2 and demonstrated in there. The activity also has two secondary goals: exploring whether a model of a spacewire IP Core written by hardware engineers in SystemC/TLM could be reused in an OBC simulator (HW/SW engineering); and exploiting the SOIS layered architecture to skip simulation of and abstract from the OBC HW/SW ICD in an OBC simulator.

This GSTP project started in March 2013 with Airbus DS (France) and Terma (Denmark) and is currently under extension by CCN and concludes with the Acceptance Review in December 2014. However the project already achieved large part of its baseline goals earlier this year and so its status was presented at the FPD in May 2014 and at the DASIA 2014.

The LEB is an evolution of the earlier project “Leon Software Validation Facility” presented at DASIA 2008. The LEB enables connecting software simulations to addresses in the I/O space, internal APB and AHB AMBA spaces, managing simulation time events as well as transmitting and receiving entire spacewire packets when a SpW IP Core is embedded in the FPGA. The transfer of entire spacewire packets and connecting simulations to the internal APB and AHB AMBA busses are new functions that enable HIL simulation of SoCs. The key mechanism of the LEB, is that whenever simulation events trigger (I/O, AMBA, time or packet), the clock signal to the Leon IP Core is suspended to keep time representativity for the on-board software (OBSW) while the simulations execute.

The project produced 3 configurations of the LEB: for the Atmel AT697, for a generic Leon3 configuration and for a Leon3 configuration inspired from the SCOC3 SoC by Airbus DS and which embeds the Spacewire IP Cores.

The LEB is the core of the OBC simulator integrated in the EagleEye ATB in the ESTEC avionics Lab via SMP2 interfaces.