Advanced Memory Controller and Embedded File System Manager IP Cores

Activity: TRP

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Abstract:

The objective of the project was the development and validation of 2 IP cores:
1.) Advanced Memory Controller IP Core (AMEMCTL IP Core)
2.) Embedded File System Manager (EFSM IP Core)

1.) The AMEMCTL IP Core supports NAND-Flash and DDR2 SDRAM memories, it executes the following memory management functions

• Mode management of the memory devices
• Initialization sequence at power-up according to the memories used
• Auto-refresh management (DDR2 only)
• Self-refresh management (retention mode, DDR2 only)
• Operational read/write mode according to the memories used
• Low-level interface with the memory devices
• Individual management of addresses according to read and write process
• Full or reduced memory test
• Scrubbing (with higher-level assistance for Flash)
• Local status management and switch-off control
• Data protection EDAC (Reed Solomon)

It interfaces two memory types:
• non–volatile NAND Flash memory
• volatile DDR2 SDRAM memory

2. The EFSM IP Core is a mass memory file system manager using a file allocation table principle. It main functions are to

• provide sector address for data storage in a mass memory (write command)
• provide sector address for read data from the mass memory (read command)
• provide sector address in function of time (seek command)
• remove sector from files (delete command)

The project was divided into 3 phases:

a) IP Definition Phase
This phase was dedicated to the top-level functionality understanding and to the system requirements definition. This requirements definition phase was based on the preliminary IP Specification issued in the frame of the proposal and on the ESA comments and advices. The steps of the system development and the description of the test and validation execution were defined and described in the IP Verification Documents. Preliminary IP Datasheets were generated. The Specifications Review (SR) concluded this first phase.

b) IP Architectural Design Phase
Based on the documents issued during the definition phase, the IP architectural design was started. The design was broken down into modules and functions which were defined and described in the

Architectural Design Documents. The functional description of the IP was then developed in VHDL code including test benches dedicated to the test and verification of the implemented functionalities. A preliminary IP database was issued. The IP Datasheet was updated to reflect the IP evolutions. The validation strategy of the IP was described in the Verification Plan document. This phase was concluded by the Architectural Design Review (ADR). On ESA request, the Datasheet, the Architectural Design Description and the Verification Plan (test case as well as database description) were compiled into one document, the IP User Manual.

c) IP Detailed Design Phase

During this project phase the IP was synthesized in the selected technologies and placed and routed in FPGA technologies. The IP Datasheets and Verification documents were updated with the performance and place and route results. The User Manuals were updated. The IP databases were updated. This task was concluded by the Final Review (FR).