SYDERAL

VHDL IP Cores

Contract No. 4200022043 - R. Weigand

TEC-ED & TEC-SW Final Presentation Days

ESA / ESTEC 9-10 Dec 2014

SYDERAL SA - S. Humbert

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Project Overview

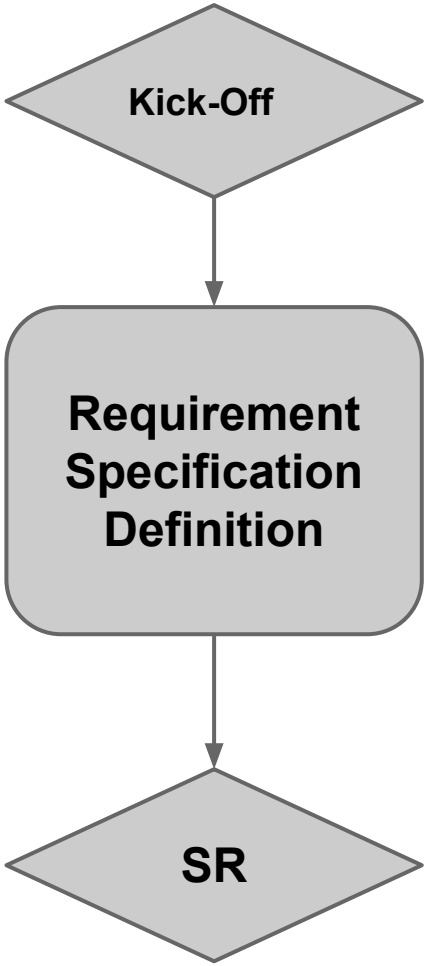
- **Advanced Memory Controller IP Core**

  ⇒ AMEMCTL IP Core

- **Embedded File System Manager IP Core**

  ⇒ EFSM IP Core

Project Phases



IP Definition Phase

Top-level function understanding

Establish the IPs requirement specification based on the preliminary IP Specifications provided in the proposal

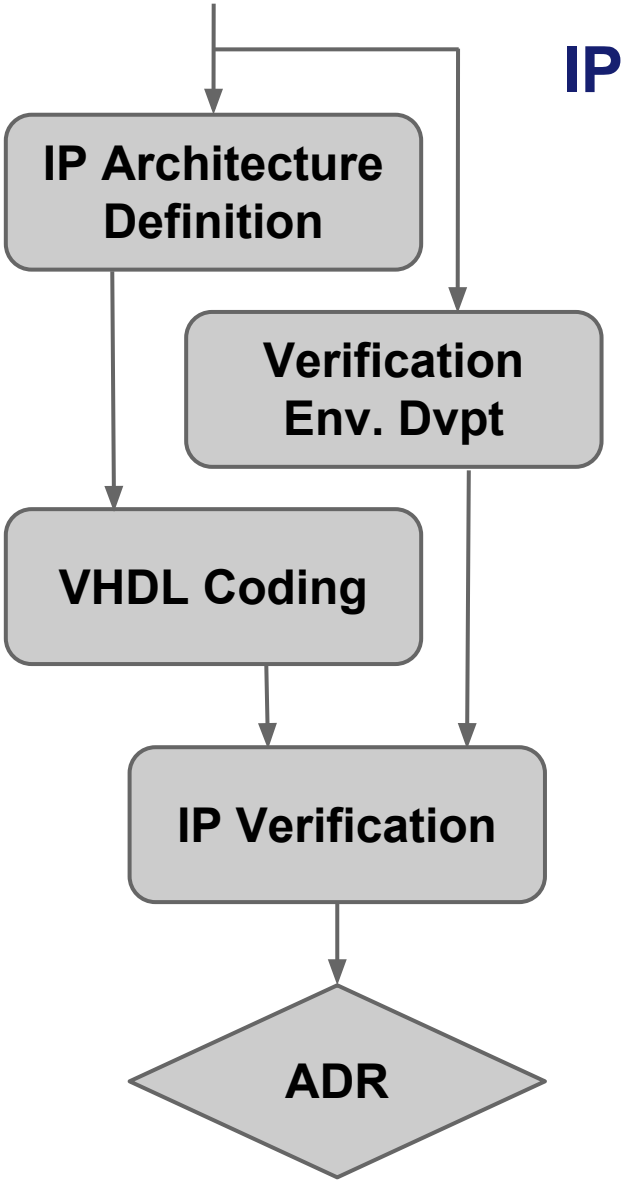
⇒ IP Requirement Specification

⇒ Preliminary IP Datasheet

⇒ Preliminary IP Verification Plan

Concluded by Specification Review

Project Phases



IP Architectural Design Phase

Design broken down into modules

IP development (VHDL)

Verification environment coding (SV)

IP Verification task

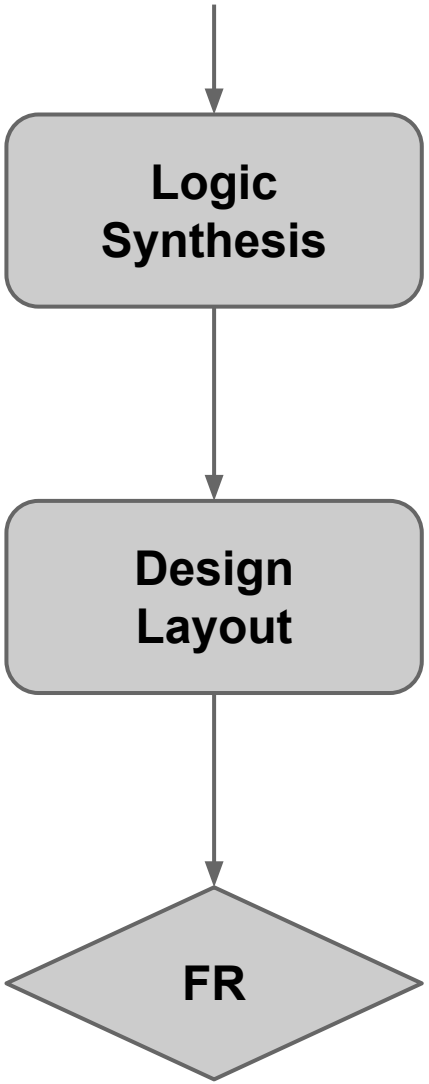
⇒ IP Datasheet (updated)

⇒ IP Verification Plan & Report

⇒ IP Database

Concluded by Architectural Design Review

Project Phases



IP Detailed Design Phase

IP logic synthesis and place & route (layout) in FPGA technologies:

- Microsemi RTAX-S
- XILINX Virtex4 / Virtex5

Resources, Timing & performance report

IP Datasheet, Architecture and Verification merged in :

⇒ IP User Manual

Concluded by Final Review

Project Contributors

Phases	Advanced Memory Controller IP	Embedded File System Manager IP
IP Definition	Syderal / ESTEC	Syderal / ESTEC
IP Architectural Design	HES-SO Valais	Syderal
IP Detailed Design	HES-SO Valais	Syderal

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Advanced Memory Controller IP Core (AMEMCTL)

Main IP Features

- Memory Controller IP For Solid State Mass Memories
- Block Based Access to Memory Banks
- Generic AMBA Interface
- Interface either Nand Flash or DDR2 SDRAM Devices or both
- Configurable IP
- Protected Storage

Memory Management

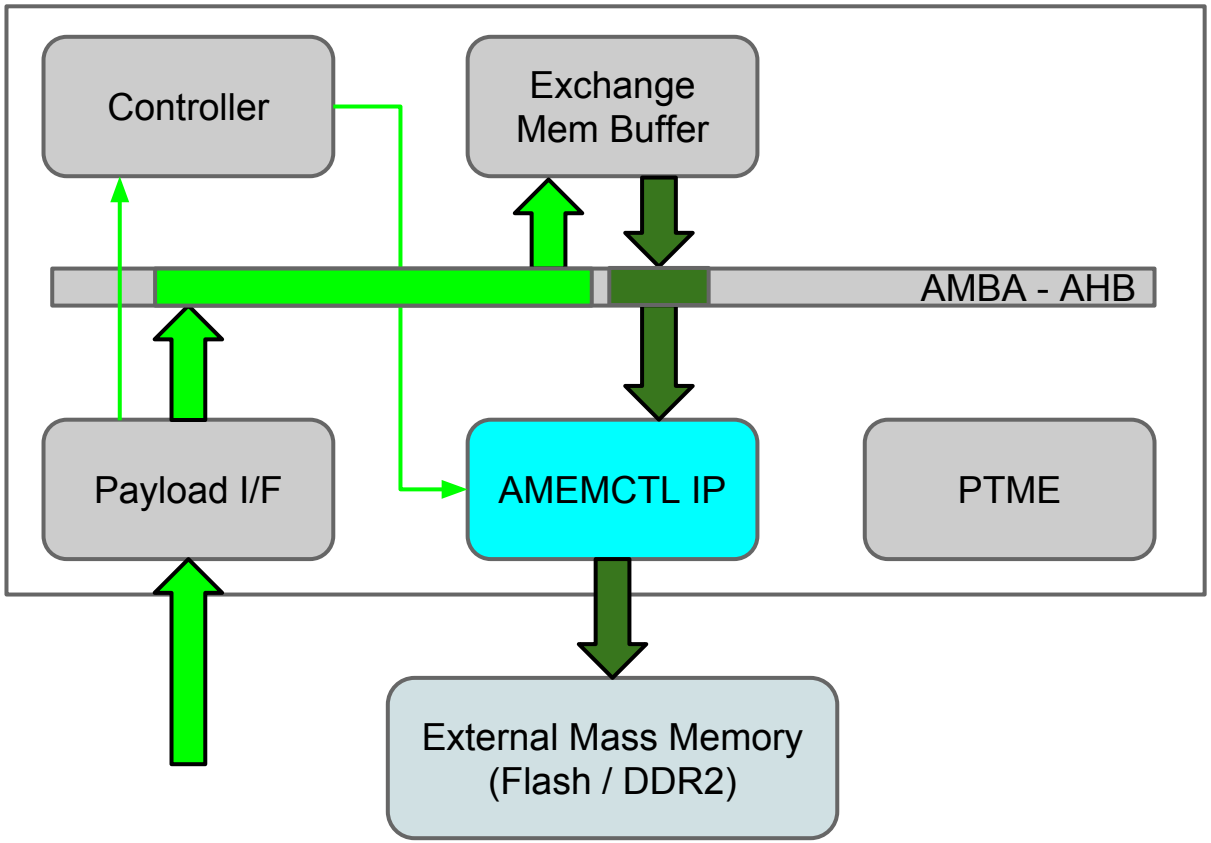
- Memory Devices Mode Management
  - Initialization
  - Auto-refresh/Self-refresh
  - Read/write(/erase) sequences
- Memory Testing (Blocks, Devices, Banks)
- Memory Scrubbing
- Event/status Reporting

Main Interfaces

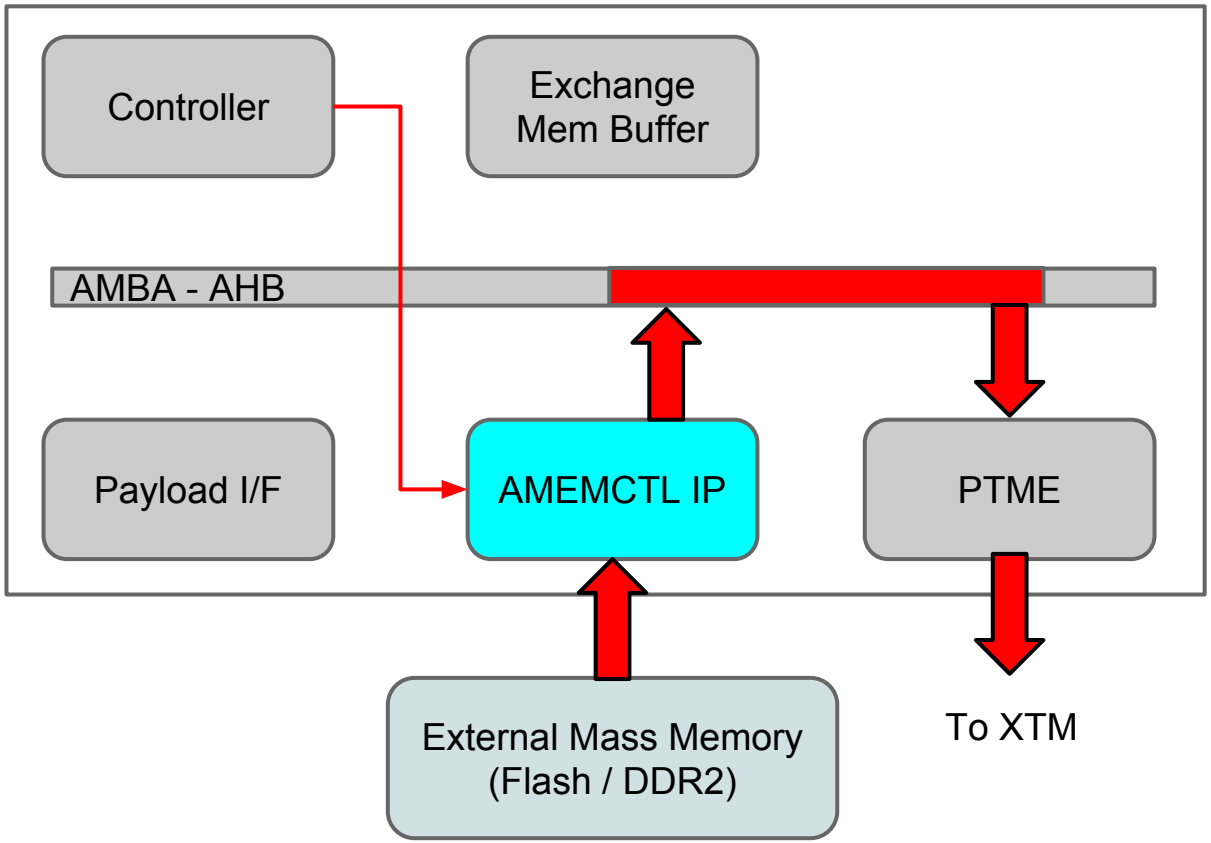
- **AMBA – AHB Master**
  Used for Data transfer to/from Memory
- **AMBA – APB**
  Commands / Configuration registers access
- **DDR2 and / or Flash Memory Interface**
  DDR2: EDE5108 64M words x 8 bits

  Flash: K9F8G08 1G x 8 bits 4096 Blocks of 64 Pages

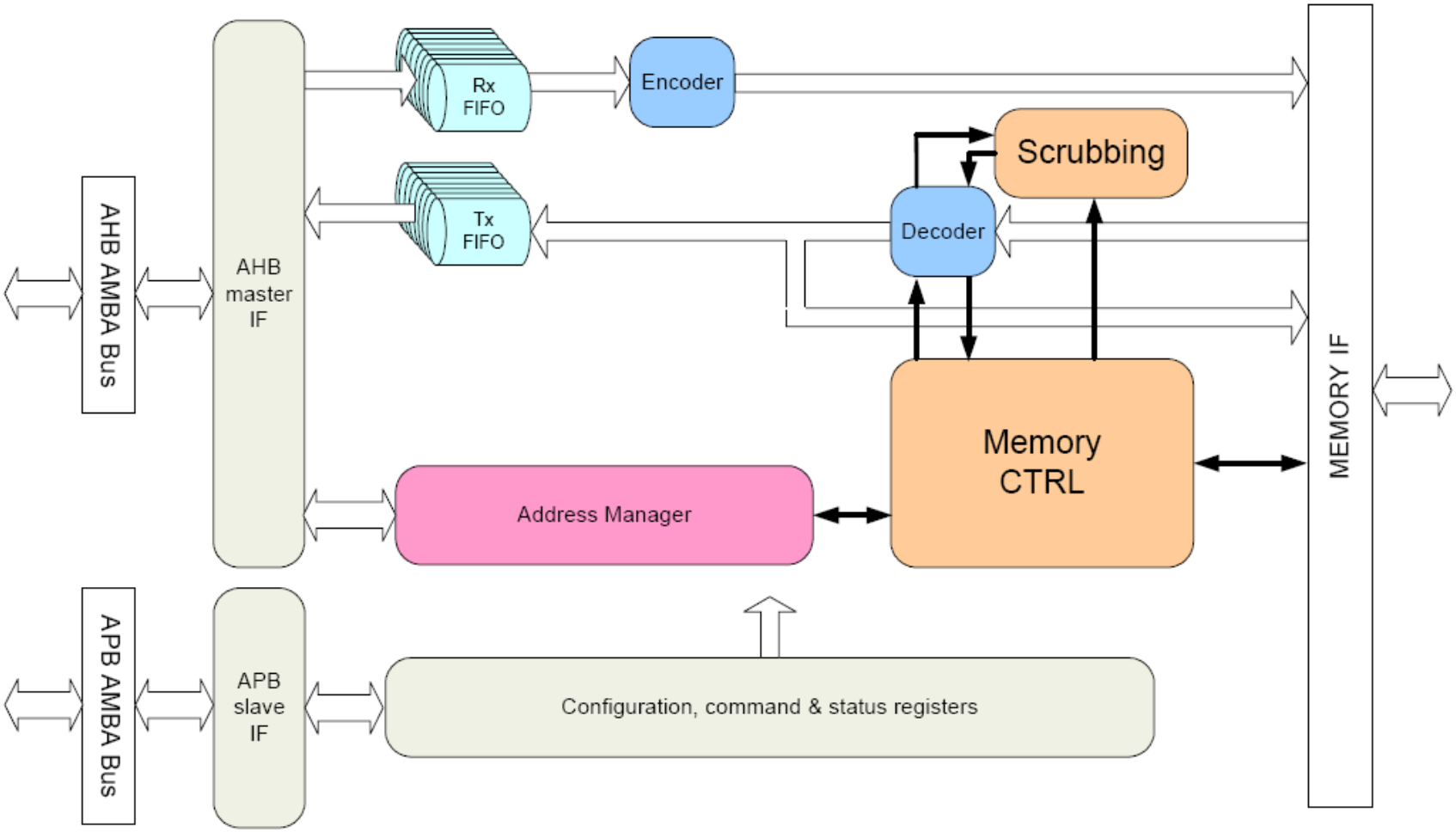
Application Example - Write Operation



Application Example - Read Operation



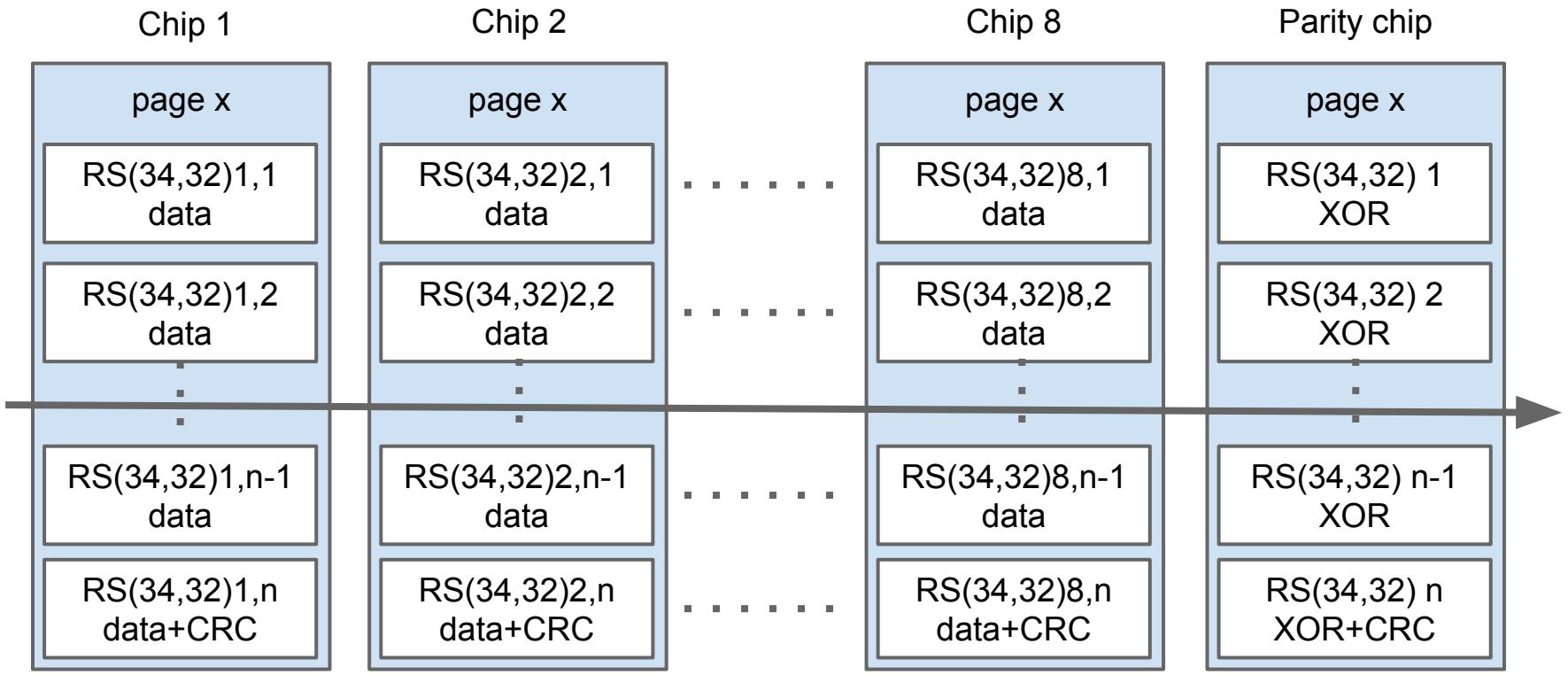
IP High-level architecture



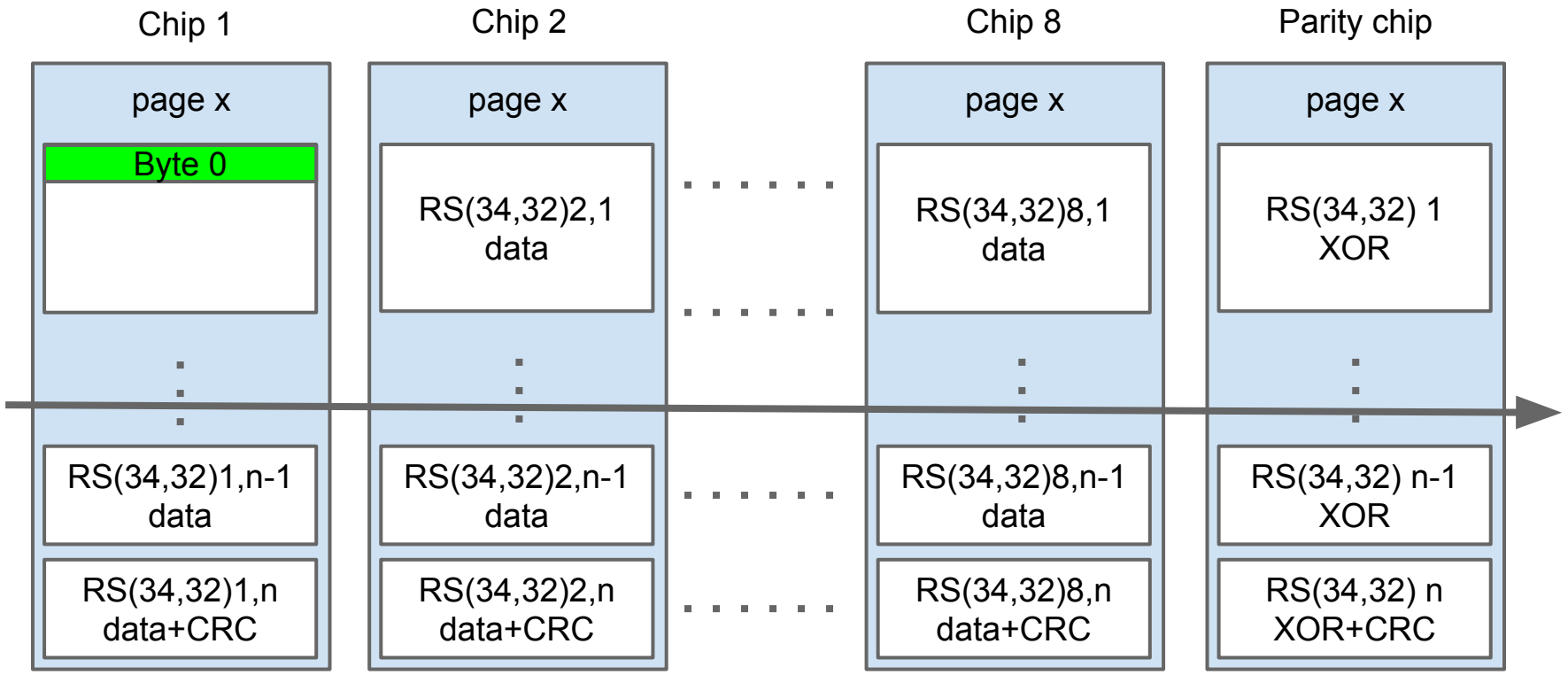
Error protection mechanisms

- A Reed Solomon (34,32) code able to detect and correct a single symbol error
- A 64-bit Cyclic Redundancy Check (CRC) able to detect multiple errors
- A XOR parity chip computed through the chips (row by row) able to correct multiple errors due to a page, block or chip failure

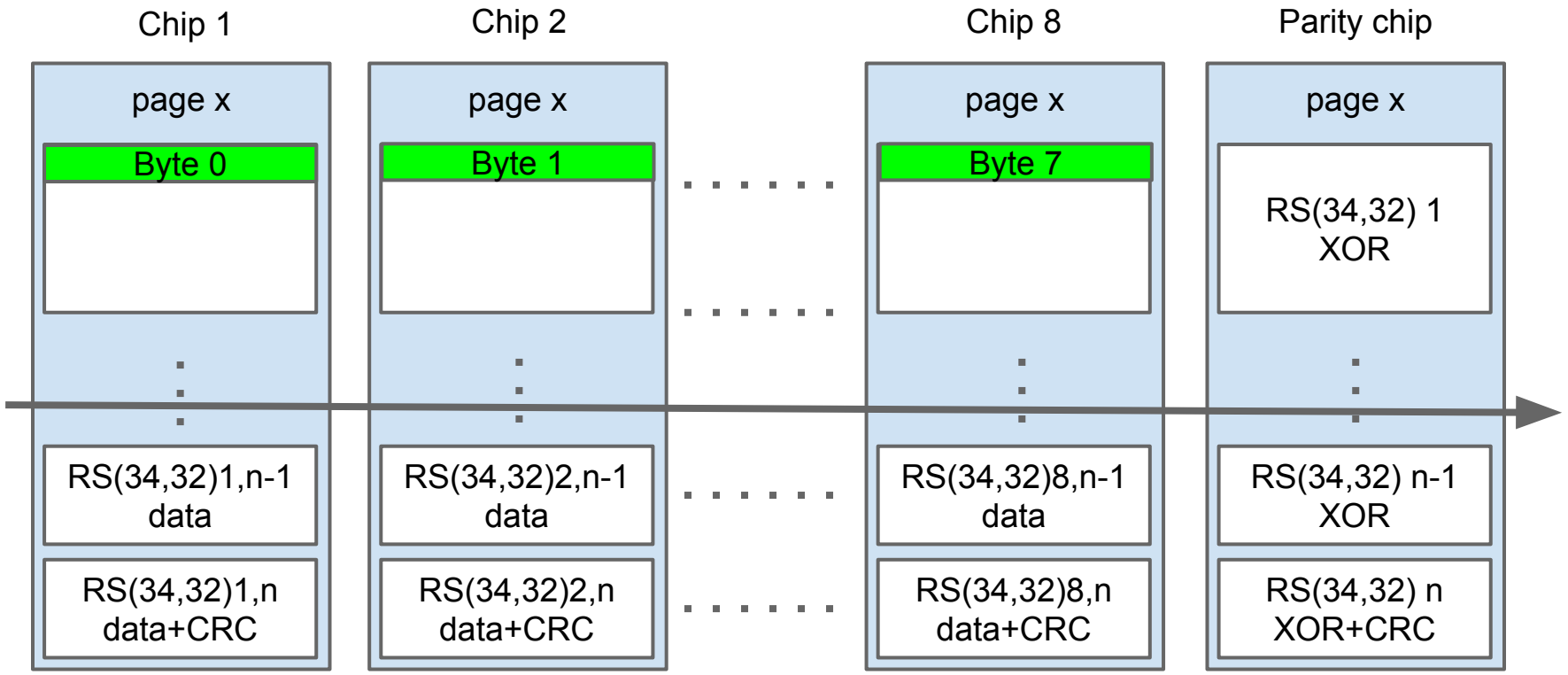
Error protection mechanism



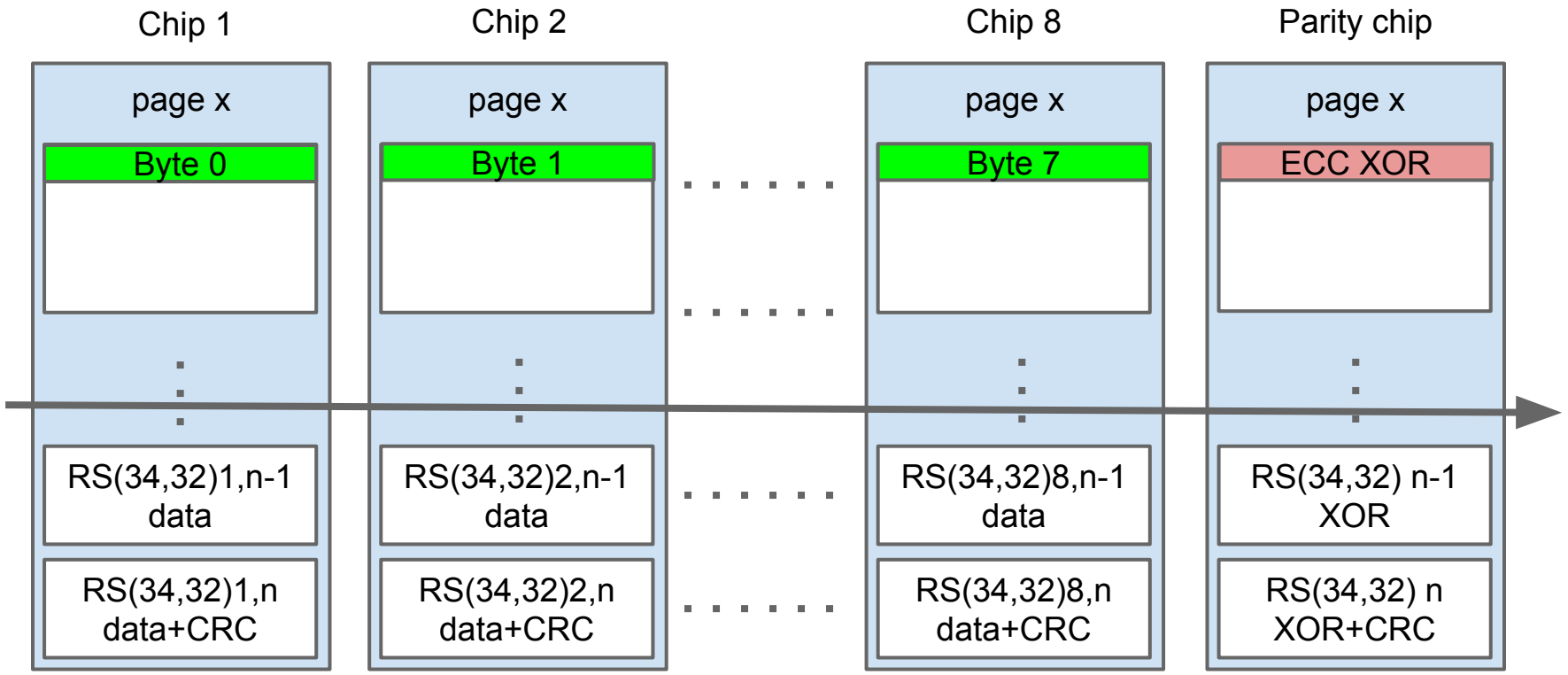
Error protection mechanism



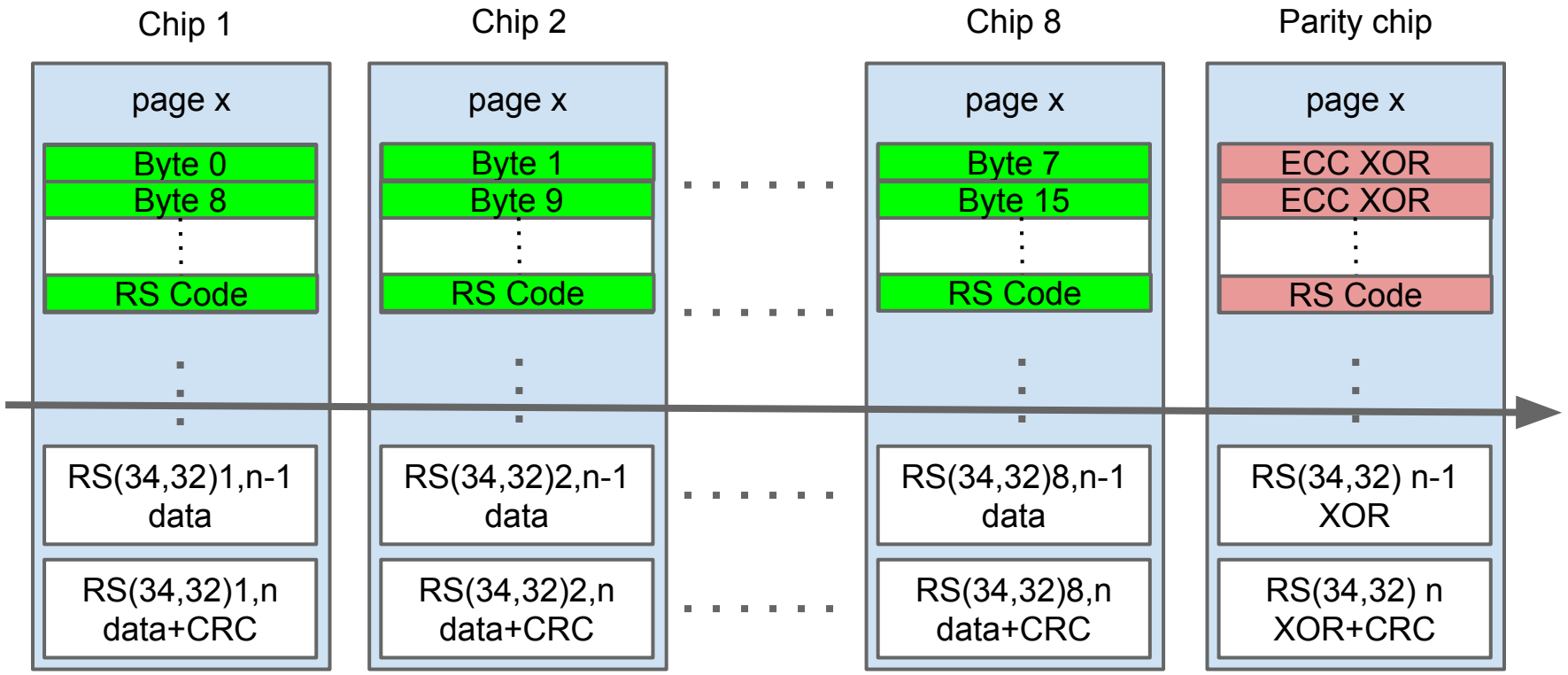
Error protection mechanism



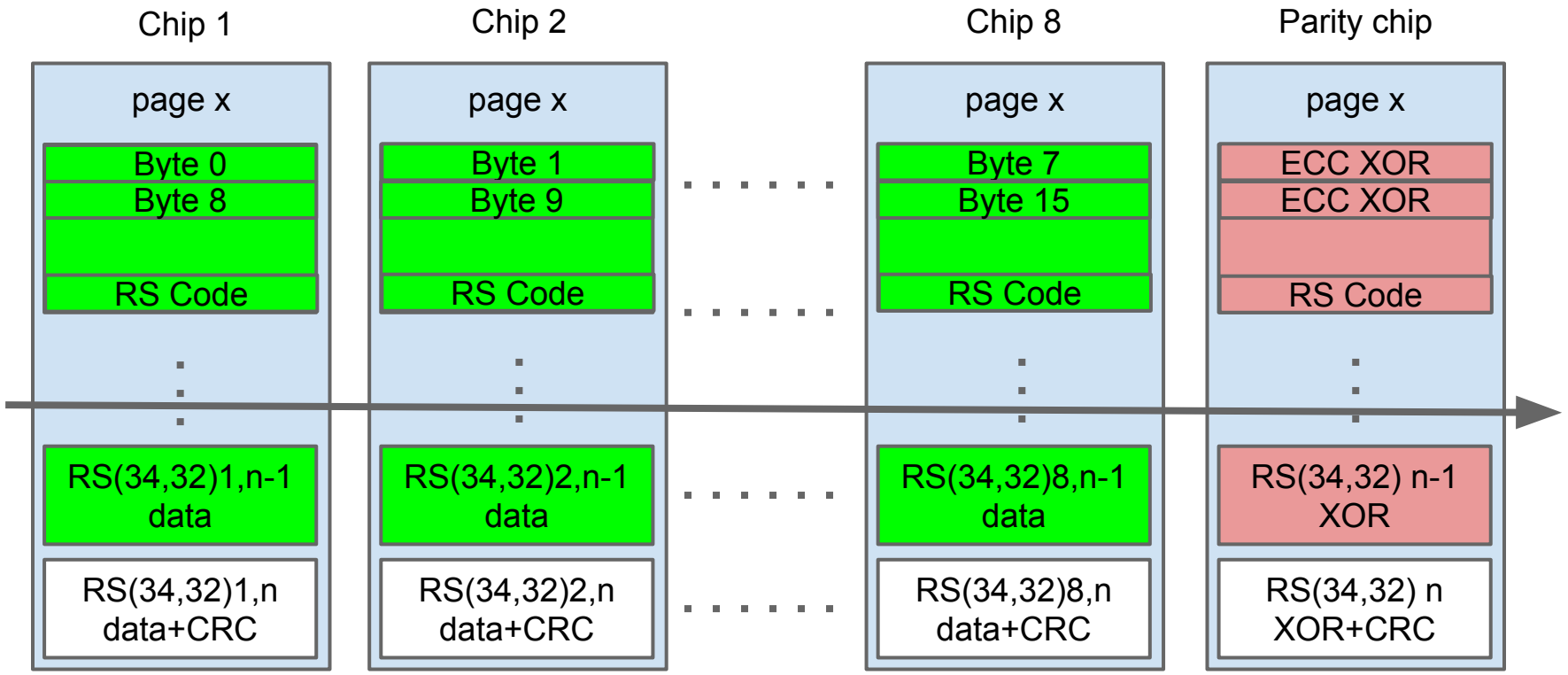
Error protection mechanism



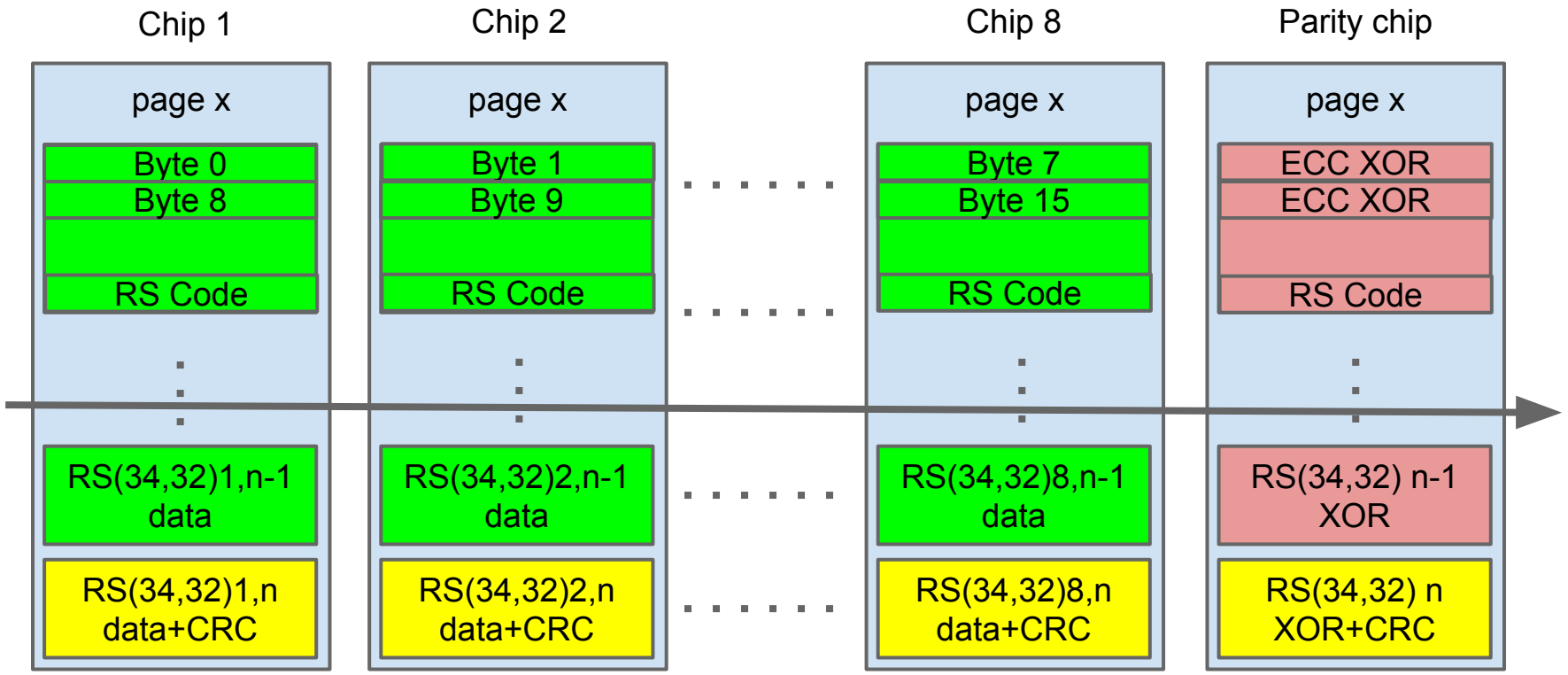
Error protection mechanism



Error protection mechanism



Error protection mechanism



Implementation Results

IP Configuration 1 (small & simple)

Flash memory only, 4 chips without redundancy (XOR)

No embedded EDAC (data already protected at source level)

Technology : Microsemi RTAX4000S

⇒ Resources Usage:

Core cells: 16% (9'444 of 60'480 cells)

Internal Ram blocks: 60% (72 of 120)

⇒ Performances : 50MHz

Implementation Results

IP Configuration 2 (all inclusive)

Flash & DDR2 control, 8 chips with redundancy (XOR)

Embedded EDAC (Reed-Solomon & CRC)

Internal buffers protected with EDAC

Technology : Xilinx Virtex5

⇒ Ressources Usage:

LUT : 15% (21'055 LUT)

Internal Ram blocks: 85% (164 of 192)

⇒ Performances : >70MHz (System clock)

: >200MHz (DDR2 input clock)

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Embedded File System Manager IP Core

(EFSM IP)

Main IP Features

- Manage the File System used for packet data storage in Mass Memory
- Generic AMBA Interface
- Several file types supported
- Configurable IP
- Read / Write / Delete / Search operations

Main Interfaces

- **AMBA – AHB Slave**
  Used to access FSM & File Tables by user
- **AMBA – APB**
  Configuration registers access
- **RAM IF (optional)**
  Internal/external dedicated RAM access (Tables)
- **AMBA - AHB Master (optional)**
  Tables access on AMBA RAM Interface

Supported File Types

- **Cyclic files**
  Circular file
- **Fixed size files (non-cyclic files)**
  Recording is allowed until file is full
- **Dynamic files**
  File size updated dynamically

File System Management

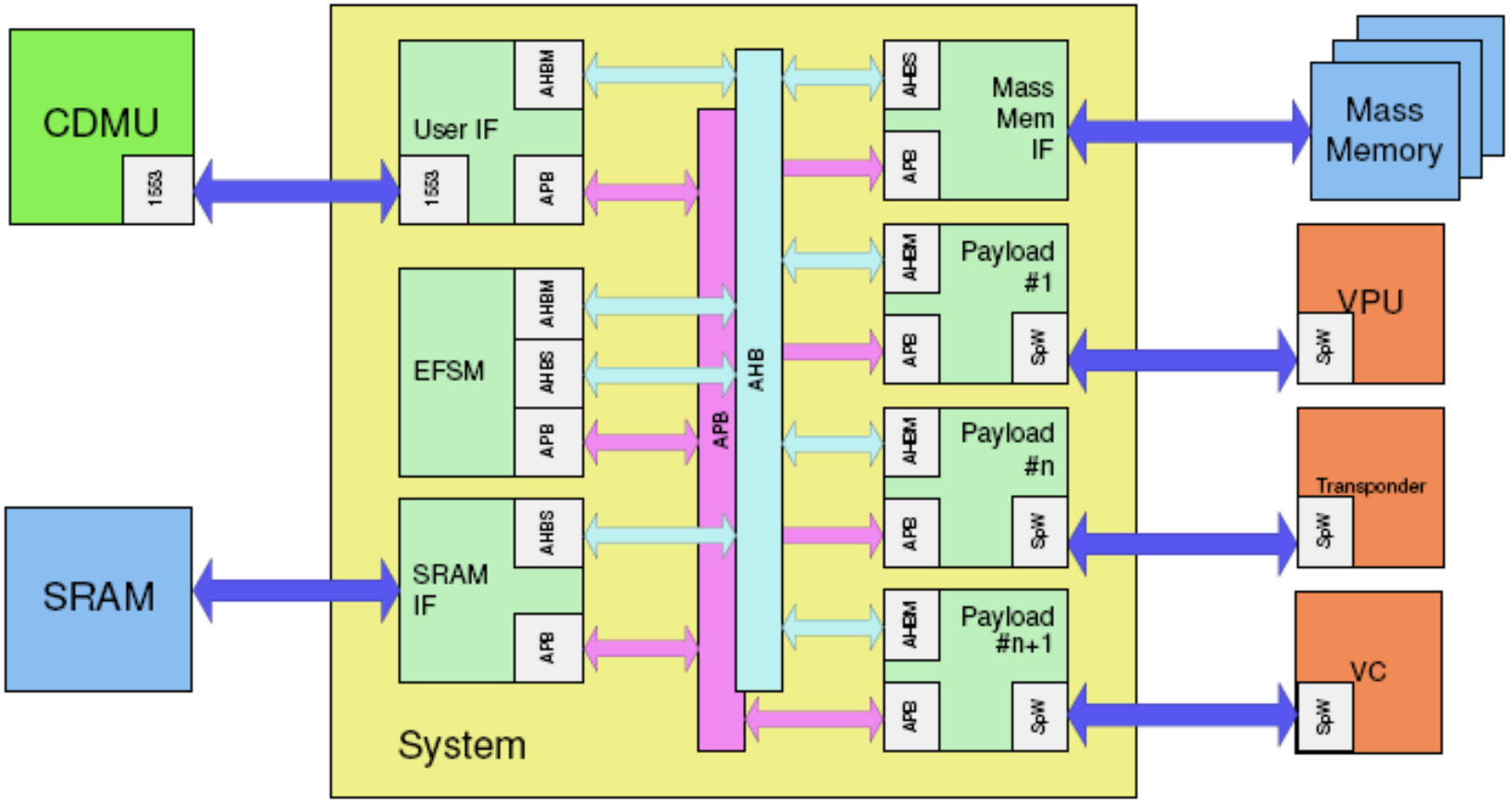
- **Processor based SoC**

  Reduce processor load by handling File System Management

- **Stand-Alone SoC File System handling**

  Autonomous File System Management

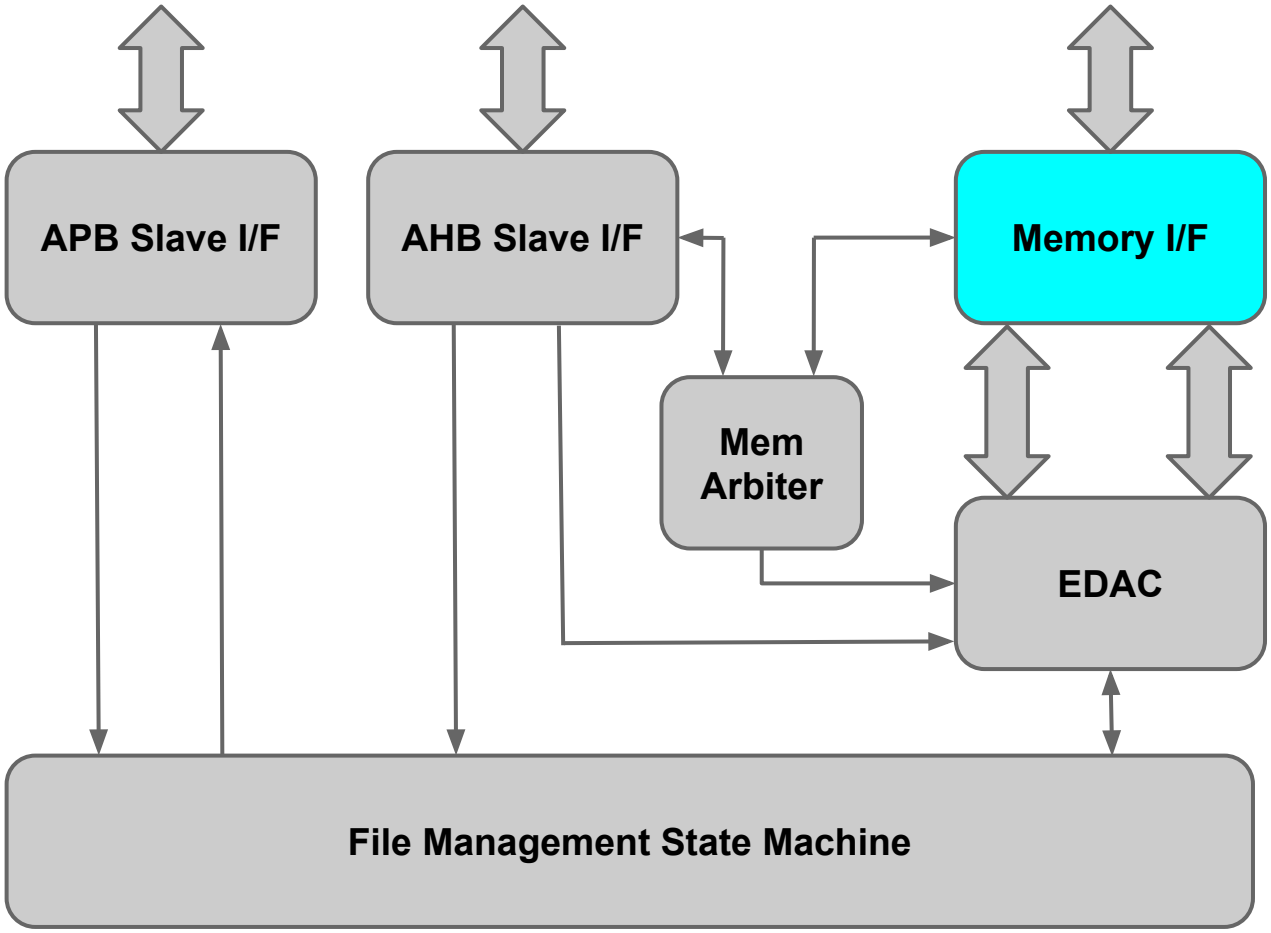
Application Example



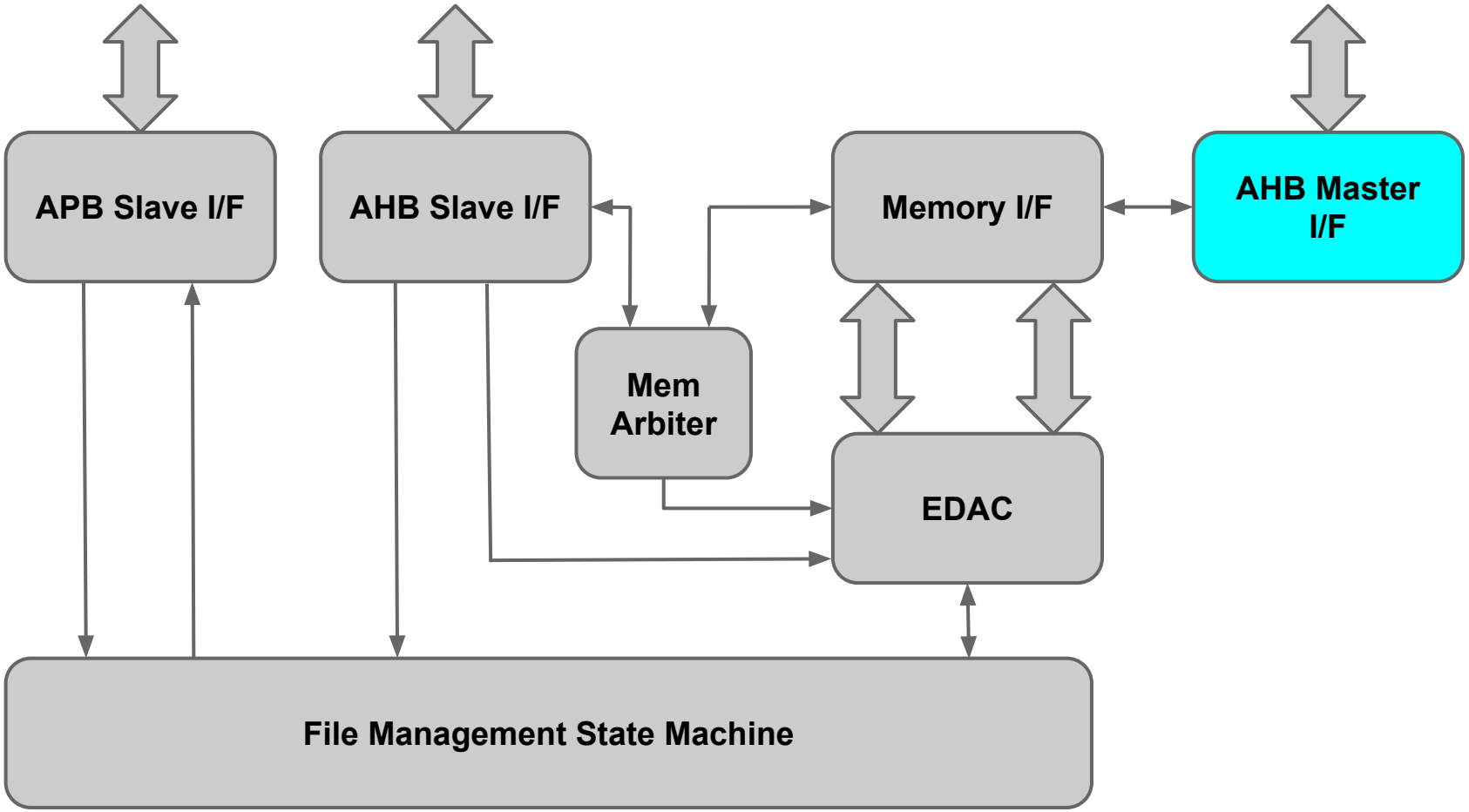
File Management

- **File System Management based on tables:**
  - **Look Up Table (LUT)**
    Link between Application ID and File ID
  - **File Header Table (FHT)**
    Main information for each file
  - **Sector Link Table (SLT)**
    Link between each memory sector
  - **Sector Time Table (STT)**
    Open / Close sector time
  - **Allocation Table (ALT)**
    Sector usage information

IP architecture - Direct Access to Table Memory



IP architecture - Table Memory Access through AMBA



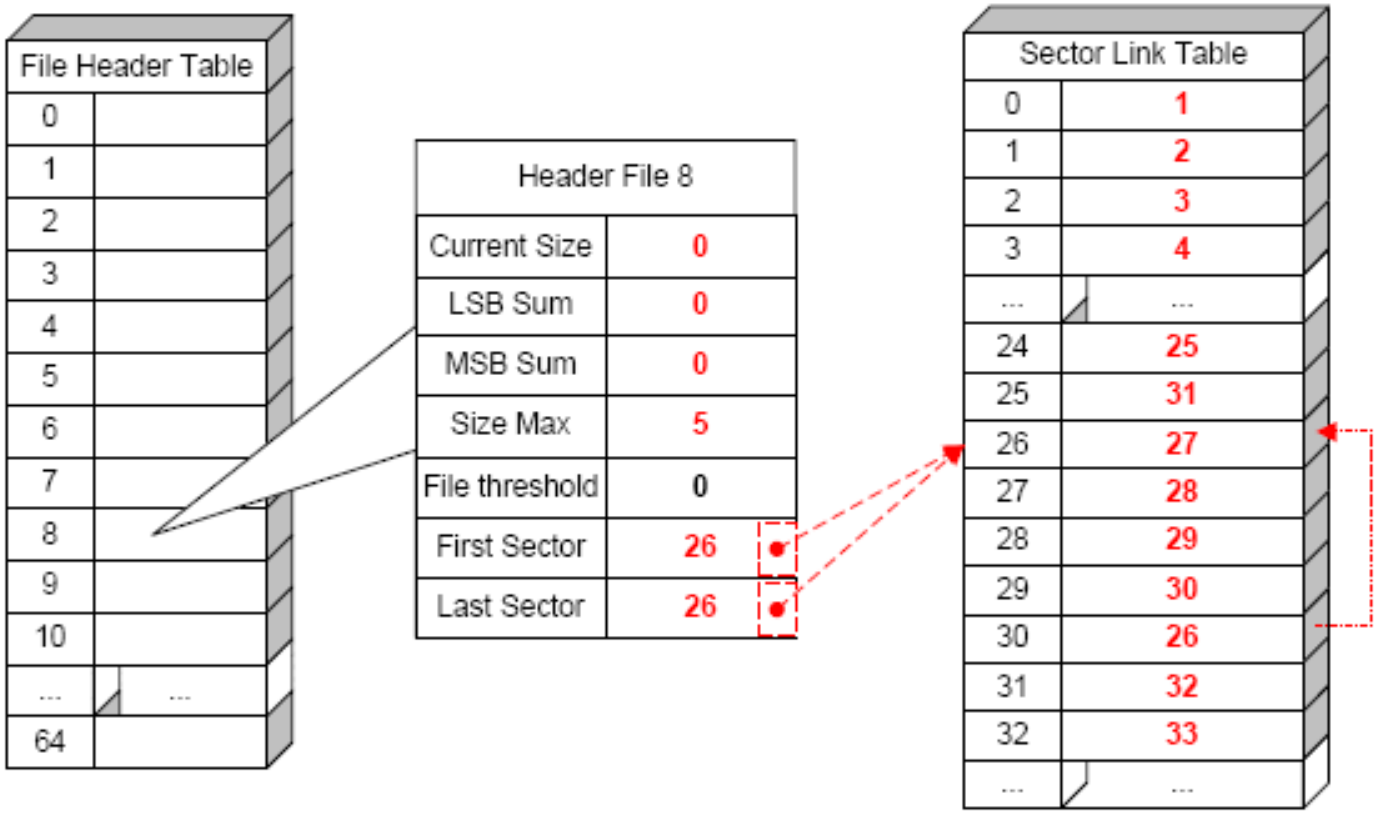
Configurable

- Files (max 2^{12})
- Sectors (max 2^{22})
- Block Size (1-byte to n-bytes)
- User maximum packet size
- AMBA index and address

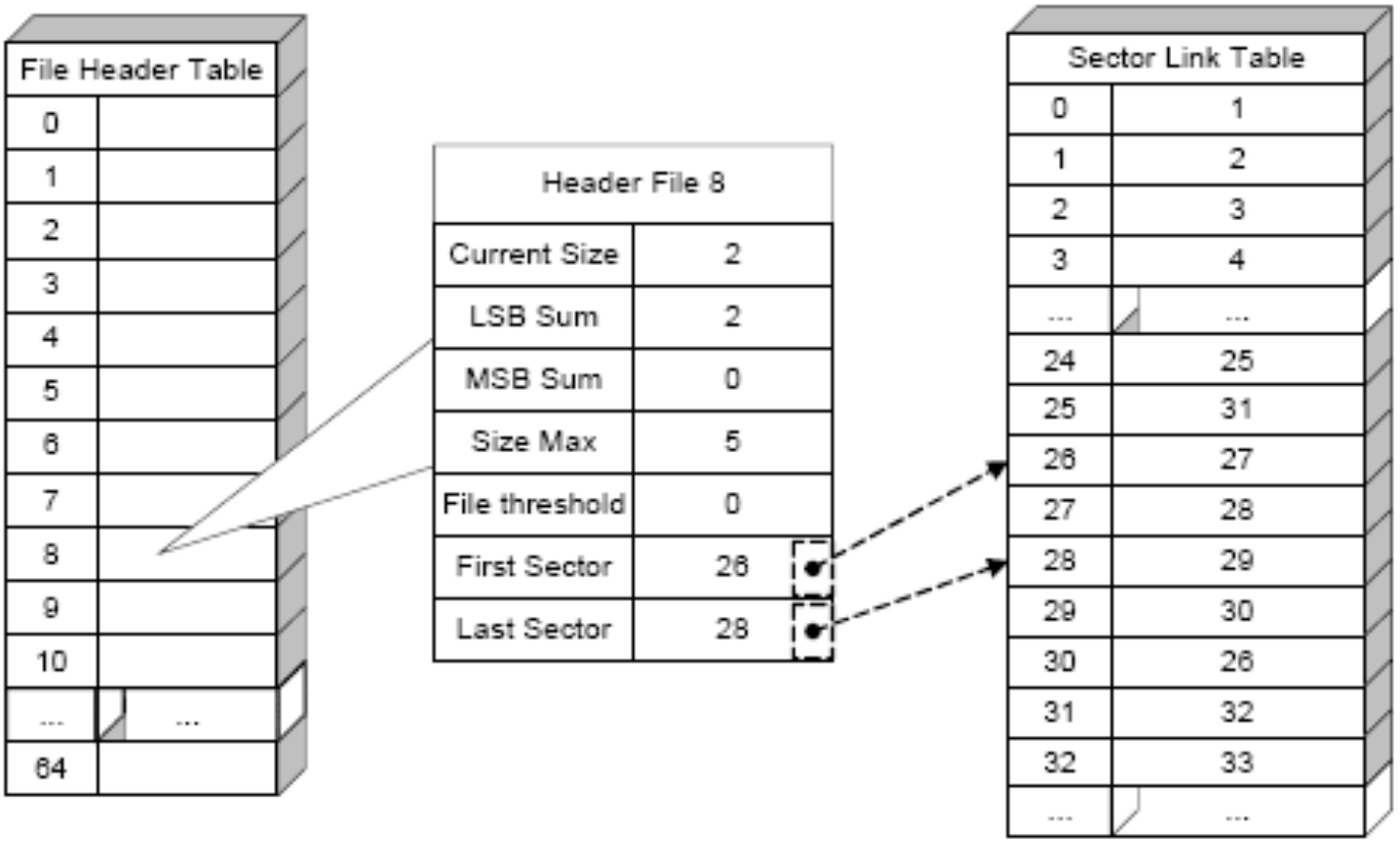
File Management - Principle of operation

- Tables Initialization
- Cyclic File
- Dynamic File

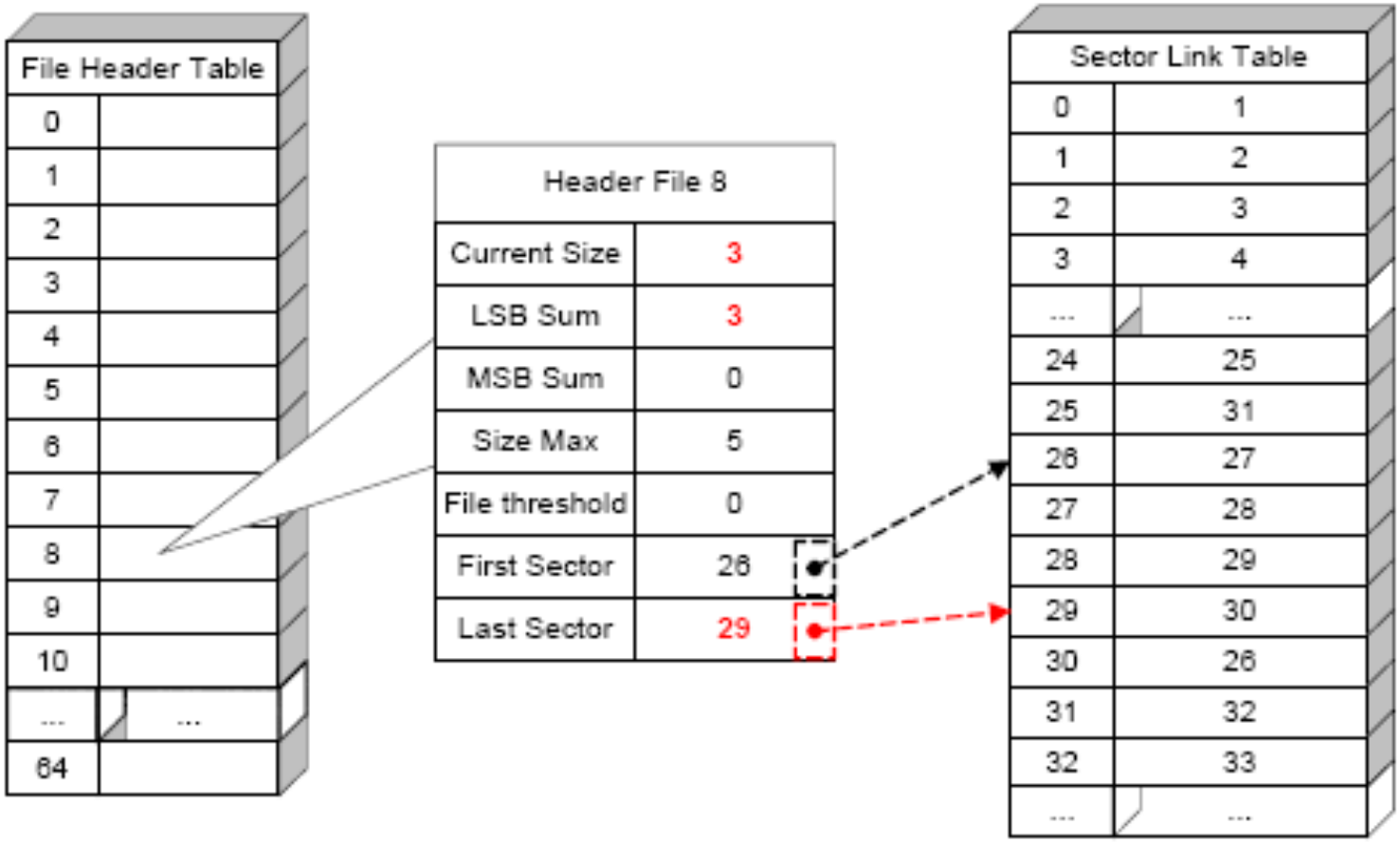
Cyclic File Management - Initialization



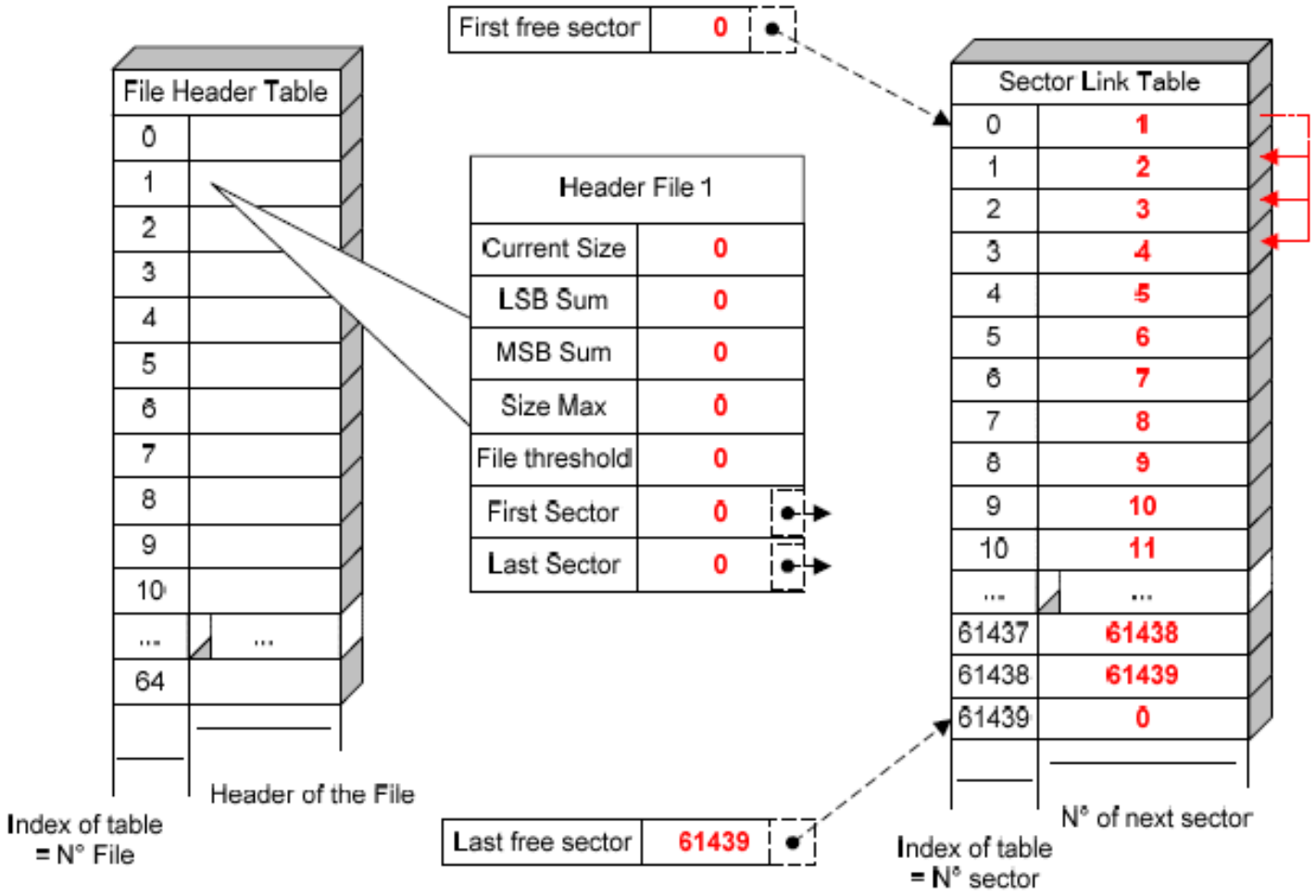
Cyclic File Management - New sector



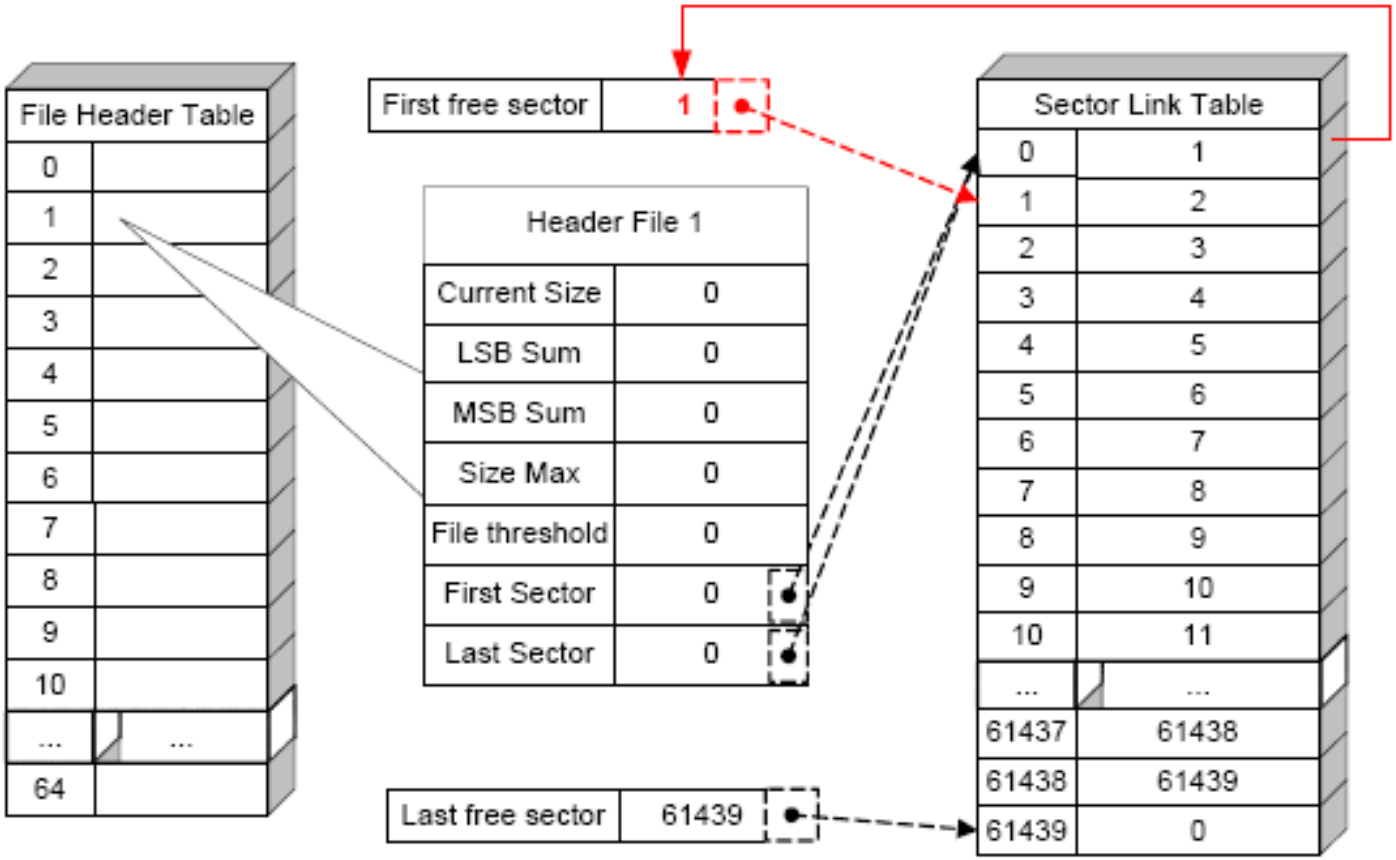
Cyclic File Management - New sector



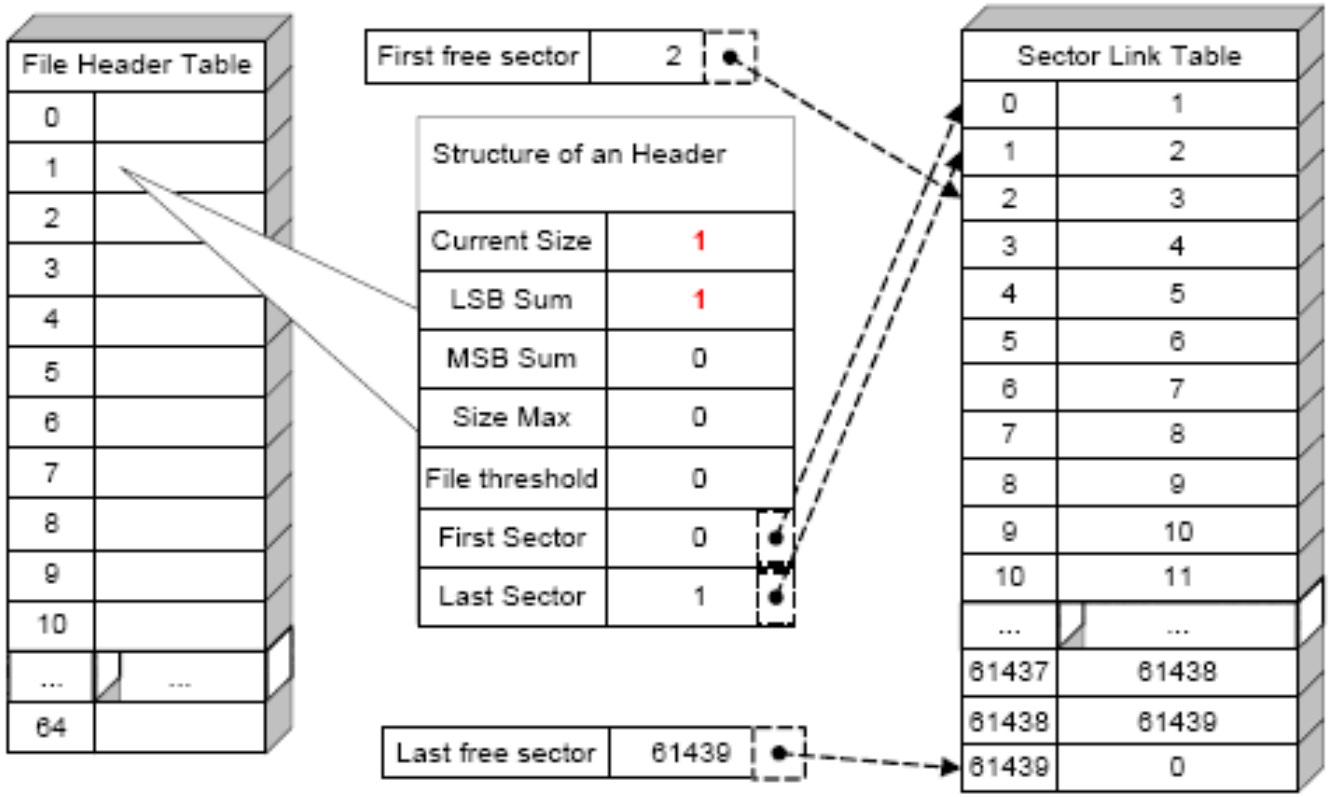
Dynamic File - Initialization



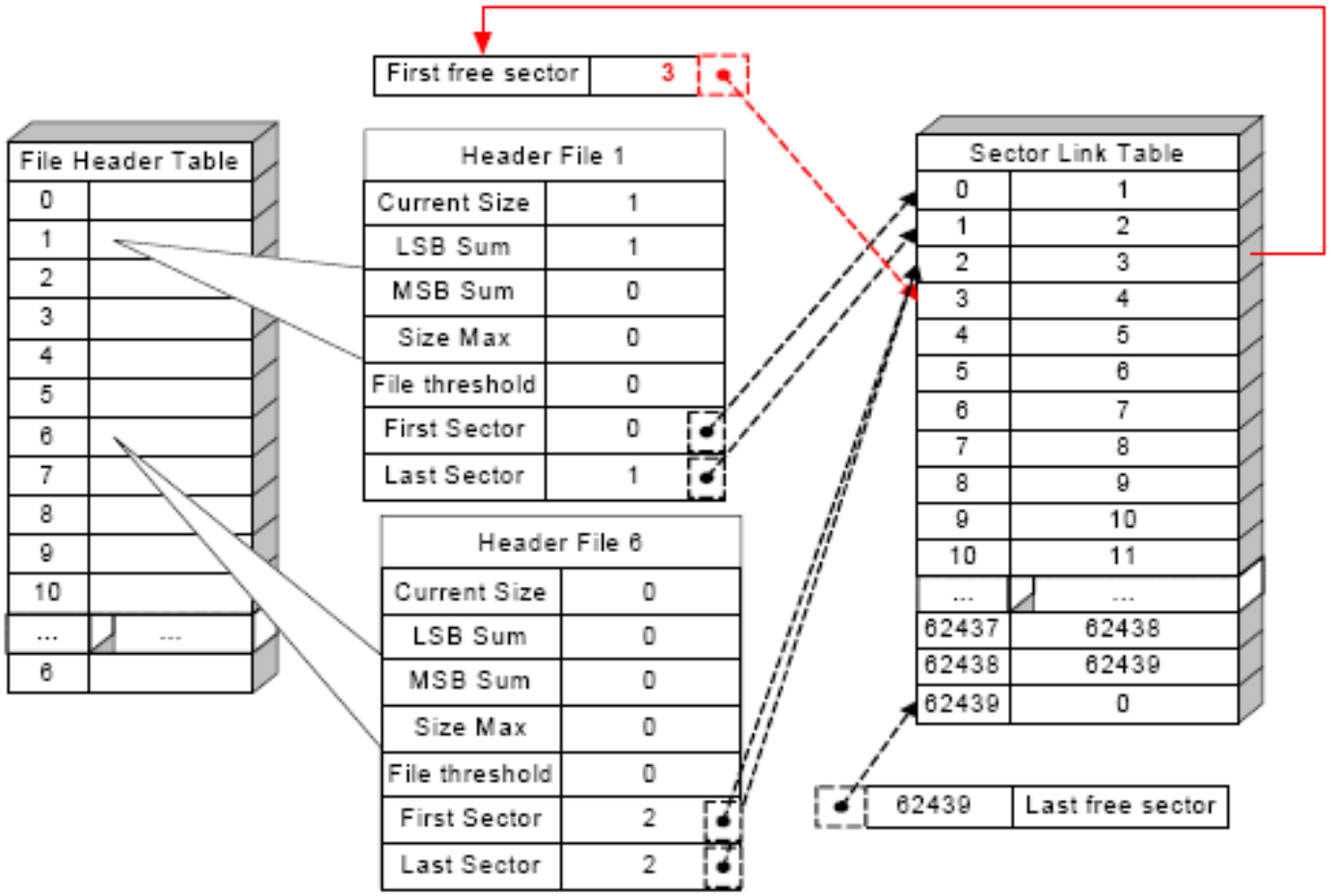
Dynamic File - First sector assignment



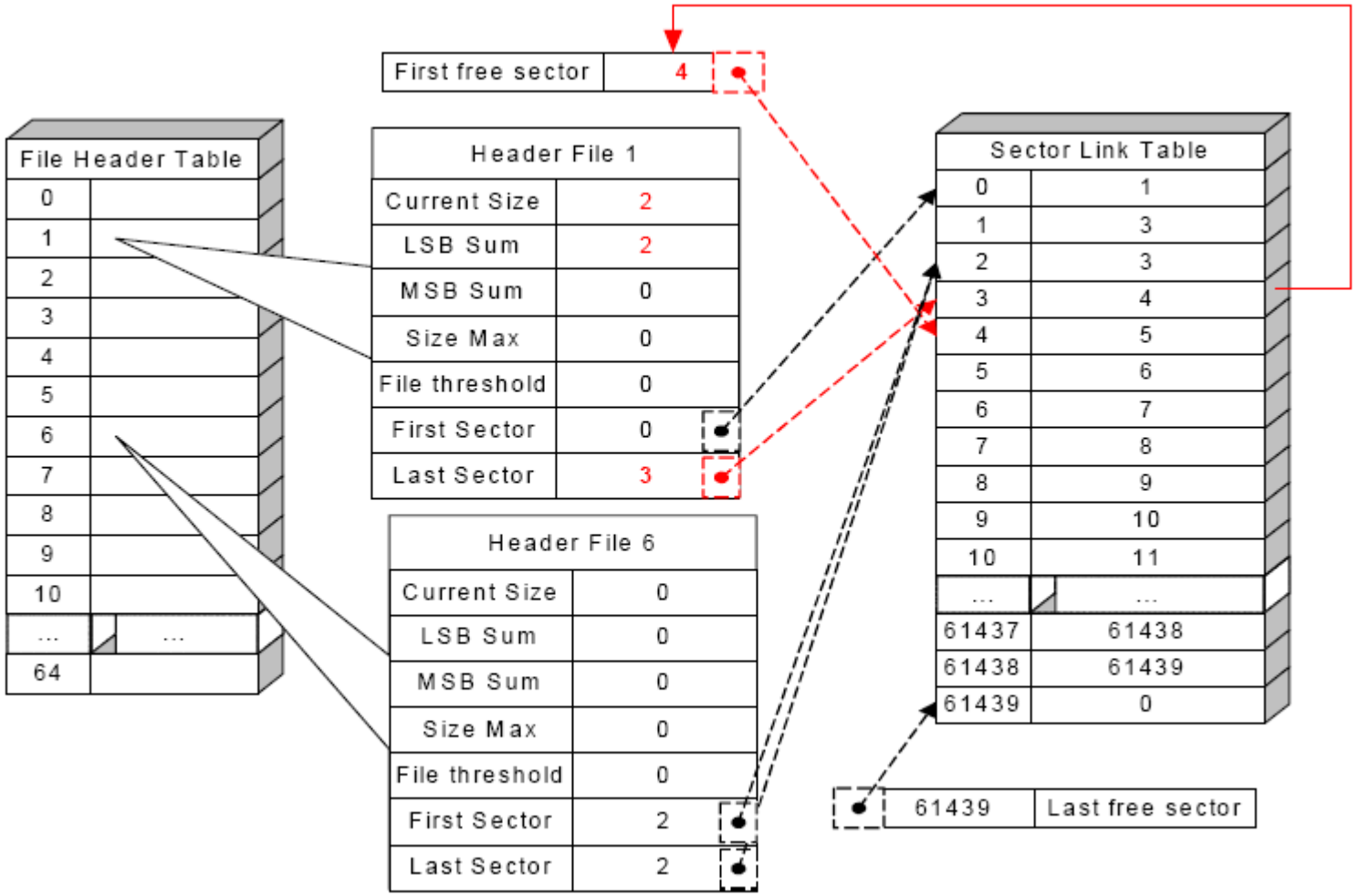
Dynamic File - New packet creating a new sector



Dynamic File - First sector in an additional file



Dynamic File - New sector in file 1



Implementation Results

IP Configuration

256 files, 256 sectors and 256 blocks

EDAC & AHB master interface are enabled

Technology : Microsemi RTAX (RTAX2000SCQ352)

⇒ Ressources Usage:

Core cells: 8% (2'448 cells)

Internal Ram blocks: No RAM Block used

⇒ Performances : 43 MHz

⇒ Response time : 52 clock cycles / 1,3 us @ 40MHz

Implementation Results

IP Configuration

256 files, 256 sectors and 256 blocks

EDAC & AHB master interface are enabled

Technology : XILINX VIRTEX4 (XC4VLX200)

⇒ Ressources Usage:

Core cells: 1% (1'497 LUT)

Internal Ram blocks: No RAM Block used

⇒ Performances : 89 MHz

⇒ Response time : 52 clock cycles / 650 ns @ 80MHz

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Thanks

For Your Attention