A RADIATION TOLERANT LOW POWER SRAM COMPILER IN 65NM CMOS TECHNOLOGY
OUTLINE

Introduction
Specifications
Strategies applied
Architecture
Layout and compiler
Conclusion
TRIGGER SYSTEM IN LHC EXPERIMENTS

Single event is ~1MB data

Collision rate 40 MHz
~40 TB/s of data

▸ not all events are interesting for physics

The trigger system selects only interesting events

▸ reduces data shipped out of the experiments

▸ Average trigger rate ~100 kHz

imec
MOTIVATION

Trigger system evaluation ~ μs
during: data is stored in a FIFO
- FIFOs in front-end ASICs embedded as SRAM blocks

LHC luminosity upgrade:
stringent constraints to FE detector
- Low-power, fast data rates, small pixels, radiation-hard …
- 65nm CMOS is the chosen technology
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SPECIFICATIONS

- Pseudo dual port behavior
- 65 nm technology with standard Vt devices
- 4 metal layers used
- Supply 1.2 V ± 10%
- Power consumption 24uW/MHz (32Kbit)
- Temperature range: -40 ... 125°C
- Max frequency 80 MHz
- TID hardening > 200 Mrad
- LET threshold > 15 MeVcm²/mg
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TIMING BEHAVIOR

Pseudo dual port

- 1 master clock
- 2 address inputs (R/W)
- 1 data port (I/O)

SRAM

$2^m \text{ words} \times n \text{ bit}$

$\begin{align*}
\text{RA}_{m:1} \\
\text{WA}_{m:1} \\
\text{WD}_{n:1} \\
\text{REN} \\
\text{WEN} \\
\text{CLK} \\
\text{RD}_{n:1}
\end{align*}$
LOW POWER

Multiple techniques

▸ Split word lines
  - Global word lines
  - Local word lines with optimized buffer

▸ Discharge level of bit-lines reduced to 100mV
  - Timing optimized by self-timing (dummy memory)
RADIATION HARDENING

TID
- Minimum size MOS > DRC minimum
- p+ guard bands between n-type regions

SEE
- Drive strength hardening
- DICE FF
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ARCHITECTURE

ADDRESS DECODING

3 LSB : bit interleaving decoding
INT-B : word line decoding
1-2 MSB : row decoding

Aspect ratio improvement

\[
\text{#mosaic rows} = \sqrt{\frac{\text{current aspect ratio}}{\text{target aspect ratio}}}
\]
MEMORY BLOCK

2 flavors

▸ 512 words x 8 bits
  - 64 word lines
▸ 128 words x 8 bits
  - 16 word lines

Split word line

▸ Local optimized buffers

8 bit interleaving
MEMORY CELL

Standard 6T cell

TID hardening:
  Not minimal width of MOS
  P+ guard band

Verified PVT

SNM > 18% of Supply voltage
DICE FLIP-FLOP

Corner stone of SEU hardening

Output redundancy
- A=C and B=D

C-Cell
- Absorbs SEU by going high impedance

Location in the design:
- Stores addresses
- Stores I/O data
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2 dedicated floorplans
- 128 words memory block
- 512 words memory block

2 SRAMs on test chip
- 1024 words x 32 bits ≈ 450µm x 380µm
- 128 words x 8 bits ≈ 245µm x 70µm
- Post layout verified in all PVT corners
COMPILER

2 layered system

- VDL for easy planning
  - Dimensions
  - Buffer size
- IL generates views
  - Modular structure

Virtual design layer

Implementation layer

OPEN ACCESS DATABASE

SKILL

JAVA

LEX

PEX

LIB

DOC

imet
CONCLUSION

Presented the design of a SRAM compiler

- 65nm CMOS technology
- Pseudo dual port
- Low power
- Radiation hardened against TID and SEE
- 2 flavors in memory blocks for optimal scalability
- 2 layered compiler
  - Virtual design
  - Modular implementation layer