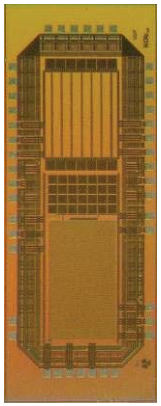
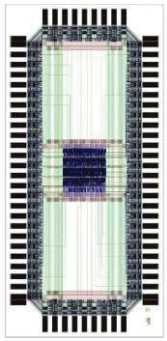
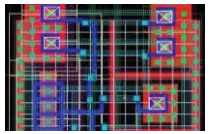
DARE User Day

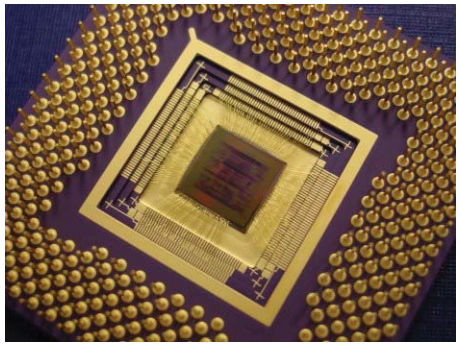


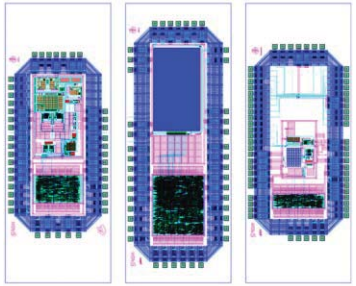
ESA and DARE Technology

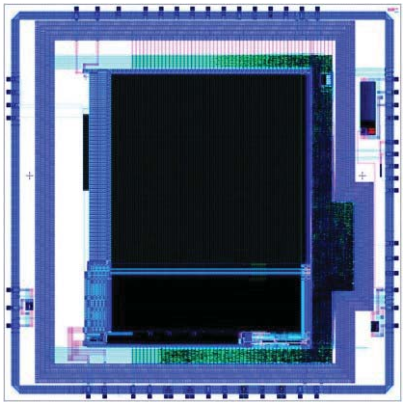


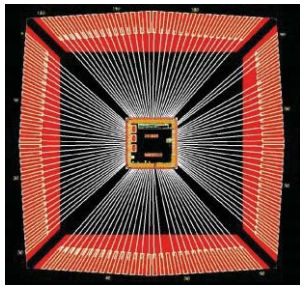
A. Fernandez Leon / B. Glass / R. Jansen
ESA TEC-EDM
9/Dec/2014











Design **A**gainst **R**adiations **E**ffects

WHEN did we start, and **WHY**

- end of the **90's** , **space ASICs:**

- State-of-the-art: Atmel(F) **0.5µm** under qualification, next 0.35µm; Mitel-ABB HAFFO(Sweden), Mitel-GEC Plessey(UK) **1-0.8µm**

- problem: rad-hard-by-"*process*" (e.g. Silicon-on-Sapphire) European Fabs & space components **discontinuation** + better performance -> **smaller** feature sizes wanted

- Possible solution: rad-hard-by-"*design*" (libraries) + commercial Fabs/processes

- tech choice adopted: IMEC(B) rad-hard libraries + UMC 180nm (fab in Taiwan), advanced node, price competitive (Europractice MPW)

ESA and DARE Technology:

WHAT

•1st successful proof-of-concept in 2000, then a series of contracts to consolidate a **rad-hard library by IMEC(B)** tailored for CMOS 180nm UMC, and a new **space ASIC offer**

•Quickly became attractive for **Analogue and Mixed-signal**, due to IMEC/Europractice/UMC full custom options and flexibility

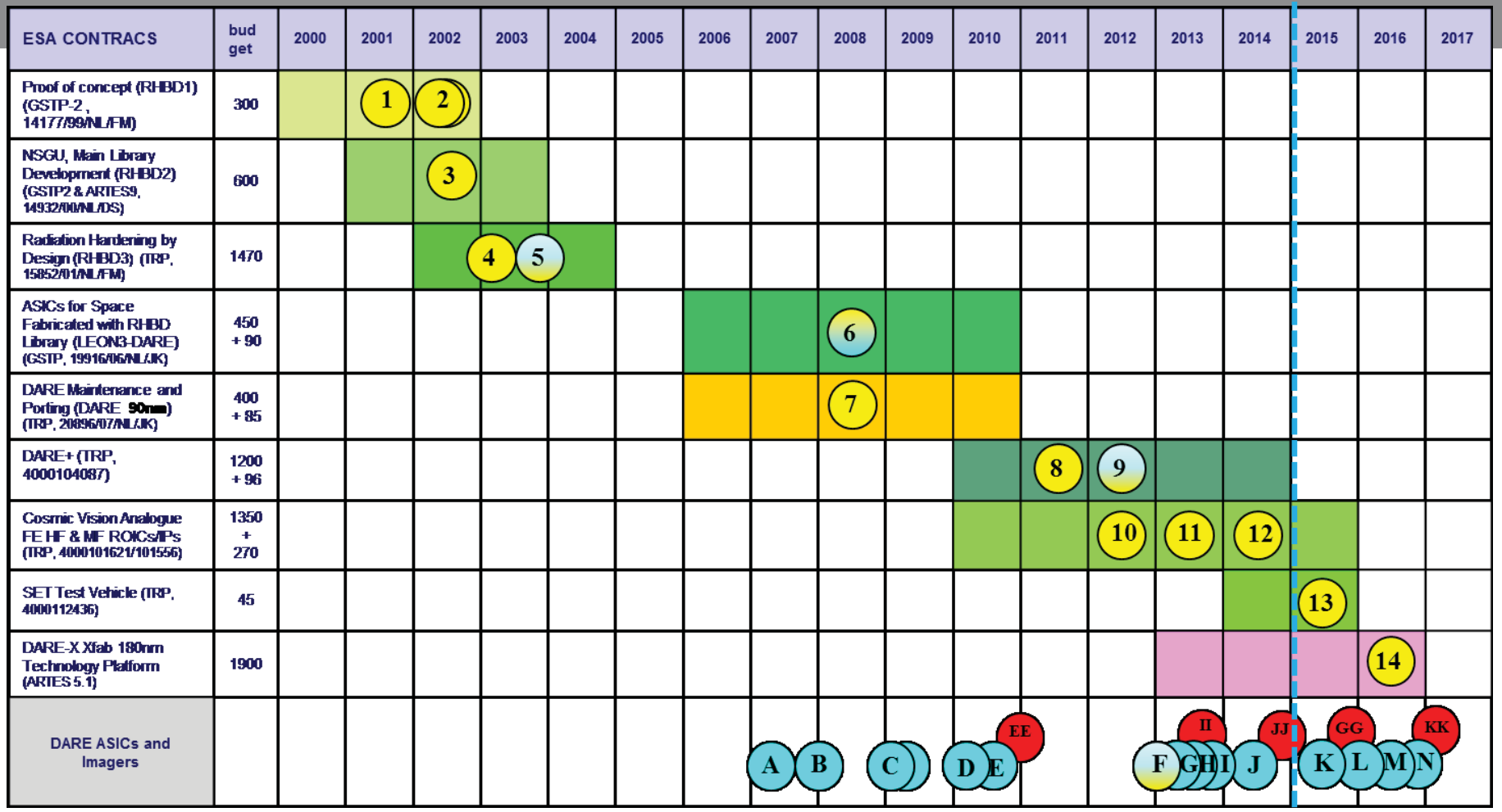
•Also for **sensors** including mixed-signal read-outs, thanks to UMC CMOS Image Sensor (CIS) process

•After a small contrat on UMC 90nm (now on hold), new developments now on **Xfab (Taiwan) 180nm ("DARE-X")**, to bring in **HV, NVM.**

•Also preparing new A&MS platforms **DARE35 (OnSemi I3T80)** and **DARE65 (TSMC)**

•First cases of **analogue IP Cores reuse** (implemented on DARE) are happening now.

ESA and DARE Technology: HOW



TEST CHIPS:

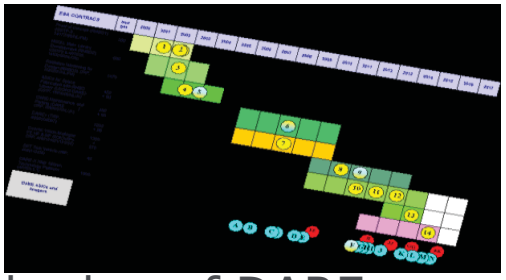
1- Testchip, **2 –** OZONE variants, **3 –** NSGU NASIG with DARE test block, **4 –** DIE HARD, **5 -** DROM (Alcatel), **6 -** LEON3DARE (A. Gaisler), **7 –** DIE HARDER, **8 –** DTV, LTV , **9 –** Cosmic Vision application ASIC (Recore Xentium DSP-monocore), **10/11/12 –** Cosmic Vision HF and MF test chips & IP Cores (Arquimea, IMSE, CNM – E) , **13 –** SET Test Vehicle, **14 -** DARE-X TV (Xfab 180nm, TAS-ETCA)

CUSTOMER ASICs and Imagers:

A – Shamrock (SRON-NL, for Exomars), **B -** HIT (Austrian Aerospace), **C -** KNUT1,2 (TESAT, SmallGEO), **D –** Sun-Sensor-on-Chip (CMOSIS-B, GSTP), **E-** DRA REDSAT (ARTES5, CASA-E, SmallGEO), **EE –** Sun Sensor on a Chip-1st (CMOSIS-B) , **F –** ESA CAN transceiver, **G,H –** DPC G1 run1a & run1b (TAS-ETCA, ARTES), **I –** SpaceWire-16X (A. Gaisler, GSTP), **II –** LFNIR/SWIR Detector (Caeleste-B), **J –** LVDS Repeater (A. Gaisler, GSTP) , **JJ –** Sun Sensor on a Chip-2nd (CMOSIS-B), **K –** 16b ADC (Alter-E, TRP-GSTP), **KK –** LCMS2 Faint Star 1st (CMOSIS-B), **L -** CLP (Sabca-B, GSTP), **M -** Scalable Sensor Data Processor (TAS-E, CTP), **N –** Space Microcontroller (A. Gaisler, TRP), **NN –** LCMS2 Faint Star 2nd (CMOSIS-B).

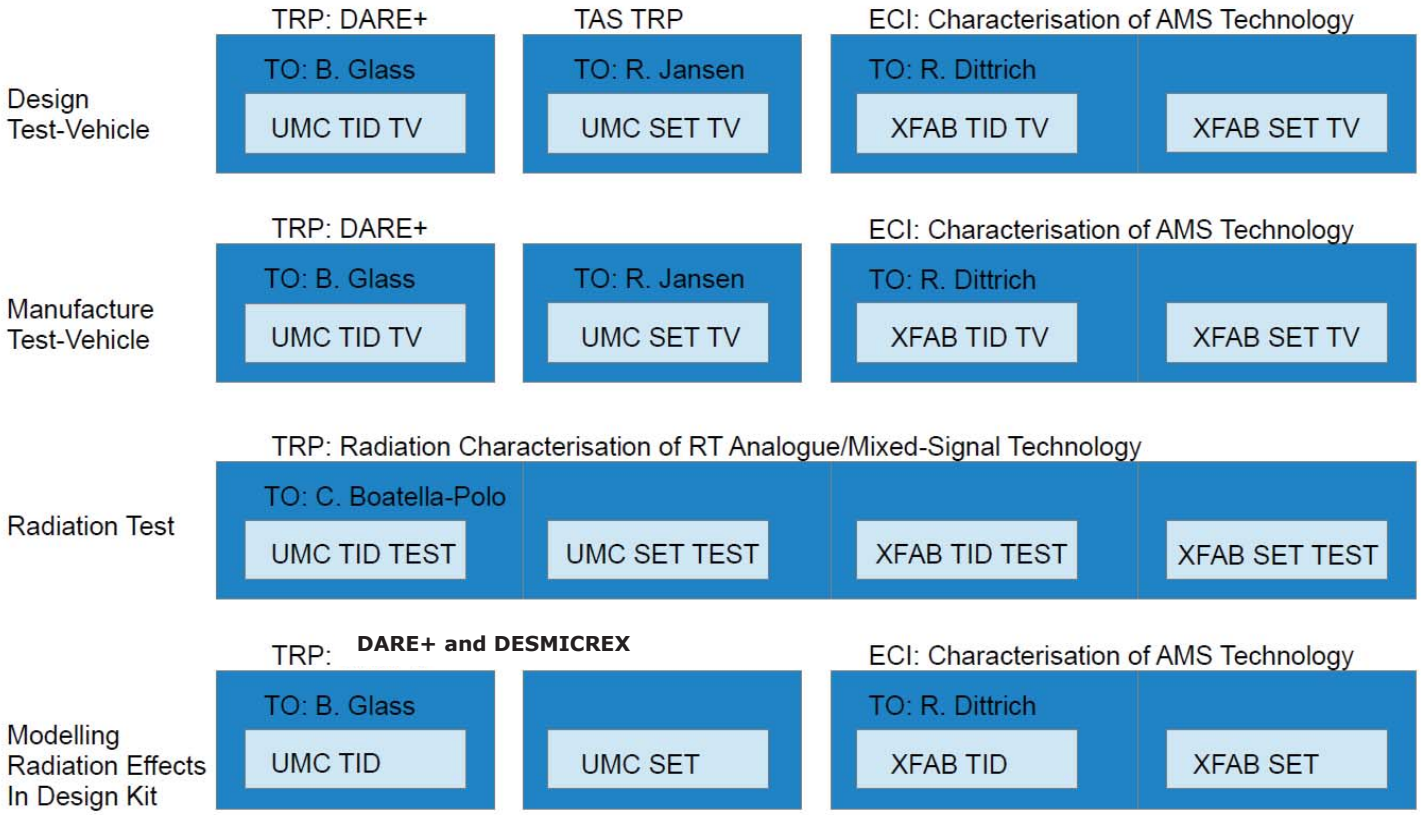
ESA and DARE Technology: HOW

- 8 M€ in 16 years in ESA technology contracts (TRP, GSTP, CTP, ARTES)
  - > 14 test chips, >10 customer ASICs 3 sensors
  - 4 ASICs , 2 sensors in preparation



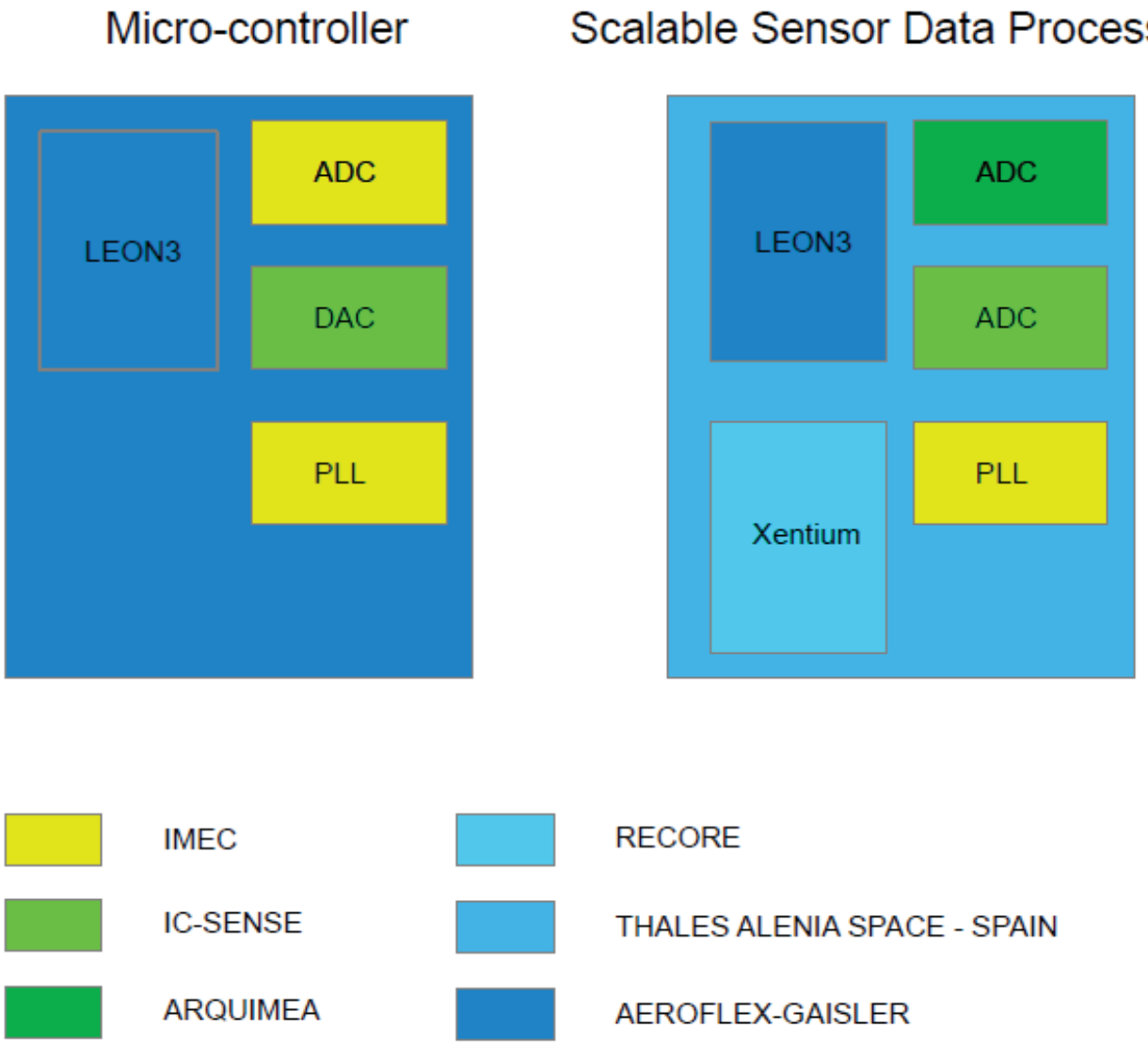
- IMEC(B)'s own parallel activities & investment. IMEC is the broker of DARE technology to customers.
- Multiple companies involved in:
  - **Design** of test chips (with basic **library elements** and larger **IP Cores**) and **customer chips**
  - **Tests**: Functional, electrical, radiation, life-time tests of the test vehicles and customer chips
- Dissemination: ESA and Europractice webs, AMICSA workshops (2006-14), multiple conf (RADECS, SEE symp, etc), 1st DARE User Day (Feb 15th 2011) and today

Technology Characterisation

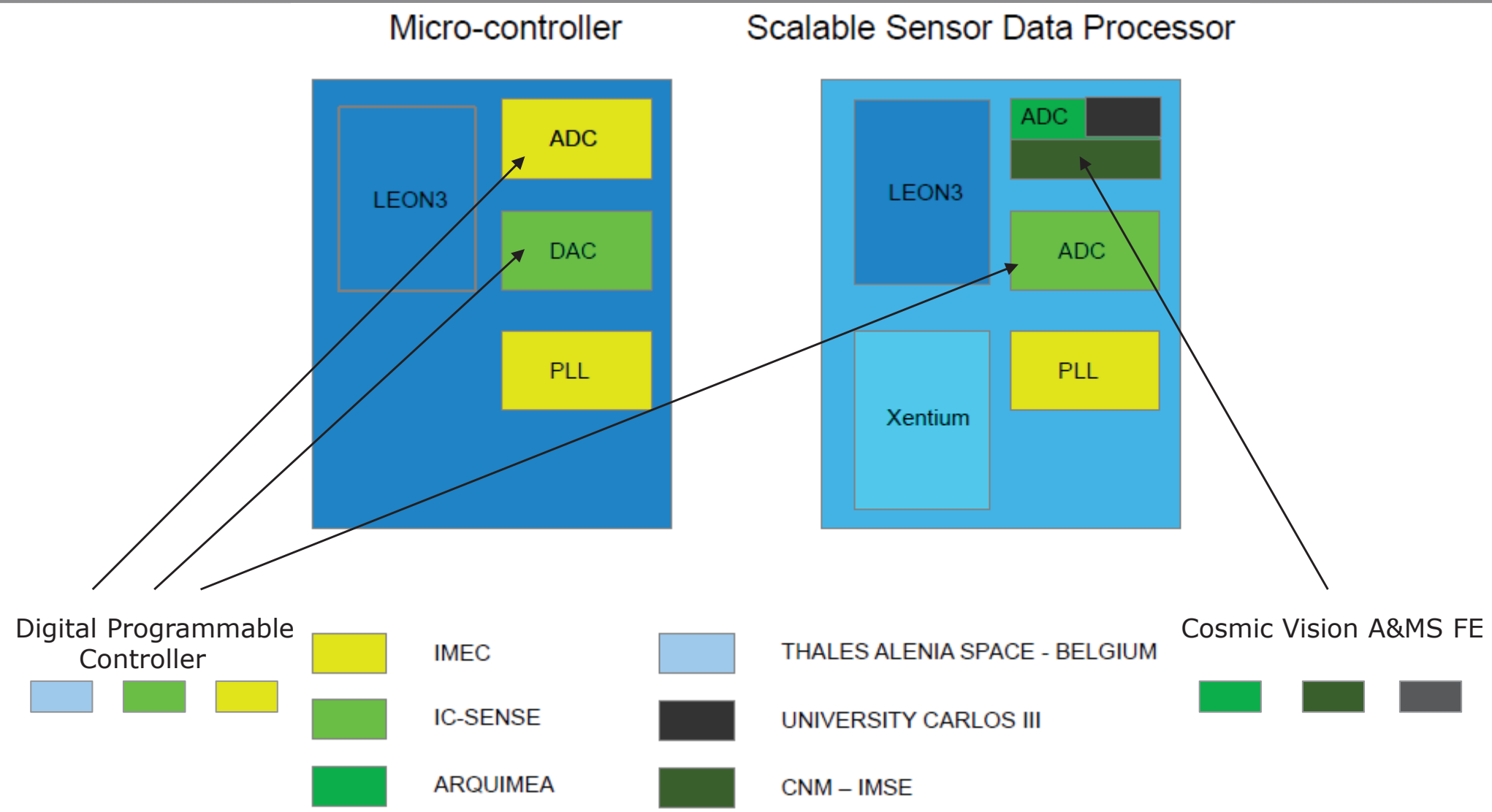


UMC = UMC 180nm CMOS
XFAB = XFAB 180nm CMOS XH

Technology Building Blocks – A&MS IP Cores



Technology Building Blocks – A&MS IP Cores



Technology Building Blocks – A&MS IP Cores

Issues of A&MS IP Cores

1. Efficient procurement
2. Effective integration and verification
3. Effective testing and validation
4. Effective creation

A rich A&MS IP Core Library increases the value of the Technology

Workshop to improve the availability/reuse of A&MS IP Cores