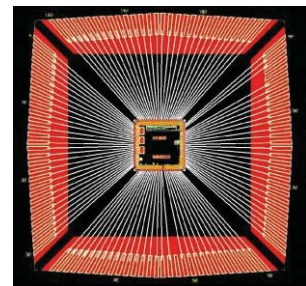
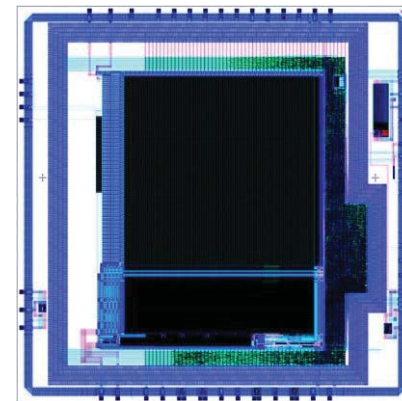
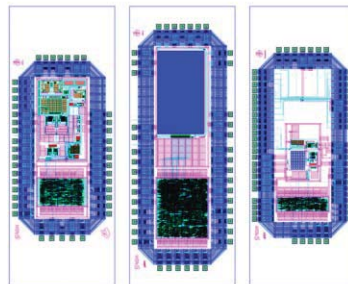
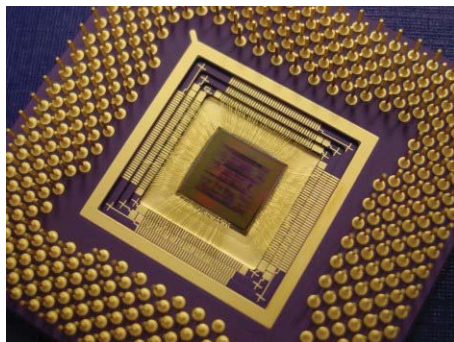
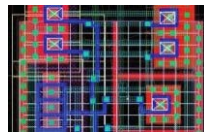
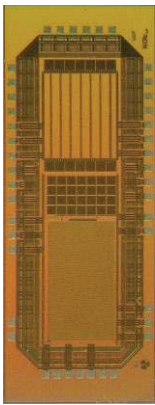
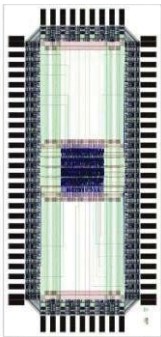


DARE User Day



ESA and DARE Technology

A. Fernandez Leon / B. Glass / R. Jansen
ESA TEC-EDM
9/Dec/2014



Design Against Radiations Effects

WHEN did we start, and **WHY**

- end of the **90's** , **space ASICs**:
- State-of-the-art: Atmel(F) **0.5 μ m** under qualification, next 0.35 μ m; Mitel-ABB HAFFO(Sweden), Mitel-GEC Plessey(UK) **1-0.8 μ m**
- problem: rad-hard-by-"*process*" (e.g. Silicon-on-Sapphire) European Fabs & space components **discontinuation** + better performance -> **smaller** feature sizes wanted
- Possible solution: rad-hard-by-"*design*" (libraries) + commercial Fabs/processes
- tech choice adopted: IMEC(B) rad-hard libraries + UMC 180nm (fab in Taiwan), advanced node, price competitive (Europractice MPW)

WHAT

- 1st successful proof-of-concept in 2000, then a series of contracts to consolidate a **rad-hard library by IMEC(B)** tailored for CMOS 180nm UMC, and a new **space ASIC offer**
- Quickly became attractive for **Analogue and Mixed-signal**, due to IMEC/Europractice/UMC full custom options and flexibility
- Also for **sensors** including mixed-signal read-outs, thanks to UMC CMOS Image Sensor (CIS) process
- After a small contract on UMC 90nm (now on hold), new developments now on **Xfab (Taiwan) 180nm ("DARE-X")**, to bring in **HV, NVM**.
- Also preparing new A&MS platforms **DARE35 (OnSemi I3T80)** and **DARE65 (TSMC)**
- First cases of **analogue IP Cores reuse** (implemented on DARE) are happening now.

ESA and DARE Technology: HOW



ESA CONTRACS	budget	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017							
Proof of concept (RHBD1) (GSTP-2, 14177/99/NL/FM)	300		1	2																						
NSGU, Main Library Development (RHBD2) (GSTP2 & ARTES9, 14932/00/NL/DS)	600			3																						
Radiation Hardening by Design (RHBD3) (TRP, 15852/01/NL/FM)	1470				4	5																				
ASICs for Space Fabricated with RHBD Library (LEON3-DARE) (GSTP, 19916/06/NL/JK)	450 + 90									6																
DARE Maintenance and Porting (DARE 90nm) (TRP, 20896/07/NL/JK)	400 + 85								7																	
DARE+ (TRP, 4000104087)	1200 + 96												8	9												
Cosmic Vision Analogue FE HF & MF ROICs/IPs (TRP, 4000101621/101556)	1350 + 270													10	11	12										
SET Test Vehicle (TRP, 4000112436)	45																13									
DARE-X Xfab 180nm Technology Platform (ARTES 5.1)	1900																		14							
DARE ASICs and Imagers										A	B	C	D	E	EE	F	G	H	I	J	JJ	GG	KK	L	M	N

TEST CHIPS:

1- Testchip, 2 – OZONE variants, 3 – NSGU NASIG with DARE test block, 4 – DIE HARD, 5 - DROM (Alcatel), 6 - LEON3DARE (A. Gaisler), 7 – DIE HARDER, 8 – DTV, LTV , 9 – Cosmic Vision application ASIC (Recore Xentium DSP-monocore), 10/11/12 – Cosmic Vision HF and MF test chips & IP Cores (Arquimea, IMSE, CNM – E) , 13 – SET Test Vehicle, 14 - DARE-X TV (Xfab 180nm, TAS-ETCA)

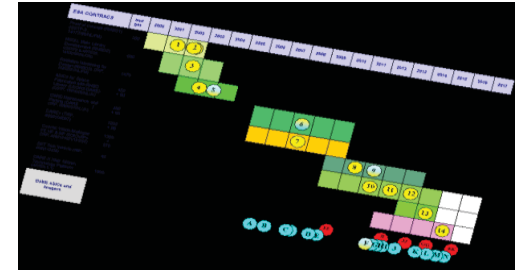
CUSTOMER ASICs and Imagers:

A – Shamrock (SRON-NL, for Exomars), B - HIT (Austrian Aerospace), C - KNUT1,2 (TESAT, SmallGEO), D – Sun-Sensor-on-Chip (CMOSIS-B, GSTP), E- DRA REDSAT (ARTES5, CASA-E, SmallGEO), EE – Sun Sensor on a Chip-1st (CMOSIS-B), F – ESA CAN transceiver, G,H – DPC G1 run1a & run1b (TAS-ETCA, ARTES), I – SpaceWire-16X (A. Gaisler, GSTP), II – LFNIR/SWIR Detector (Caeleste-B), J – LVDS Repeater (A. Gaisler, GSTP) , JJ – Sun Sensor on a Chip-2nd (CMOSIS-B), K – 16b ADC (Alter-E, TRP-GSTP), KK – LCMS2 Faint Star 1st (CMOSIS-B), L - CLP (Sabca-B, GSTP), M - Scalable Sensor Data Processor (TAS-E, CTP), N – Space Microcontroller (A. Gaisler, TRP), NN – LCMS2 Faint Star 2nd (CMOSIS-B).

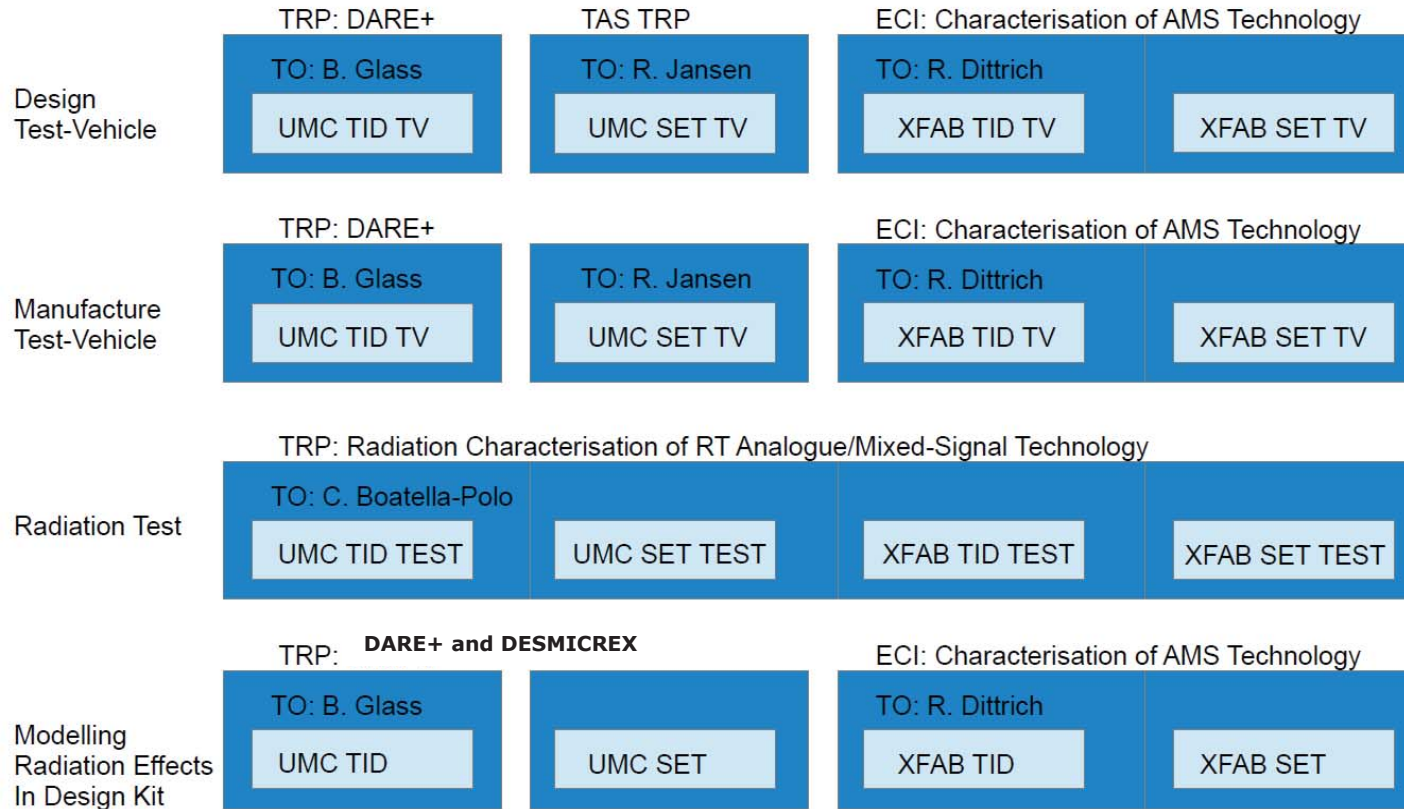
ESA and DARE Technology: **HOW**



- 8 M€ in 16 years in ESA technology contracts (TRP, GSTP, CTP, ARTES)
 - > 14 test chips, >10 customer ASICs 3 sensors
 - 4 ASICs , 2 sensors in preparation
- IMEC(B)'s own parallel activities & investment. IMEC is the broker of DARE technology to customers.
- Multiple companies involved in:
 - **Design** of test chips (with basic **library elements** and larger **IP Cores**) and **customer chips**
 - **Tests**: Functional, electrical, radiation, life-time tests of the test vehicles and customer chips
- Dissemination: ESA and Europractice webs, AMICSA workshops (2006-14), multiple conf (RADECS, SEE symp, etc), 1st DARE User Day (Feb 15th 2011) and today

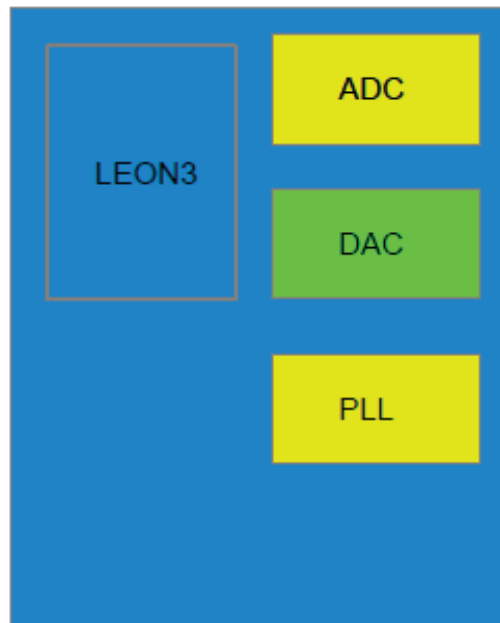


Technology Characterisation

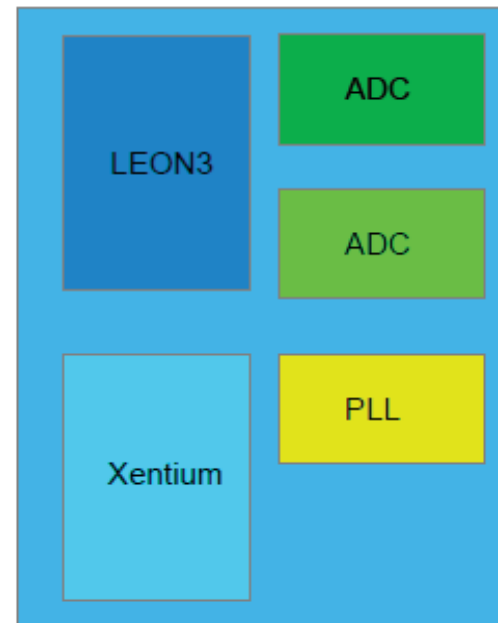


UMC = UMC 180nm CMOS
XFAB = XFAB 180nm CMOS XH

Micro-controller



Scalable Sensor Data Processor



IMEC



IC-SENSE



ARQUIMEA



RECORE



THALES ALENIA SPACE - SPAIN



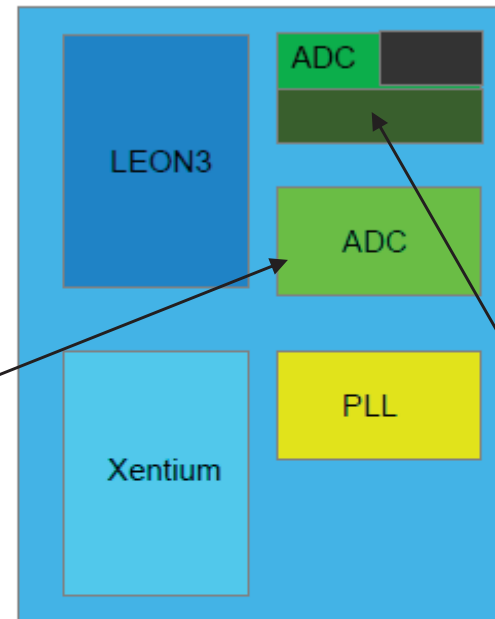
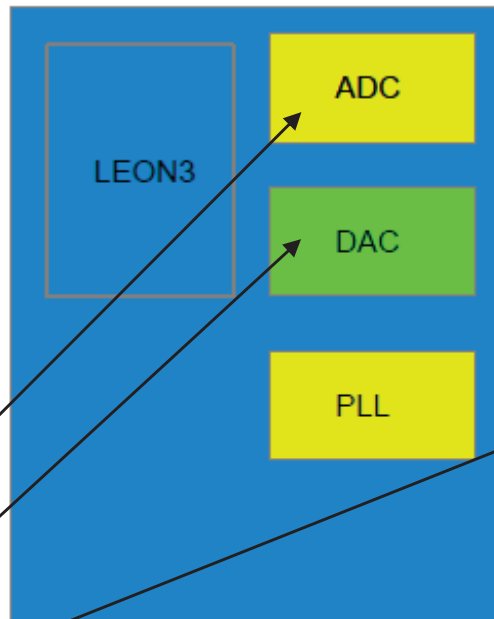
AEROFLEX-GAISLER

Technology Building Blocks – A&MS IP Cores



Micro-controller

Scalable Sensor Data Processor



Digital Programmable Controller



IMEC



IC-SENSE



ARQUIMEA



THALES ALENIA SPACE - BELGIUM



UNIVERSITY CARLOS III



CNM - IMSE

Cosmic Vision A&MS FE



Issues of A&MS IP Cores

1. Efficient procurement
2. Effective integration and verification
3. Effective testing and validation
4. Effective creation

A rich A&MS IP Core Library increases the value of the Technology

Workshop to improve the availability/reuse of A&MS IP Cores