DARE User Day 2014-12-08
@ ESTEC, Noordwijk, the Netherlands

RADIATION-HARD & CRYOGENIC COMPANION CHIP FOR HIGH-END SCIENTIFIC IMAGE SENSORS
Outline

• About Easics
• Chip Requirements: ESA ITT
• Chip Architecture
• **Digital Design** using imec/ESA DARE library
• Test Setup
• Conclusions & Next Steps
• Q & A
About Easics

Easics is a System-on-Chip design company, targeting designs in FPGAs and digital & mixed-signal ASICs.

Easics designs reliable and scalable high-performance & low-power embedded systems.

Located at the Arenberg Science Park, Leuven, Belgium
3 Pillars of Easics
About Easics

Customers:
• OEMs: electronics, optics, mechanics
• Semiconductor companies
• Analog / mixed-signal IC design houses

Markets:
imaging / image sensors, aerospace, industrial, medical / healthcare, multimedia, wireless & wired connectivity, broadcast, measurement equipment
**Why an ASIC?**

To operate imagers

** Analog domain**
- Signal conditioning
- Analog to digital converters
- Regulated power supply
- Bias voltage/current references

** Digital domain**
- Digital control core
- Memory & Clock
- Data Communication

[Z.Zhao.SDA'05]
Why an ASIC?

Camera Module

- Analog Pixel Data
- Clocks and Control
- Configuration SPI
- Monitoring
- Bias/Vref

System Bus
- SpaceWire

Hardware Trigger

Image Sensor

Companion Chip

2014-12-08
Companion Chip for High-End Scientific Image Sensors
This development aims at providing the community with an IR imager companion ASIC

- Single chip solution, tailored to imagers (especially IR sensors)
  - Easy to control
  - Easy to integrate
- Support IR/CMOS/CCD detectors of multiple manufacturers and technologies (HgCdTe, InGaAs, …)
- Able to drive multi-sensor/array systems
- Wide operating temperature range: 77K … 300K
- Radiation hard
  - 1Mrad TID
  - 60MeVcm²/mg SEU / SEL, SET
“Prototype ASIC Development for Large Format NIR/SWIR Detector Array”

To manage image sensor operation:

- Programmable sequencer: 32 programmable outputs, 8 levels of nesting
- Multi-channel pixel data digitization: 4-channel 16-bit ADC @ 100kHz
- ADC for imager health monitoring
- SPI interface for imager configuration
- 8 control outputs, 8 monitor/trigger inputs
- Voltage reference & bias generation (using DAC)
- SpaceWire / RMAP communication interface: 2 … 200 Mbit/s
- System Clock: 0 … 200 MHz
Companion Chip for High-End Scientific Image Sensors
Technology

- Foundry: UMC 180nm (1.8V, 3.3V)
- Digital design by Easics, using DARE library & imec physical design:
  - digital standard cells: gates + FFs + HIT FFs
  - SRAM memories
  - standard I/O cells
  - LVDS I/O cells
- Custom analog design by Caeleste
Prototype ASIC Layout

area = 10mm x 10mm
Programmable Sequencer

**Event** PIXCLK_H: OUT0 = 1
**Event** PIXCLK_L: OUT0 = 0
**Event** SAMPLE: sample input 0 of ADC 1
**Event** ENABLE_ON: OUT1 = 1
**Event** ENABLE_OFF: OUT1 = 0

**Sequence** CLK_PULSE: wait 100 ns; PIXCLK_H; wait 100 ns PIXCLK_L

**Sequence** PULSE_TRAIN: repeat 4 times: CLK_PULSE

**Sequence** READOUT: repeat 2 times: ENABLE_ON; PULSE_TRAIN; wait 100 ns; SAMPLE; wait 100 ns; ENABLE_OFF; wait 100 ns

Sample ADC1. input 0
Radiation Hardening

System Architecture
- Watchdogs, communication redundancy, ...

ASIC Architecture
- Redundancy (parity, hamming, TMR), scrubbing, watchdog, clock gating, frequency scaling

Netlist
- Avoid asynchronous signals, TMR, increased drive strengths, ...

Standard Cell Library
- Radiation hardened cells, e.g. HIT cell, IMEC DARE library

Physical
- Specific Radiation Tolerant processes, e.g. SOI (Silicon on Insulator), Shielding

Increasing Abstraction Level
Design for Low Temperature

- DARE is characterized down to -55°C (218K)
- DARE digital cells @ lower temperature:
  - Gates faster due to higher mobility: Hold time analysis after derating (adapted models)
  - Larger IR-drop due to higher current peaks: power grid!
Design for Low Temperature

• DARE SRAM, LVDS & std. I/O @ lower temp.
  – Backup registers for SRAM

• On-chip characterization structures

• Limited heat dissipation of the chip, to maintain low noise @ cooled imager
Unified design for:
- Room Temperature (RT)
- Cryogenic Temperature (CT) using FMC connector (FPGA Mezzanine Card)

PC controlled using Easics’ hardware TCP/IP core on FPGA
Conclusions

• Prototype ASICs available and demonstrated: Q2 2014
  – tested down to 77K

• Chip area is 1 cm²

• FPGA-based test setup:
  – using FMC plug-in cards for room temp & cryogenic temp testing
  – using Easics’ hardware TCP/IP core to communicate with PC

• Digital DARE demonstrated at cryogenic temp (77K)

• Digital DARE combined with custom analog design
Next Steps towards Flight Models

• Further discussions on the requirements:
  • with instrument builders
  • with image sensor manufacturers

• ASIC design update:
  • digital section
  • analog section

• ADCs:
  • more channels: 32 … 64 (?)
  • faster

• Irradiation testing
Questions?

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