

# **DARE digital flow (Redsat) & DARE MS flow (Cosmic Vision)**

08/12/2014

DARE User Meeting 2014

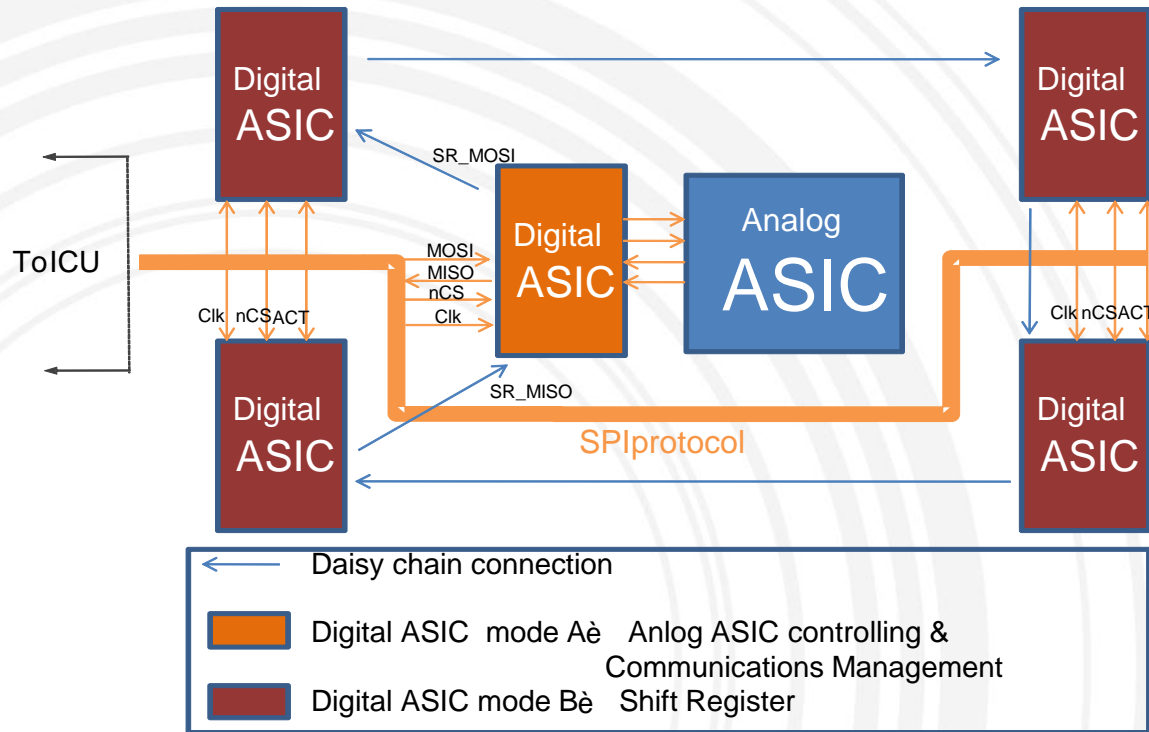
# Outline

- DARE digital flow (Redsat)
  - Chip description
  - Design flow
  - Test and qualification
- DARE Mixed signal flow (Cosmic Vision)
  - Chips description
  - Design flow
  - Cosmic vision status
- Comments and lessons: Designing with DARE

# Redsat – chip description

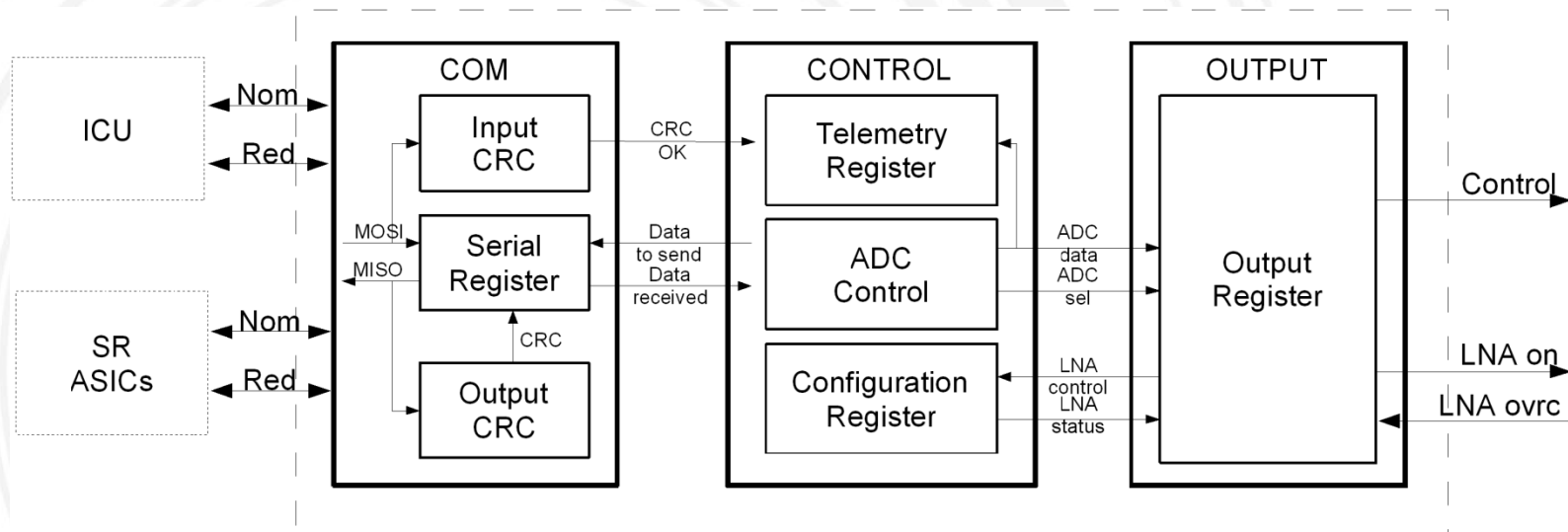
- Arquimea's ARQ-RSB01 chip is a Dual Mode ASIC which can be configured to perform two different functions:
  - Mode A: Control of an antenna chipset
  - Mode B: 24/48 bits shift register (Mode B).
- ARQ-RSB01 has been designed to work together with ARQUIMEA's ARQ-RSA01 or ARQ-RSA02 analogue ASICs mounted in a hybrid. The ARQ-RSB01 is available in a PGA100 package

# Redsat - Application



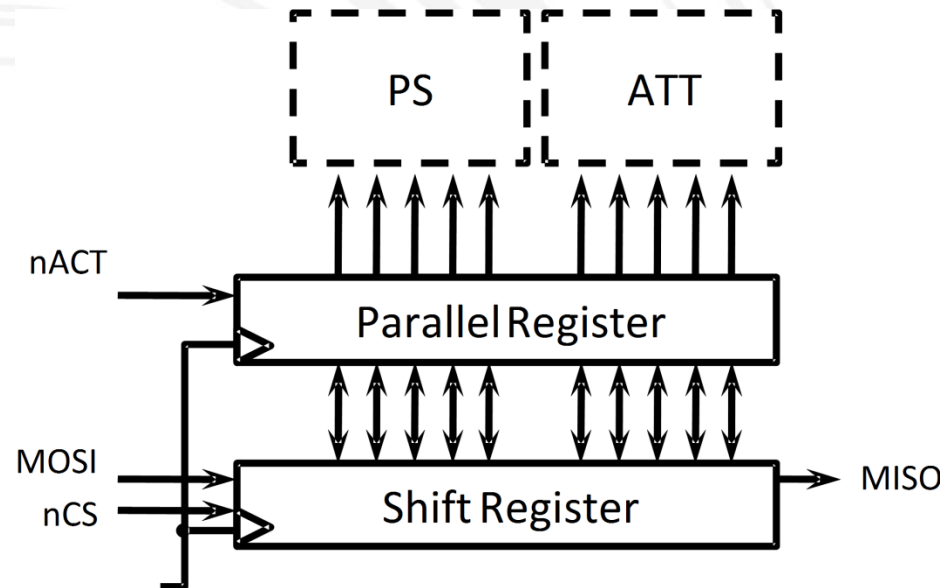
# Redsat – Mode A

- In this mode, the ASIC is responsible for:
  - The communication with an ICU (through SPI).
  - External ADC control and SAR algorithm implementation
  - Miscellaneous input/output registers & Analog ASIC control



# Redsat – Mode B

- In this mode, the ASIC is responsible for:
  - Shift registers used for SPI communication from/to other ARQ-RSB01 chips
  - Parallel registers used to driver parallel data buses



# Redsat – Key specifications

- Dedicated pin for digital purposes. 62
- Successive Approximation Register: 8bits
- Serial-In, Parallel-Out Shift Register: 24/48 bits
- Maximum Operating Frequency: 10 Mhz
- Operating temperature range: [-20;80]<sup>a</sup>C

# Digital flow



System design

Digital Front-end

Netlists & Constraints

Post Layout verification

DARE180 DK

Digital Back-end

sdf & Reports

OK?

reports

Full masks



# Cosmic Vision – chips description

- Under the frame of two ESA projects a set of mixed signal chips have been implemented for the Juice Mission (Cosmic Vision)
- ARQ-CVA-001 is configurable HF (10MHz to 100 MHz) Mixed signal ASIC that contains an LNA, a PA, a Bessel Filter an ADC and a DAC. It is available on a LQFP-120 package
- ARQ-CVB-001 is a configurable MF ADC (100 KHz to 10 MHz). It is available on a CQFP-64 package
- ARQ-CVC-001 is configurable MF (100 KHz to 10 MHz) Mixed signal ASIC that contains an LNA, a PA, a Bessel Filter and a DAC. It is available on a LQFP-120 package

# Cosmic Vision – IPs

- All the IPs developed in the frame of these two contracts are also available for ESA projects.
- The project team includes the following institutions apart from Arquimea: CSIC, UC3M, UPC and USE.

# Cosmic Vision – IPs

IP Name	Main features	Used in
HF DAC	<ul style="list-style-type: none"> <li>• 12 to 9 ENOB from 10 to 50 MHz</li> <li>• 60mA@100MHz</li> </ul>	ARQ-CVA-001
HF ADC	<ul style="list-style-type: none"> <li>• 14 to 12 ENOB from 10 to 100 MSPS</li> <li>• 250mA@100MSPS</li> </ul>	ARQ-CVA-001 SSDP
HF LNA	<ul style="list-style-type: none"> <li>• Adjustable voltage gain from -6dB to +30dB</li> <li>• Adjustable current gain from 3kΩ to 3MΩ</li> <li>• Internal decoupling for AC operation</li> <li>• 50MHz voltage-mode bandwidth</li> <li>• 75mW dissipated power</li> </ul>	ARQ-CVA-001
HF PA	<ul style="list-style-type: none"> <li>• Voltage and current input / output modes</li> <li>• Single-ended and differential output modes</li> <li>• Sinking / sourcing current output selection in current-mode output operation</li> <li>• Adjustable voltage and current common-mode output levels</li> <li>• 2 Vpp output voltage range and 80 mApp output current range</li> <li>• 2 Vpp input voltage range and 400 μApp input current-mode range</li> <li>• 50 Ω load capability in voltage mode</li> <li>• 1.4 V voltage compliance in current mode</li> </ul>	ARQ-CVA-001
HF Bessel Filter	<ul style="list-style-type: none"> <li>• 5 to 50 MHz cut-off, with SNR from 83 dB to 72 dB</li> <li>• 8mW consumption in all frequencies</li> </ul>	ARQ-CVA-001

# Cosmic Vision – IPs

IP Name	Main features	Used in
MF DAC	<ul style="list-style-type: none"> <li>• 100kHz to 1 MHz operation</li> <li>• 16 ENOB</li> <li>• 20 mA</li> </ul>	ARQ-CVC-001
MF ADC	<ul style="list-style-type: none"> <li>• 18 ENOB at 100 KHz, 30 mA</li> <li>• 15 ENOB at 1 MHz, 60 mA</li> <li>• 14 ENOB at 5 MHz, 70 mA</li> <li>• 13 ENOB at 10 MHz, 200 mA</li> </ul>	ARQ-CVB-001
MF LNA	<ul style="list-style-type: none"> <li>• Adjustable voltage gain from -6dB to +30dB</li> <li>• Adjustable current gain from 3k<math>\Omega</math> to 3M <math>\Omega</math></li> <li>• Up to 4Vpp input diff. Voltage with more than 5MHz BW</li> <li>• 80mW dissipated power</li> </ul>	ARQ-CVC-001
MF PA	<ul style="list-style-type: none"> <li>• Voltage and current input/output modes</li> <li>• Single-ended and differential output modes</li> <li>• 4 Vpp output voltage range and 80mApp output current range</li> <li>• 2Vpp input voltage range and 400 <math>\mu</math>App input current range</li> </ul>	ARQ-CVC-001

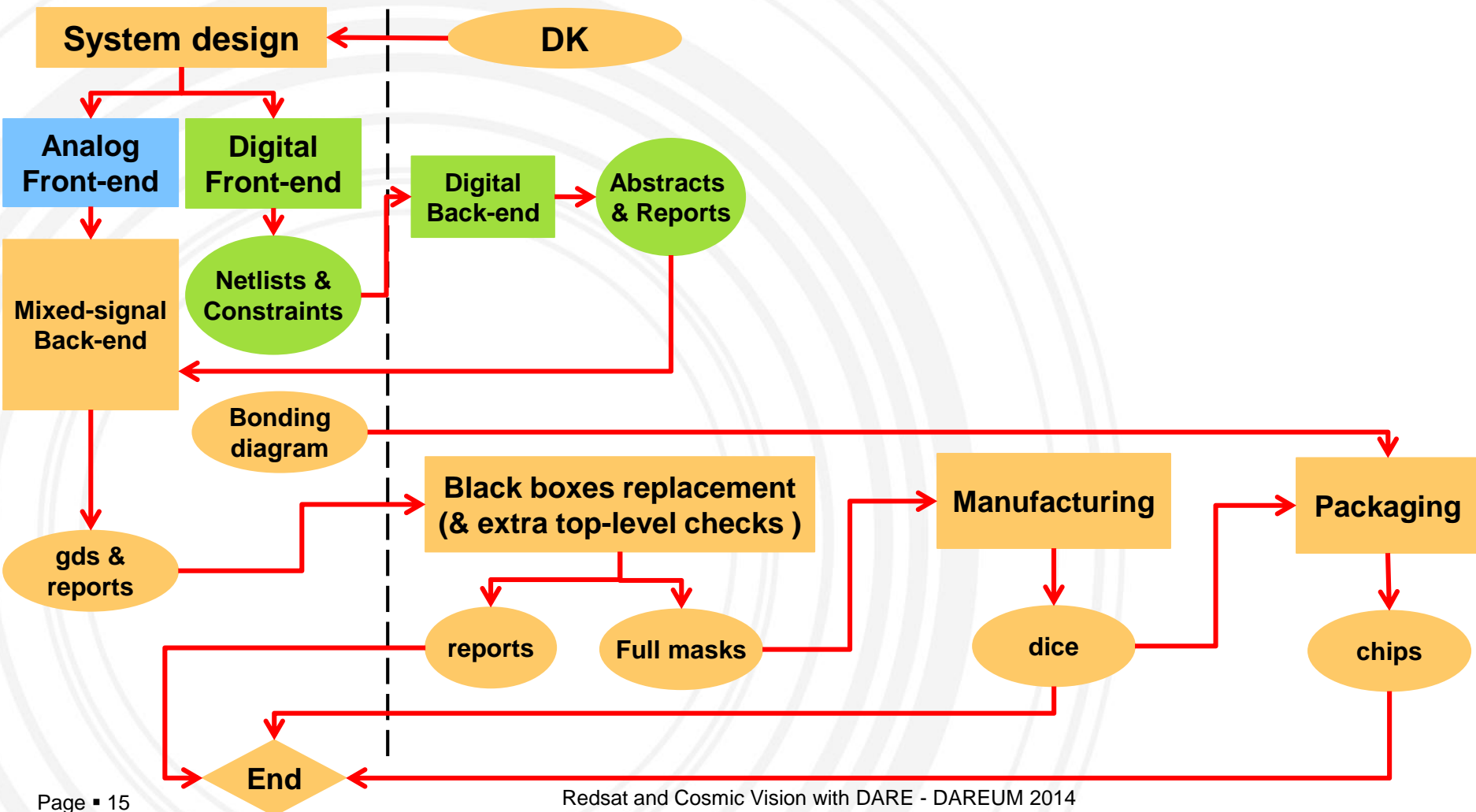
# Cosmic Vision – IPs

IP Name	Main features	Used in
MF Bessel Filter	<ul style="list-style-type: none"> <li>• 5MHz cut-off, 9mW and SNR 70 dB</li> <li>• 1MHz cut-off, 5mW and SNR 70 dB</li> </ul>	ARQ-CVC-001
SPI to bits	SPI slave up to 100 MHz	ARQ-CVA-001 ARQ-CVB-001 ARQ-CVC-001
3.3V to 1.8V Regulator	<ul style="list-style-type: none"> <li>• From 1 to 60 mA output current</li> <li>• <math>\pm 2\%</math> output voltage accuracy</li> </ul>	ARQ-CVA-001 ARQ-CVB-001 ARQ-CVC-001
3.3V to 1.8V Regulator for digital circuitry	<ul style="list-style-type: none"> <li>• High response to current peaks</li> <li>• From 1 to 60 mA output current</li> <li>• <math>\pm 2\%</math> output voltage accuracy</li> </ul>	ARQ-CVA-001 ARQ-CVB-001 ARQ-CVC-001
Bandgap 1 <sup>st</sup> order	<ul style="list-style-type: none"> <li>• 1.25V reference with 10mV variation from [-10; 85] °C</li> </ul>	ARQ-CVA-001

# Cosmic Vision – IPs

IP Name	Main features	Used in
Bandgap 2 <sup>nd</sup> order	<ul style="list-style-type: none"><li>• 1.25V reference with 3.6mV variation from [-10; 85] °C</li></ul>	ARQ-CVB-001 ARQ-CVC-001
POR	<ul style="list-style-type: none"><li>• Power-on-reset with brown-out.</li><li>• Warrantied 130 µs duration reset</li></ul>	ARQ-CVA-001 ARQ-CVB-001 ARQ-CVC-001

# Cosmic Vision mixed-signal flow



## Comments and lessons: Interfacing

- Two different interfaces: Design services and Foundry services => Quotations, POs and communication with different teams.
- Design services: Digital Backend and top level LVS (own quotations, PO and interface)
- Foundry services: MPW run and packaging (own quotations, PO and interface)
- Final go for fabrication to both teams? Still a bit unclear.



## Comments and lessons: Design Registration

- Run by MPW team?
- Not sure about what fields are mandatory and what fields are not.
- Design purpose: What should be stated for ESA funded projects? The closest option for a design led by a company is “Industrial Project Development”
- Not all options are available through this system. For instance if you want to order an additional wafer and package more dies than the ones available in a single wafer you are not allowed to introduce it through the web service. This generates confusion since you have to state different quantities here and in a separated PO. The same happens with special packages, etc.

## Comments and lessons: Designing with DARE

- IMEC design support staff is friendly, cooperative, proactive, resolute and hard-worker.
- ‘More than recommended’ tools to be used (IC6 and calibre)
- No spectre views available for digital cells (for low gate count designs). Purely analogue simulations are not possible out of IMEC.
- Supply rings in IO cells need to be virtually connected with labels.
- Black boxes in digital and IO cells could mask layout errors (nets stamping conflicts and DRC errors). This requires additional work and feedback between ARQ-IMEC

## Comments and lessons: Designing with DARE

- Radiation rules run at IMEC not accessible before hand (only report)
- Additional DRC rules run at IMEC not accessible before hand (only report)
- DARE library has been updated during the Cosmic Vision development. This implies that some digital layouts are available in version 4.3 and the rest in 5.5.
- If blocks with different version of the DARE library have to be integrated in the same chip, additional work and configuration control is required at IMEC for cell replacement. Have to take this into account when implementing design!
- Some cells area is different from version 4.3 to 5.5

## Comments and lessons: Designing with DARE

- With IP-reuse and if further changes are made to the library this will have an impact on the backend activities.
- A guide with recommendations on the Mixed signal flow with DARE will be very nice to have.

- Thank You for your attention!
- Come and talk to us in the poster session





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# ARQUIMEA

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Passion for Technology