

A mix-signal radhard micro-controller : the DPC

Noordwijk ESTEC,
Dec 8th, 2014



DARE User Forum

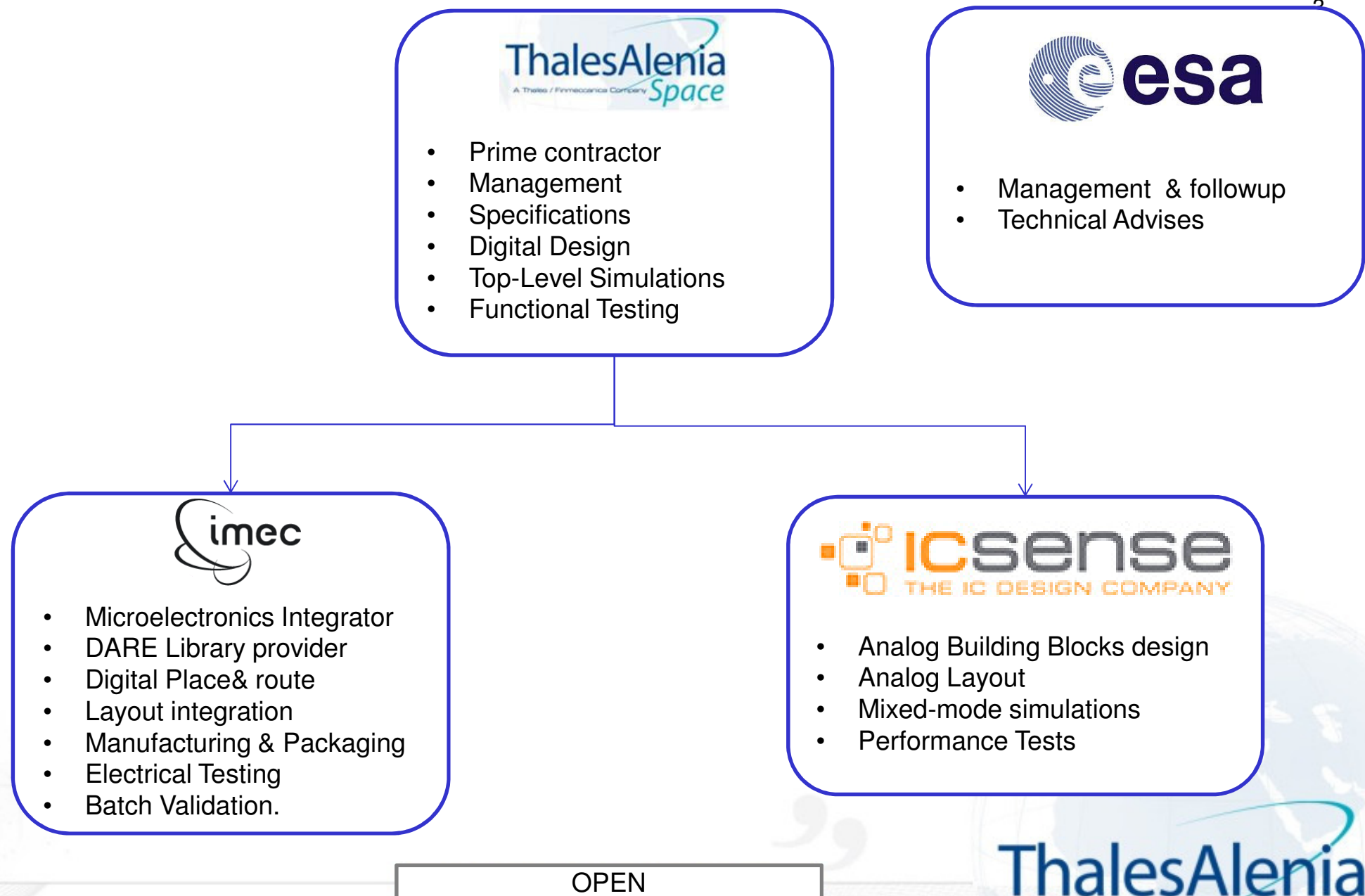


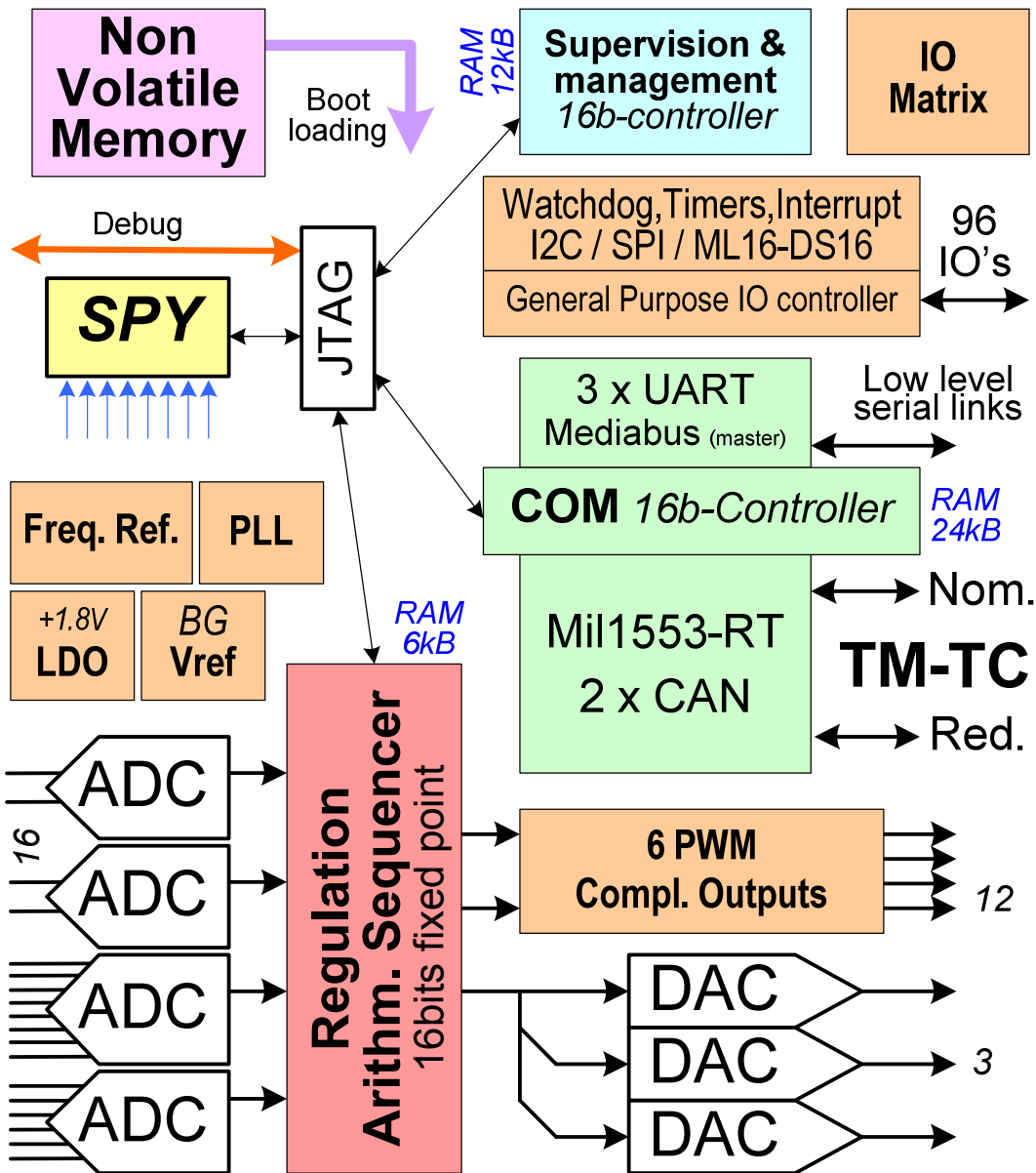
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- Organization
- Architecture
- Emulation
- DARE library
- Analog functions
- Die view
- Conclusions

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Organization





On chip :

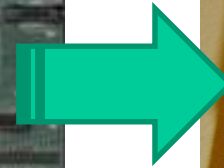
- 16bits OpenMSP430 CPU
- 42K memory
- RC oscillator + 120MHz PLL
- LDO +1.8V
- Bandgap
- 13bits ADC + input MUX
- 12 Bits DAC

Off Chip:

- E2prom
- +3.3V regulator

DARE on UMC 0,18μ
CQFP 256 pins

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Core Validation BreadBoard

- All Functional modes
- Digital Interfaces
- SW development suite
- Debug & Spy fonctionnalités

Designer Starter Kit

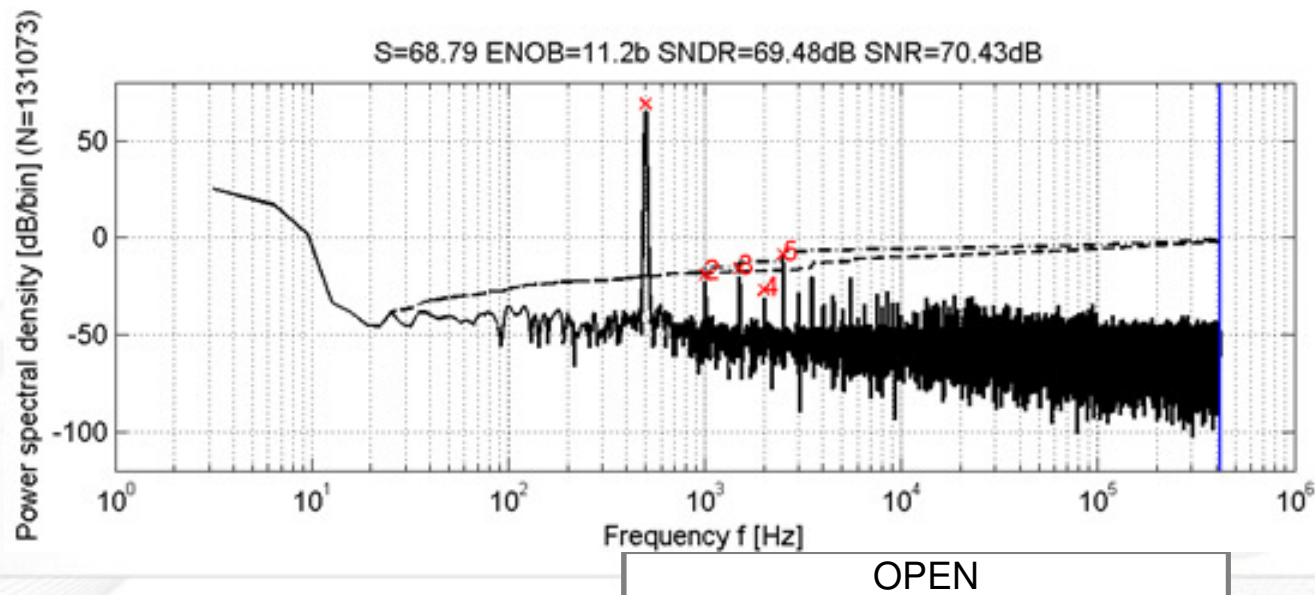
- Early integration into equipments
- Analog Interfaces
- Application SW

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- Selected library DARE on UMC 180nm
- DARE+ library enhancements
 - Clock gating cells
 - SET optimized clock and set/reset trees
 - Dual Port SRAM
 - Slew rate controlled IO
- Advanced Characterization tool (Altos)
- Analog Design kit

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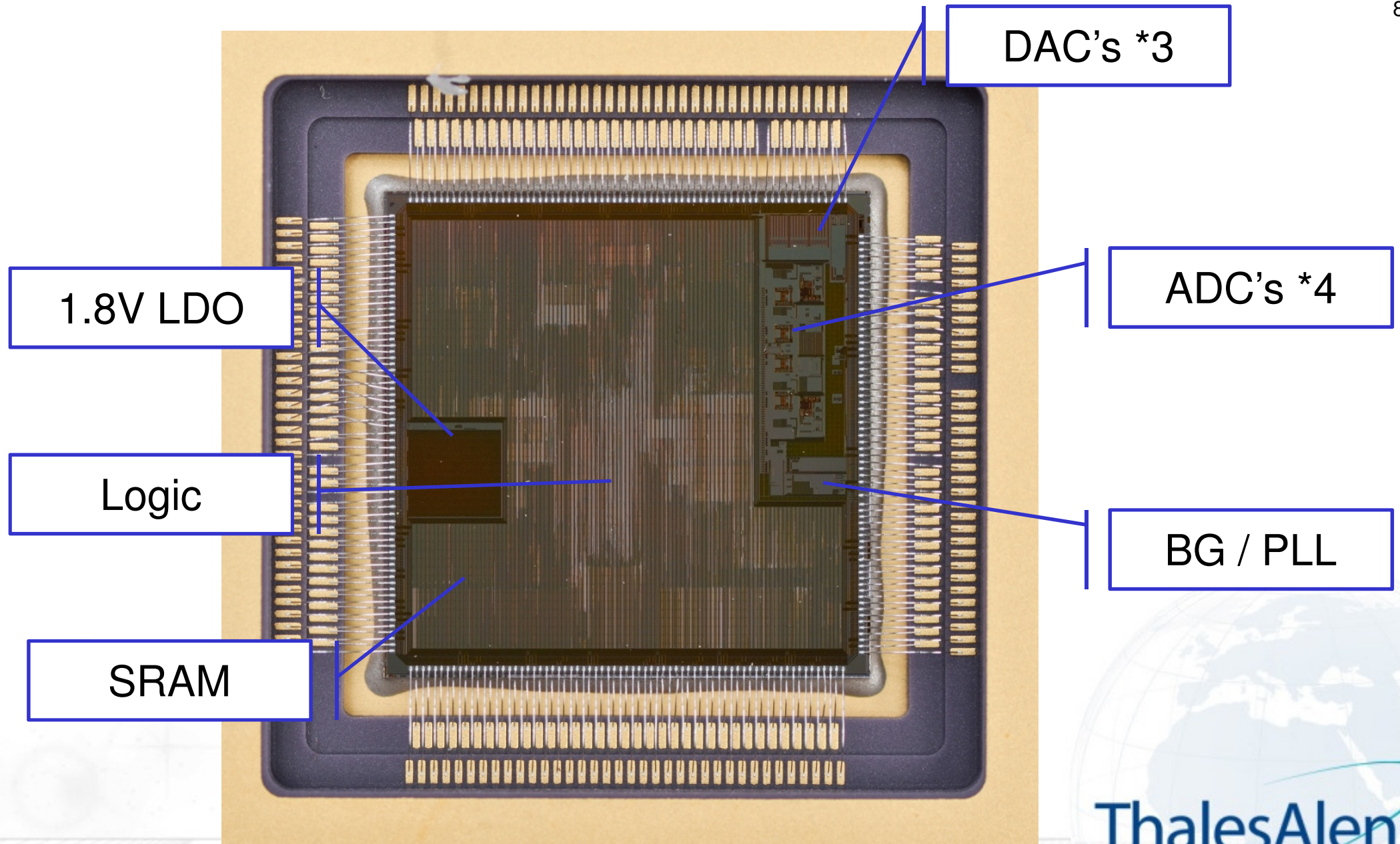
- 1V Bandgap Reference voltage and current generation
- Power-management block with LDO's
- 120 MHz frequency reference system (PLL) to provide the clock to the digital part
- 100kHz reference oscillator
- 4 flexible 13 bit , 1MSps ADCs with extensive input muxing capabilities
- 3 12 bit, 3.75 MSps DAC current-mode outputs
- Power-on-reset circuit and under voltage detector
- Rail to rail comparators, PGA (0dB, 10dB, 20dB)

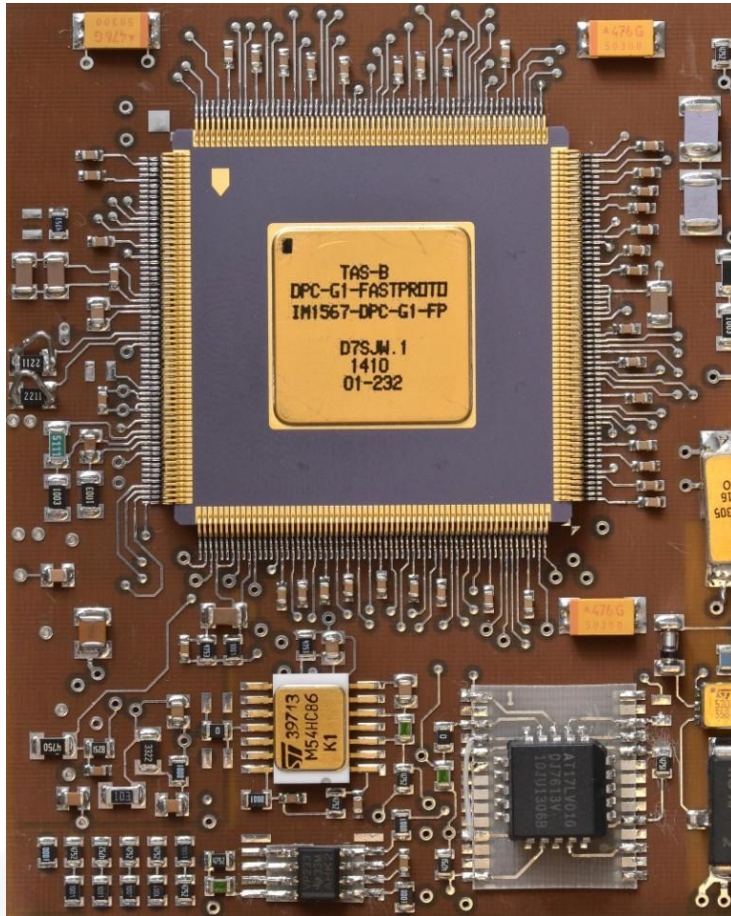


60MeV.cm²/mg



SET check :
Systematic 1.2pC





Generic & Versatile

- * Programmable
- * Configurable

Mixed mode / all analog functions on chip

Rad hard & European

Feature list OK 😊

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