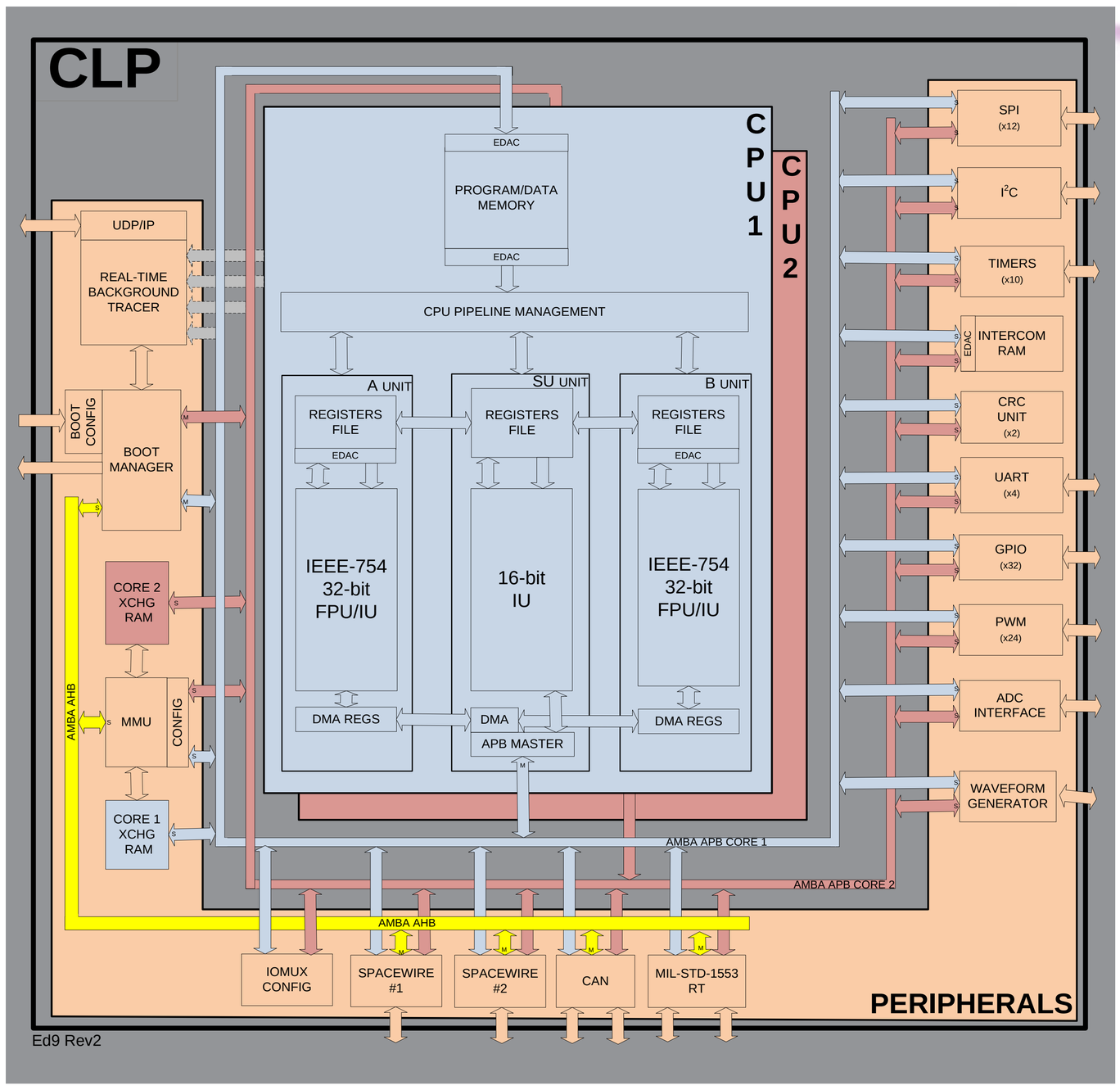
imecDARE User Meeting 2014

CLP – CONTROL LOOP PROCESOR

Features

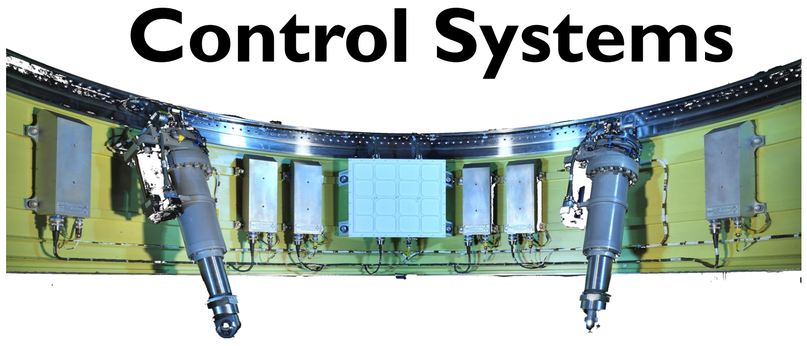
- ***Tailored to hard real-time control loops***
  - ❑ **Deterministic OS-free RISC architecture**
  - ❑ **Dual core High-Performance SIMD**
  - ❑ **Vectorial 32-bit IEEE-754 operations**
  - ❑ **Fast on-chip data memories**
  - ❑ **DMA capability**
- ***Wide range of Interfaces***
  - ❑ **Sensors, power drive and OBC bus links**
  - ❑ **Programmable APB resources allocation**
- ***Standard SDE***
  - ❑ **LLVM based**
  - ❑ **Matlab/Simulink and/or C code generation**
  - ❑ **Debugger, cycle-accurate simulator, UTM**
  - ❑ **Real-time non-intrusive SW tracing**
- ***200 MFLOPS/100 MIPS targeted***
- ***ITAR-free SW programmable ASSP***



DARE usage

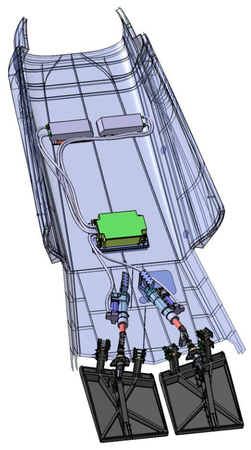
- *UMC 180 nm,3.3V*
- *HIT cells*
- *Two 8192x39 DPRAM for Program Memories*
- *Two 512x39 DPRAM for Data Memories*
- *1 PLL*
- *Massive Clock gating*
- *CQFP-256*
- *ESCC9000 qualification*

Thrust Vector Control Systems



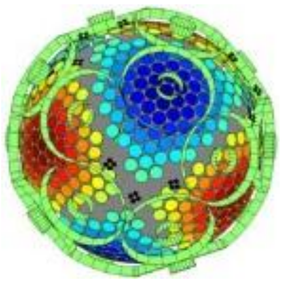
VEGA C/E, Ariane 6

Flap Control Systems



PRIDE

New AOCS Generation



ELSA

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