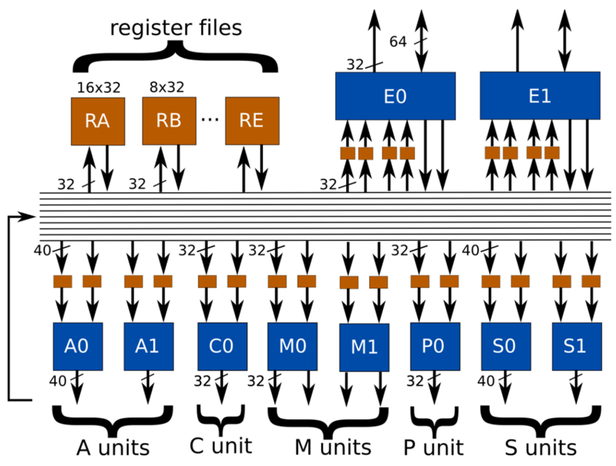
imecDARE User Meeting 2014

XENTIUM DSP IP CORE

Xentium IP: programmable high-performance DSP core



Xentium VLIW DSP IP

Architecture

- VLIW with 10 parallel execution units
- 32/40-bit fixed-point data path
- 16-bit SIMD

Efficient complex MAC execution

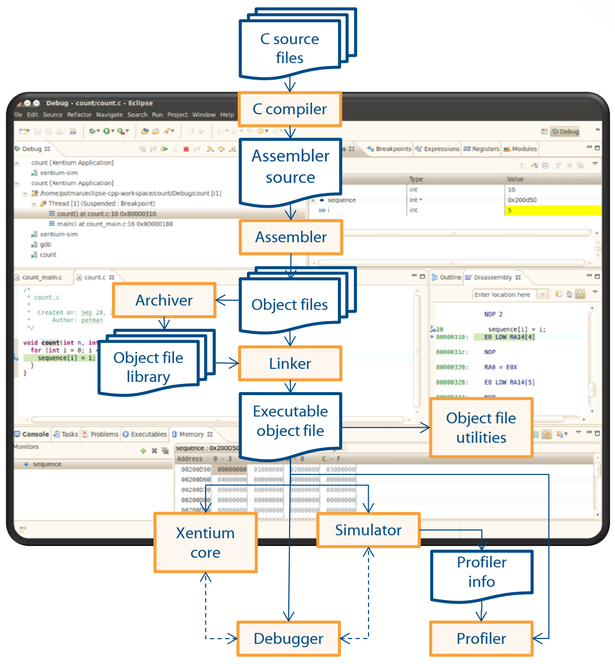
- 2 16-bit complex MACs/cycle

Development Tooling

- Eclipse C Development Tooling (CDT)

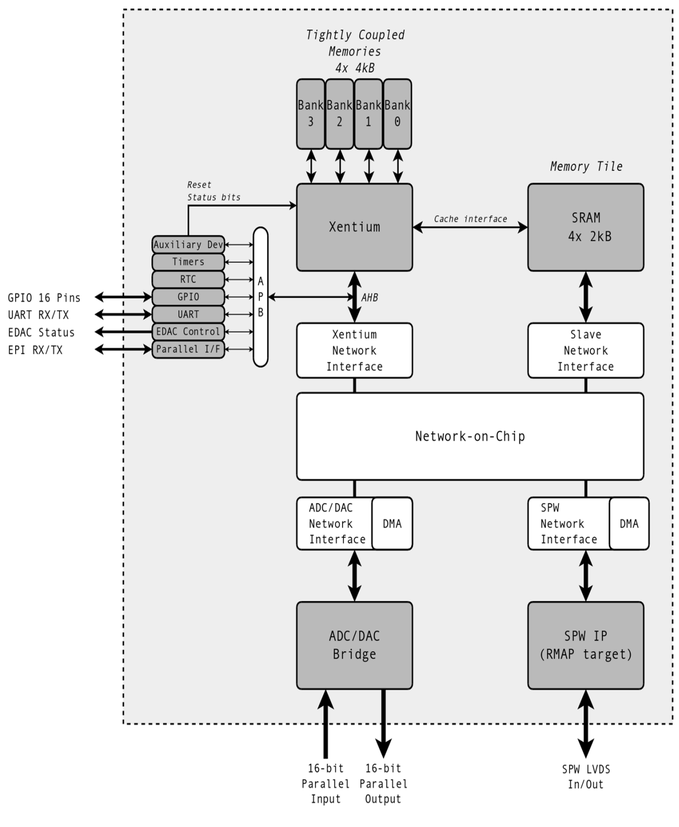
Performance benchmarks

FFT-256, radix-4	958 cycles
FFT-1024, radix-4	4680 cycles
32-tap complex FIR filter (256 samples)	4113 cycles



Eclipse C Development Tooling

Rad-hard XentiumDARE ASIC implementation and test



IP test ASIC prototype

Radiation Hardening

- DARE 180nm CMOS technology
- EDAC protected SRAMs

ASIC Prototype

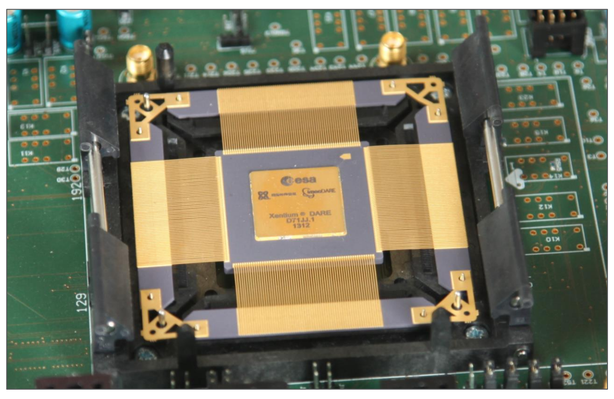
- Die area: 5x10 mm^2
- External clocks: 100MHz; 200MHz
- 1.8V Core, 3.3V IO
- CQFP 256-pin package Kyocera full-custom

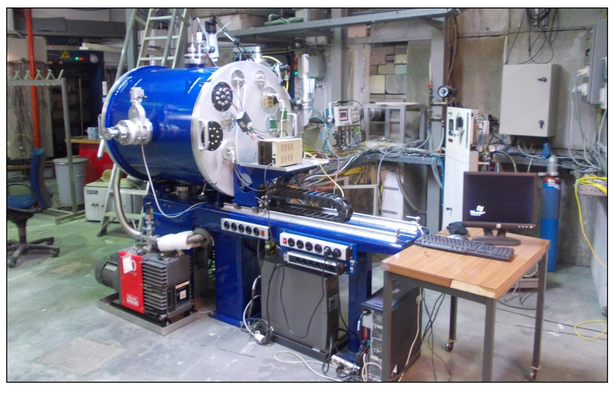
XentiumDARE SoC Architecture

- Xentium DSP IP core
- Network-on-Chip IP
- SpW-RMAP and ADC/DAC
- Small memory tile
- Watchdog

Irradiation Testing

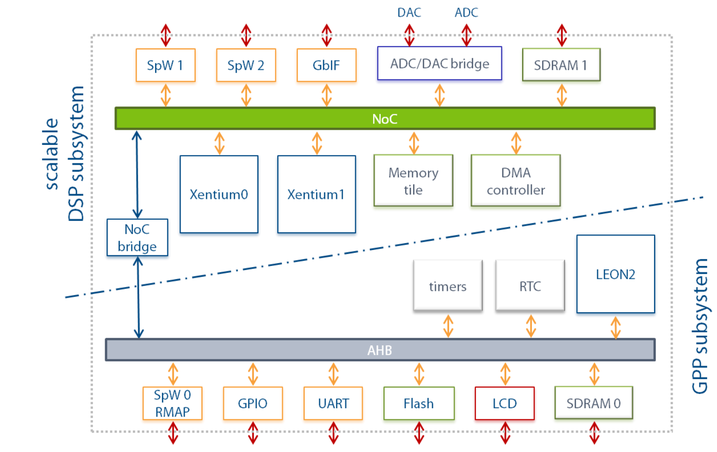
- SEE – SEU / SEL





ASIC implementation and test

Application example: heterogeneous multi-core architecture



Network-on-Chip (NoC) based Xentium DSP multicore architecture

Architecture

- 2 Xentium DSP core
- 1 Leon Core
- SpaceWire interfaces
- ADC/DAC interfaces
- Distributed memory

Network-on-Chip

- Packet-switched X-Y routing
- Memory mapped communication protocol

FPGA-based prototype

Scalable Sensor Data Processor

esa

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