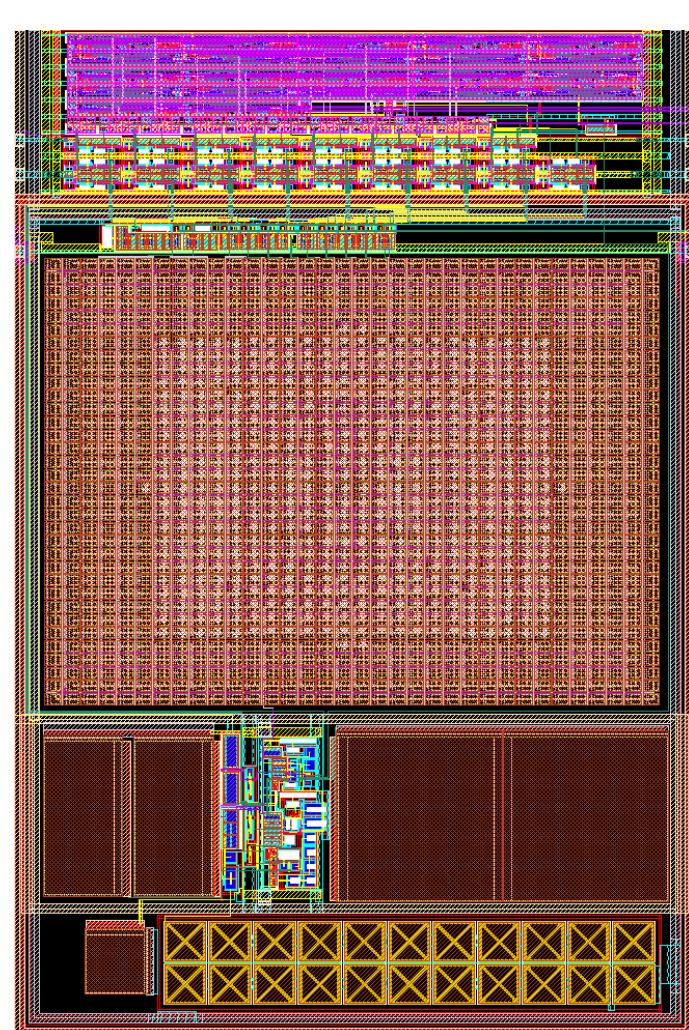


## IMEC DARE RAD HARD IP

In the course of several ESA projects several IP blocks have been designed and are available for use in other projects. Currently most of the IP is tested or qualified for flight model on the DARE180U (UMC 0.18 $\mu$ m) platform.

A selection of available IP is discussed here. For more in-depth information about usage, data sheets or porting IP to other technology node send a mail to [dare\\_support@imec.be](mailto:dare_support@imec.be)

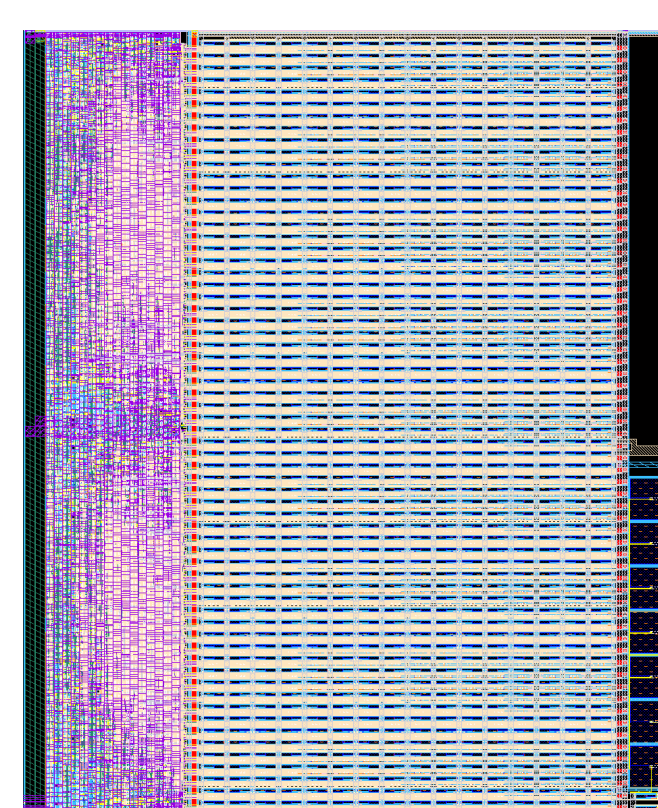
### ADC



Specification	Range
Resolution	10 bit
DNL	< 1 LSB
INL	< 1 LSB
Temperature Range	-55 °C .. +125 °C
Analog Supply Voltage	VDDA = 3.3V +/- 10%
Temperature Drift	< 1 LSB
Input Voltage Range	0 < Vin < VFS
Full Scale Voltage	1.4 < VFS < VDDA
Conversion Speed	< 1 ms
Total Dose	100 krad (Si)

On Flight Model

### DAC



Specification	Range
Resolution	10 bit
DNL	< 1 LSB
INL	< 1 LSB
Temperature Range	-55 °C .. +125 °C
Analog Supply Voltage	VDDA = 3.3V +/- 10%
I <sub>LSB</sub> low current range	1 $\mu$ A .. 6 $\mu$ A
I <sub>LSB</sub> high current range	5 $\mu$ A .. 30 $\mu$ A
Total Dose	100 krad (Si)

On Flight Model

## SRAM Blocks and Compiler

### DARE180U

#### Single port compiler

Parameter	Minimum	Typical	Maximum	Unit
Junction Temperature	-55	27	145	°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	bits
Word Count	32	-	8192	words
Word Length	8	-	256	bits
Write Mask Granularity	8	-	-	bits
Operating Frequency	-	-	200	MHz
SRAM Cell Cross-section	NA	33x10 <sup>9</sup>	NA	cm <sup>2</sup>

#### Dual port compiler

Parameter	Minimum	Typical	Maximum	Unit
Junction Temperature	-55	27	145	°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	Bits
Word Count	32	-	8192	Word
Word Length	8	-	256	Bits
Write Mask Granularity	8	-	-	Bits
Operating Frequency	-	-	TBD	MHz
SRAM Cell Cross-section	NA	120x10 <sup>9</sup>	NA	cm <sup>2</sup>

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### DARE180X

- Five dual port instances were implemented in XFAB XH018
- High-density SRAM with Non-ELT SRAM cell
- No compiler yet

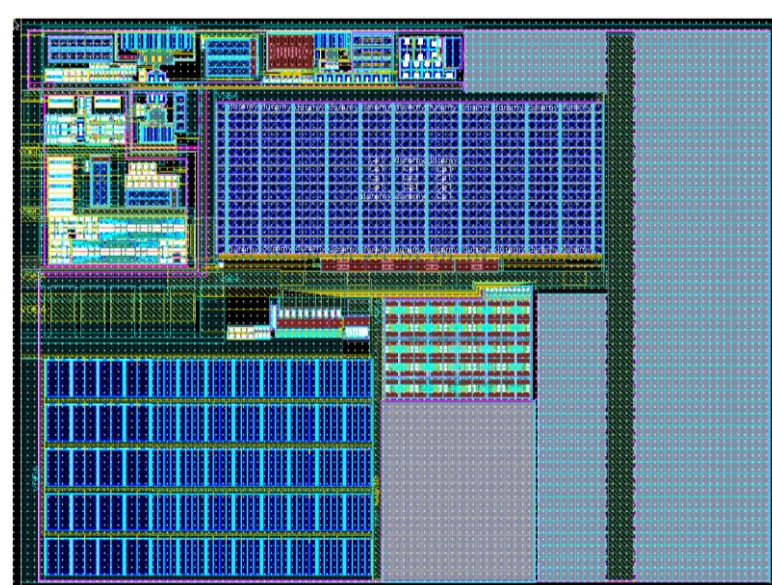
Layout Ready

### CERN 65nm

- Pseudo dual port SRAM compiler
- Power consumption 32kbit SRAM <24 $\mu$ W/MHz
- Max. frequency 80 MHz
- Total Dose >200 Mrad (Si)
- LET thresh. >15 MeVcm<sup>2</sup>/mg

Testchip Taped Out

### PLL

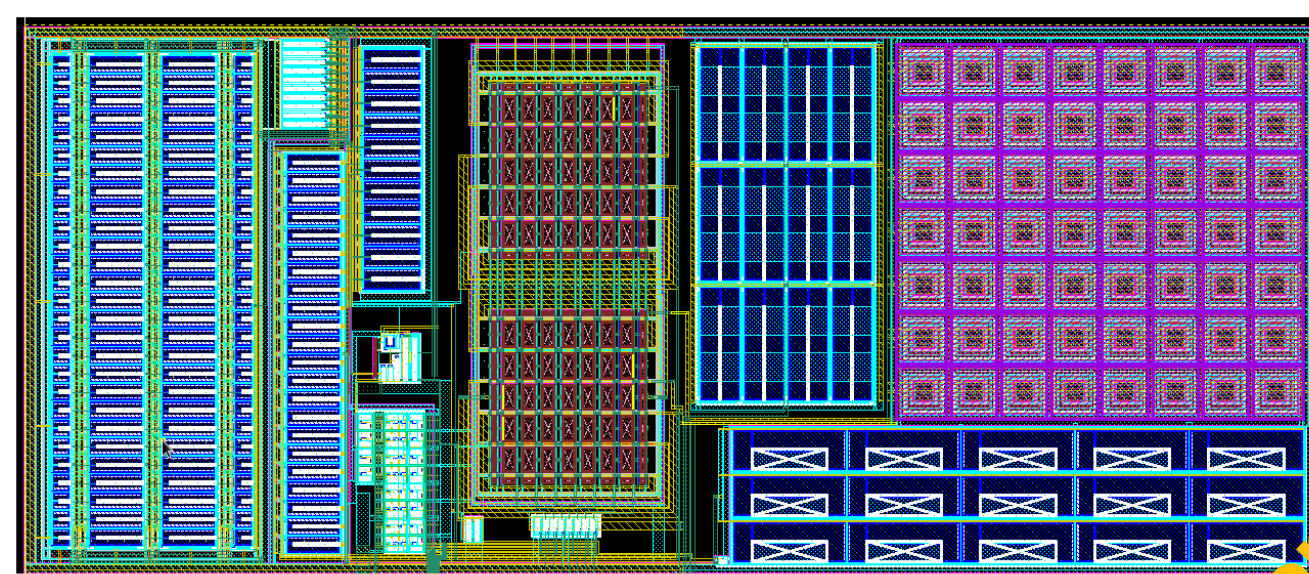


Parameter	Description	Minimum	Typical	Maximum	Unit
T	Junction temperature	-55	-	145	°C
V <sub>DD</sub>	Supply voltage	1.62	1.8	1.98	V
I <sub>VDDA</sub>	Analog supply current (f <sub>vco</sub> = 400MHz)	-	7	8	mA
I <sub>VDD0</sub>	Digital supply current	-	2	5	mA
f <sub>IN</sub>	Input frequency	10	-	50	MHz
f <sub>vco</sub>	Output frequency <sup>2</sup> (f <sub>vco</sub> )	160	-	400	MHz
f <sub>vco_div2</sub>	Output frequency <sup>2</sup> (f <sub>vco_div2</sub> )	80	-	200	MHz
f <sub>vco_div4</sub>	Output frequency <sup>2</sup> (f <sub>vco_div4</sub> )	40	-	100	MHz
f <sub>vco_div8</sub>	Output frequency <sup>2</sup> (f <sub>vco_div8</sub> )	20	-	50	MHz
f <sub>vco_div16</sub>	Output frequency <sup>2</sup> (f <sub>vco_div16</sub> )	10	-	25	MHz
D <sub>vco_div*</sub>	Duty cycle (all f <sub>vco_div*</sub> outputs)	46	-	54	%
D <sub>vco</sub>	Duty cycle (f <sub>vco</sub> output)	30	-	70	%
D <sub>refin</sub>	Duty cycle (f <sub>refin</sub> output)	40	-	60	%
J <sub>CC</sub>	Cycle to cycle jitter	-100	-	100	ps
J <sub>LT</sub>	Long term jitter	-200	-	200	ps
t <sub>lock</sub>	Lock time	-	20	30	$\mu$ s
C <sub>vco*</sub>	Output load (f <sub>vco*</sub> outputs)	-	-	3	pF
C <sub>feed</sub>	Output load (f <sub>feed</sub> output)	-	-	0.1	pF

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### Bandgap

- 1.2V voltage reference on 3.3V supply



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### Others

- Linear Voltage Regulator 50mA; 3.3V to 1.8V
- Ring Oscillator for speed monitoring
- Crystal oscillator (design stage)