ASPIRE
INVENT
ACHIEVE

imec

IMEC IC-LINK ESCC COMPLIANT ASIC MANUFACTURING AND QUALIFICATION SERVICES

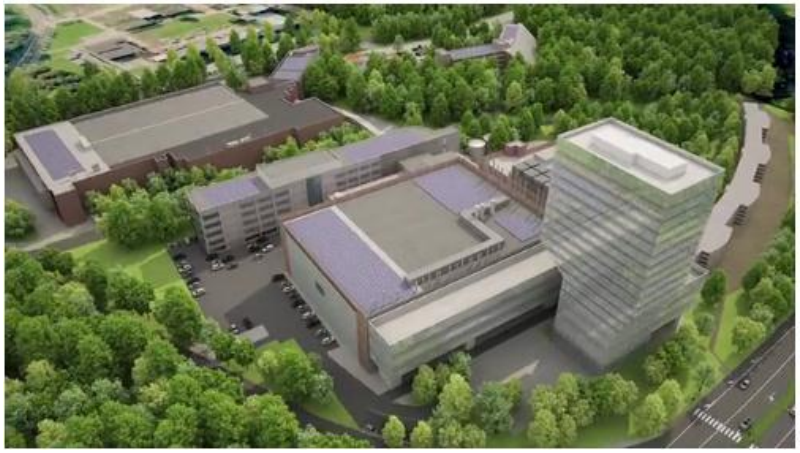
TOM RAMAN
Tom.Raman@imec.be

TOPICS

- Imec, more than DARE
- ASIC Supply Chain Flow
- Test Success stories
- Conclusions

IMEC, MORE THAN DARE

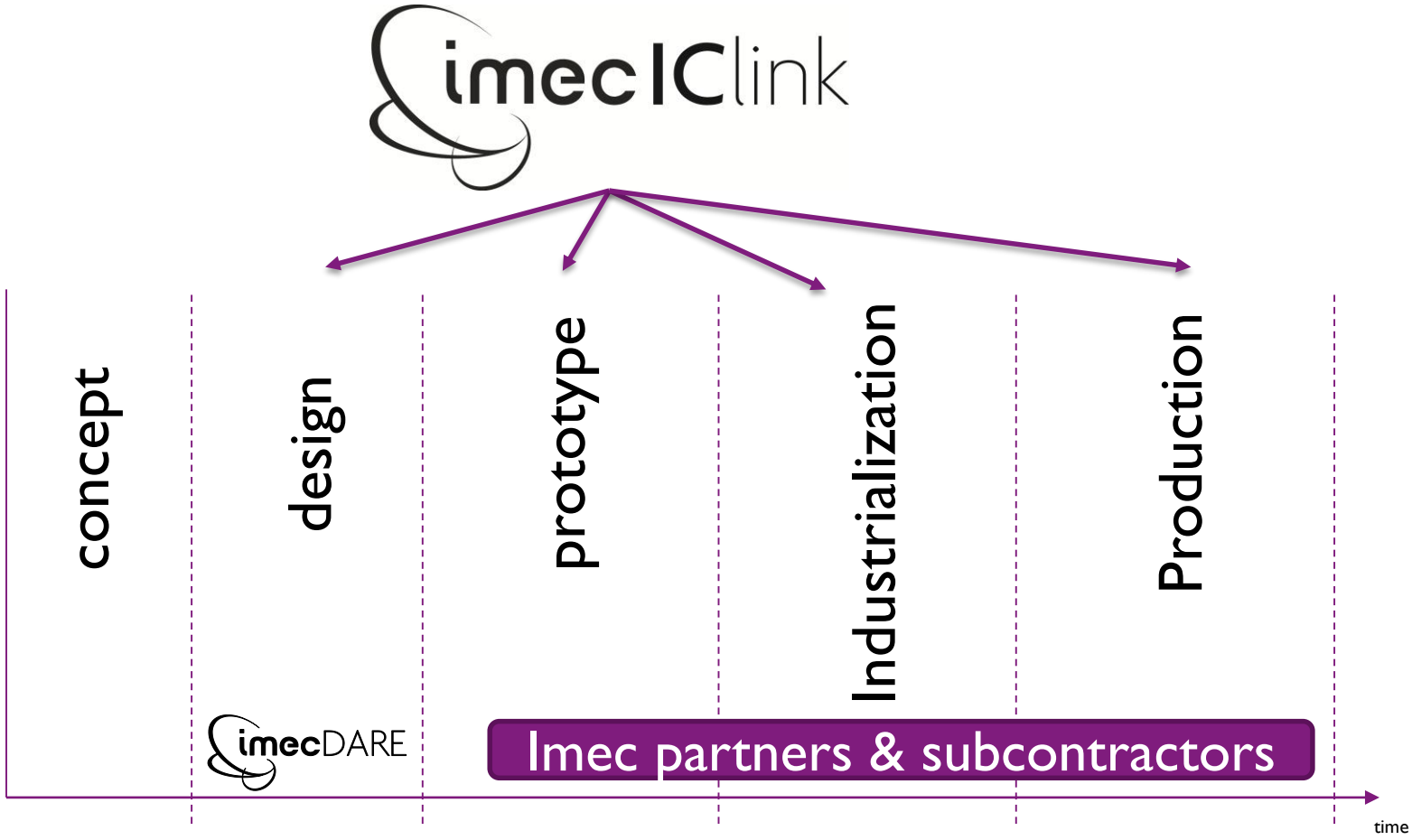
- Imec, more than the DARE library
- Imec is the one of the largest independent research institutes worldwide



- The industrial arm of imec is branded imec IC-link
  - Vision: to be an important actor in the delivery of Aerospace silicon solutions to the European space industry

IMEC, MORE THAN DARE

IMEC, MORE THAN DARE



Typical product development cycle

IMEC, MORE THAN DARE

Imec IC-link offers besides the DARE library; the following services

- Wafer production
- Assembly according to chart F2, ESCC 9000
- Test development
- Screening according to chart F3, ESCC 9000
- Qualification according to chart F4, ESCC 9000
- Failure analysis
- Access to the imec IC-link network

IMEC IC-LINK NETWORK

TOPICS

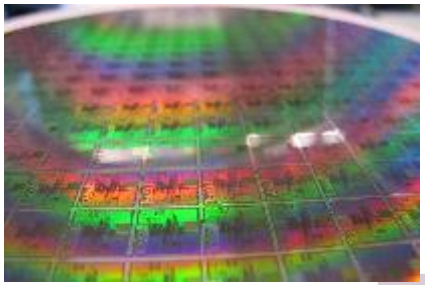
Imec, more than DARE

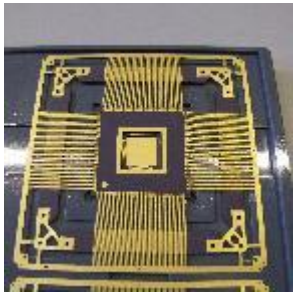
ASIC Supply Chain Flow

Test Success stories

Conclusions

ASIC SUPPLY CHAIN FLOW





Wafer foundry
- Dedicated mask-set
- MPW

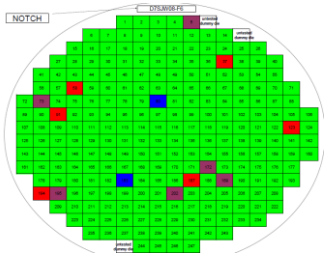
Test house
- Wafer level test
- Wafer map generation

Assembly
- Package design
- According to chart F2
- Trace-ability with respect to wafer map
- SEM inspection

Final Test
- Test on packaged components
- Test over temperatures

Screening and Qualification
- Screening acc to chart F3
- Qualification acc to chart F4
- Radiation test

Delivery to customer



ASIC SUPPLY CHAIN FLOW – WAFER FOUNDRY

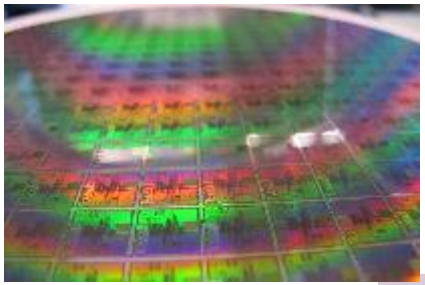
Multi Project Wafer: Prototyping service

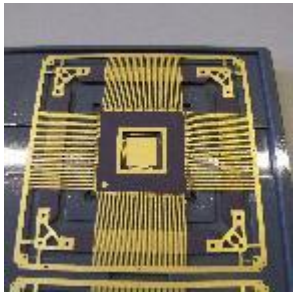
- Prove the ASIC functionality
- Limited number of packaged samples (typical 40 pieces)
- Low cost

Flight Module production only with dedicated mask-set

- Dedicated mask-set
- Engineering run of 12 or 24 wafers
  - Possibility to put wafers on hold for later mask-updates
- High NRE cost

ASIC SUPPLY CHAIN FLOW





Wafer foundry
- Dedicated mask-set
- MPW

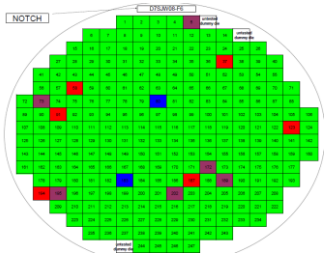
Test house
- Wafer level test
- Wafer map generation

Assembly
- Package design
- According to chart F2
- Trace-ability with respect to wafer map
- SEM inspection

Final Test
- Test on packaged components
- Test over temperatures

Screening and Qualification
- Screening acc to chart F3
- Qualification acc to chart F4
- Radiation test

Delivery to customer



WAFER PROBING

Purpose

- Remove bad dies in early manufacturing stage
  - Advantage → Save packaging cost
  - Failure due to functionality (electrical) or processing

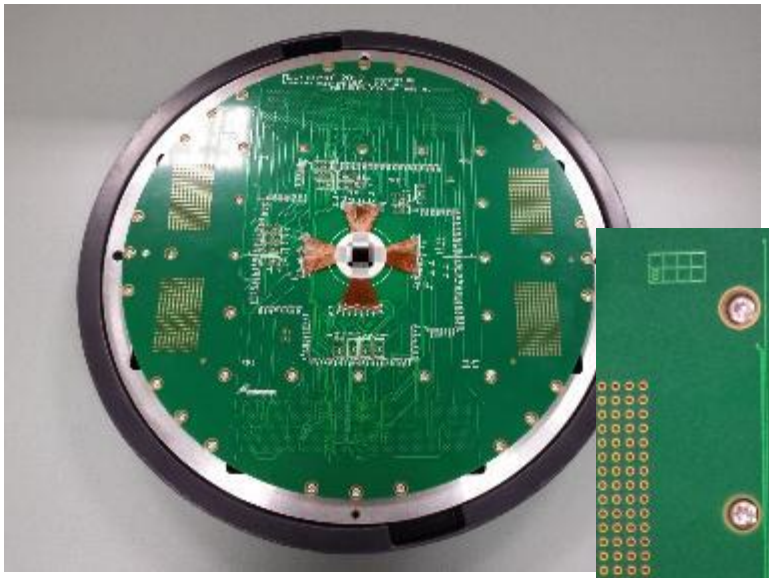
Resources

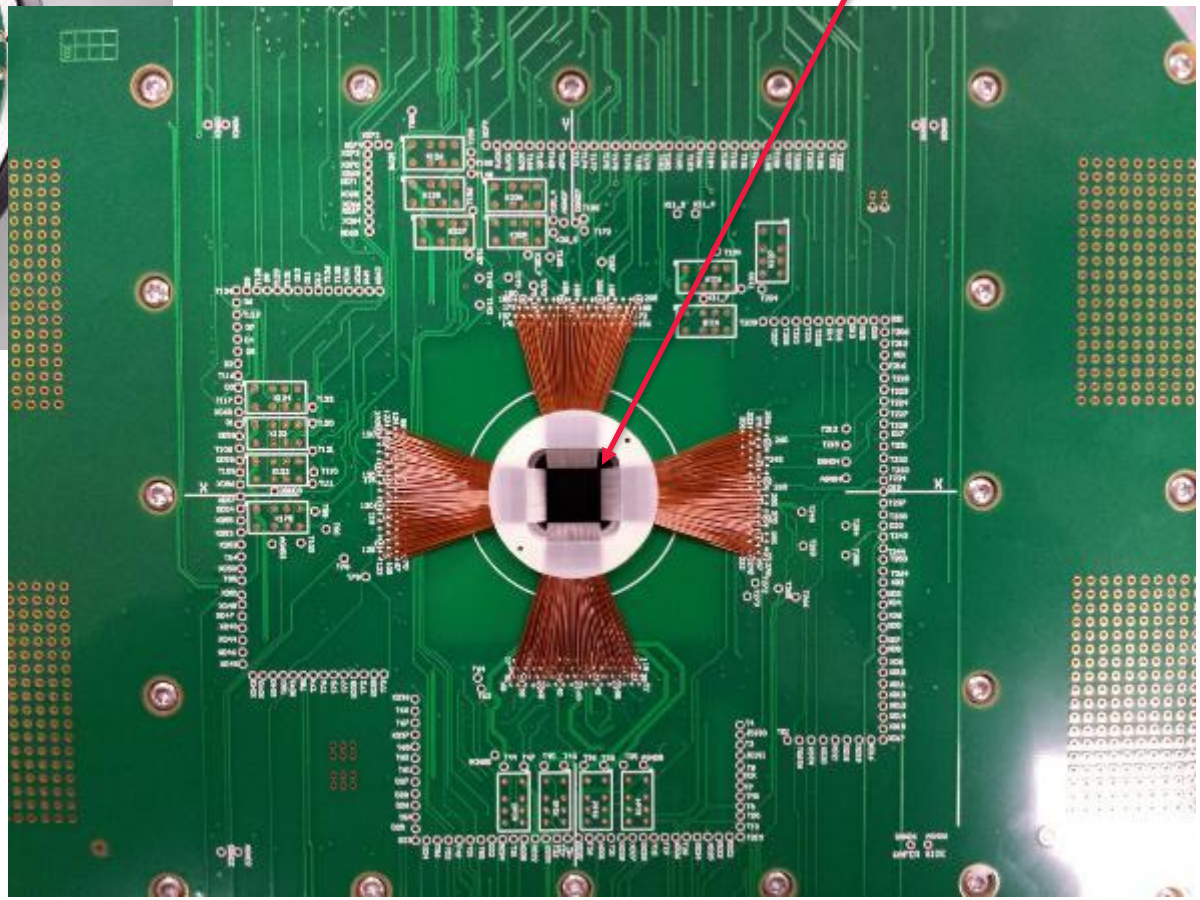
- Tester & test program
- Probe card
- Wafer prober (8” & 12” wafer probing capabilities)

Test flow

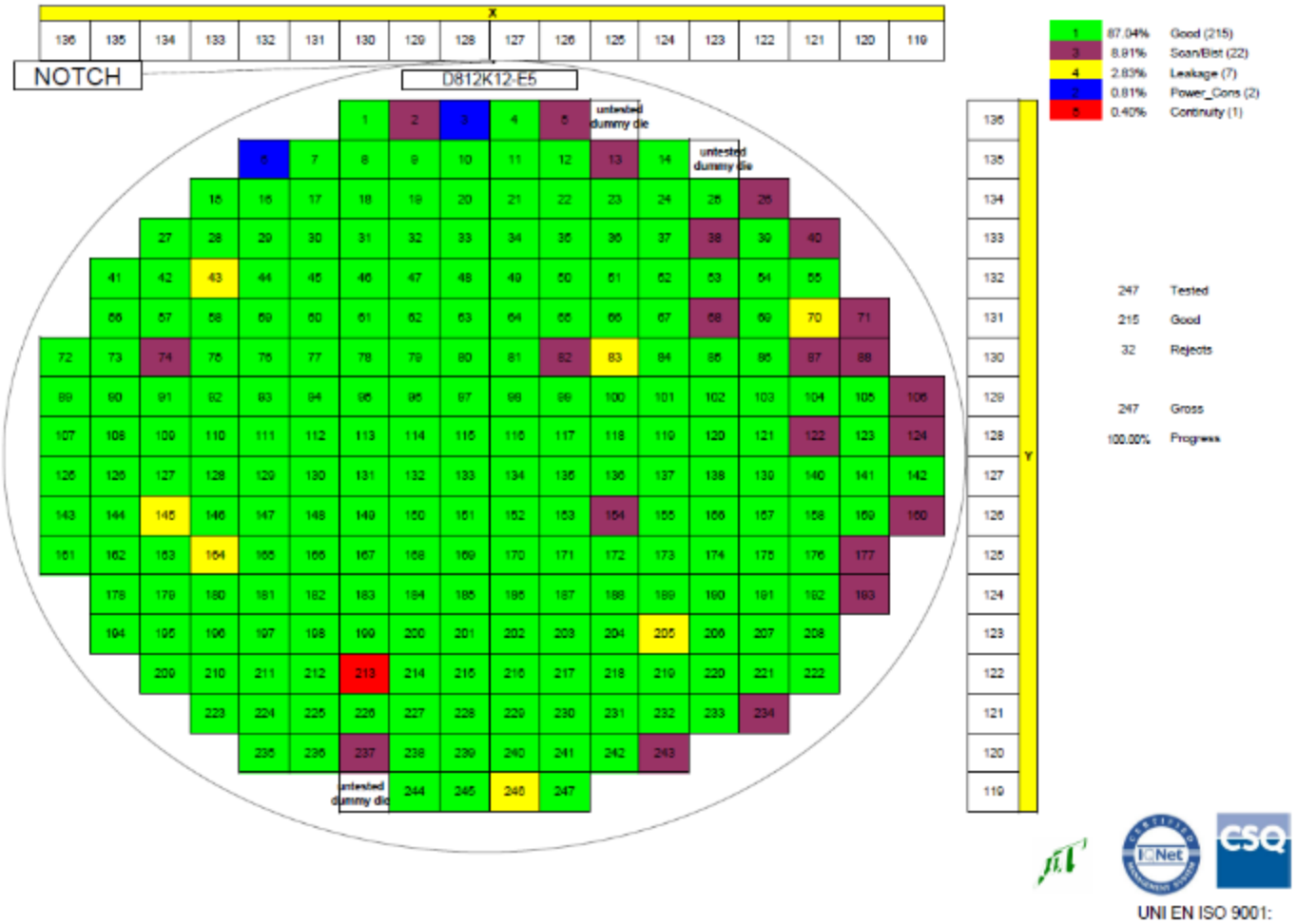
- Wafer maps generated
- Bad dies → Inked for identifications
- Good dies → Sawing → Packaging

WAFER PROBING

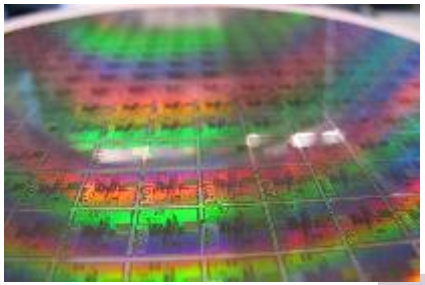


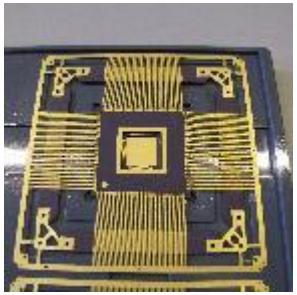


WAFER PROBING



ASIC SUPPLY CHAIN FLOW





Wafer foundry
- Dedicated mask-set
- MPW

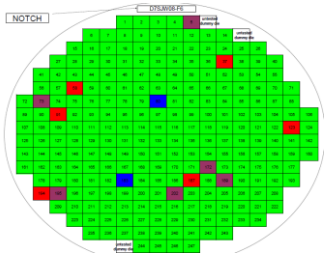
Test house
- Wafer level test
- Wafer map generation

Assembly
- **Package design**
- According to chart F2
- Trace-ability with respect to wafer map
- SEM Inspection

Final Test
- Test on packaged components
- Test over temperatures

Screening and Qualification
- Screening acc to chart F3
- Qualification acc to chart F4
- Radiation test

Delivery to customer



ASSEMBLY SERVICES – PACKAGE DESIGN

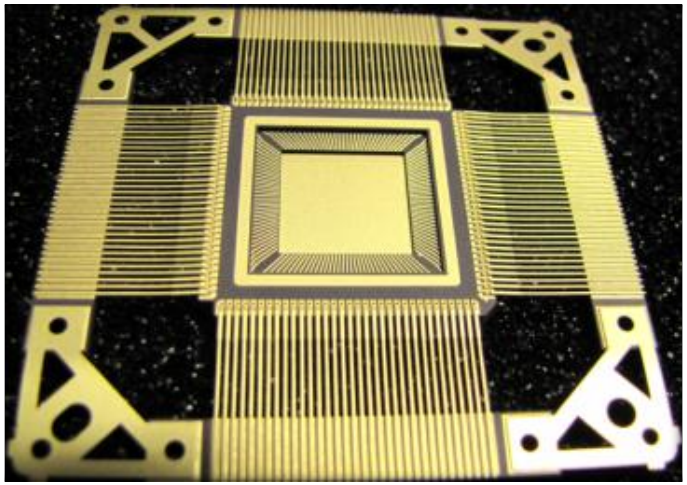
Flight modules need ceramic packages

- Requirements are very strict (towards build-up, material list etc…)
- Ceramic packages suitable for space are often "closed tools"
- Very expensive to customize dedicated packages

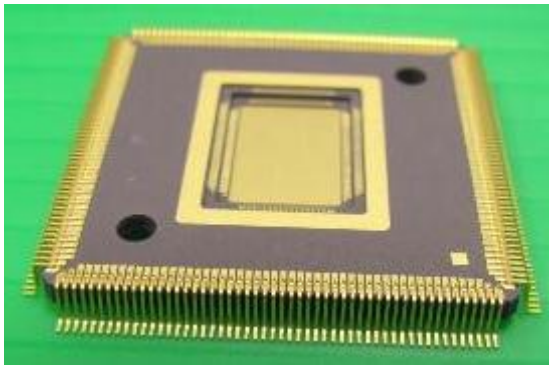
IC-link's vision is to provide a set of "standard re-usable" space compliant package to the space community

- Packages developed under ESA contract can be offered as an "open tool" for other projects under ESA contract

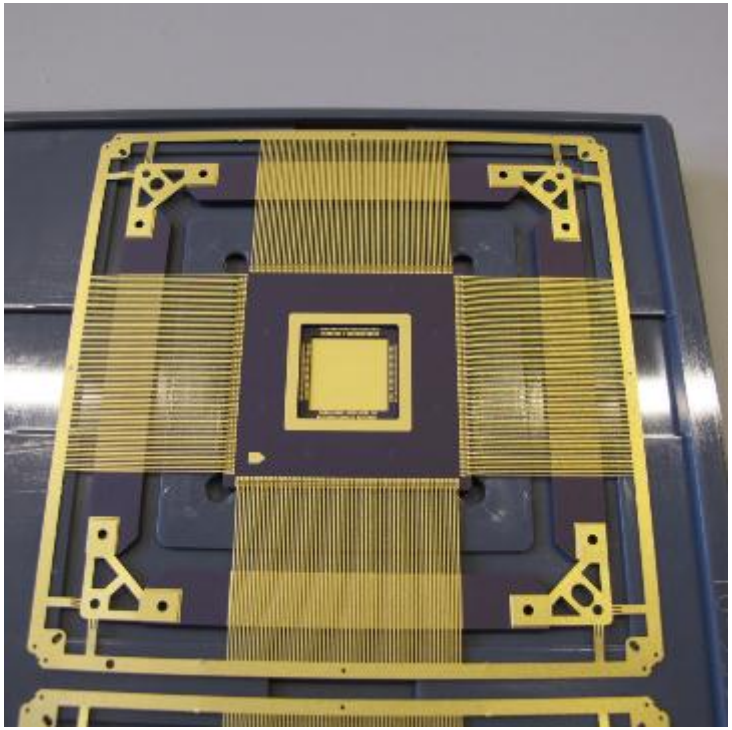
ASSEMBLY SERVICE - EXAMPLES



4-layer CQFP 132

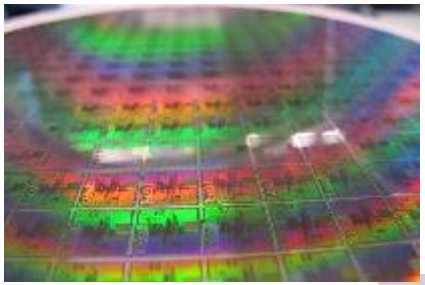


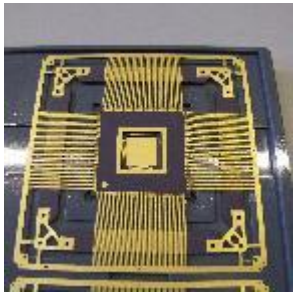
8-layer CQFP 208



13-layer CQFP 256

ASIC SUPPLY CHAIN FLOW





Wafer foundry
- Dedicated mask-set
- MPW

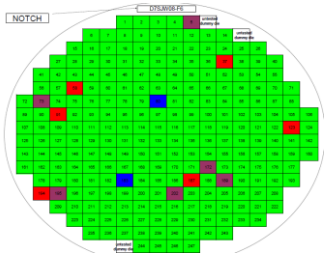
Test house
- Wafer level test
- Wafer map generation

Assembly
- Package design
- According to chart F2
- Trace-ability with respect to wafer map
- SEM Inspection

Final Test
- Test on packaged samples
- Test over temperatures

Screening and Qualification
- Screening acc to chart F3
- Qualification acc to chart F4
- Radiation test

Delivery to customer



TESTING SERVICE

Test capabilities

Test hardware & test program development

TESTING SERVICE – CAPABILITIES

- Many tester platforms available through partners to fit the needs for every application
  - 1x Teradyne A565
  - 2x Teradyne J750
  - 1x Teradyne IntegraFlex
  - 2x Teradyne MicroFlex
  - 1x Teradyne UltraFlex
- Powerful Automated Test Equipment (ATE) available

Full family of portable tester systems (**Hatina family**)

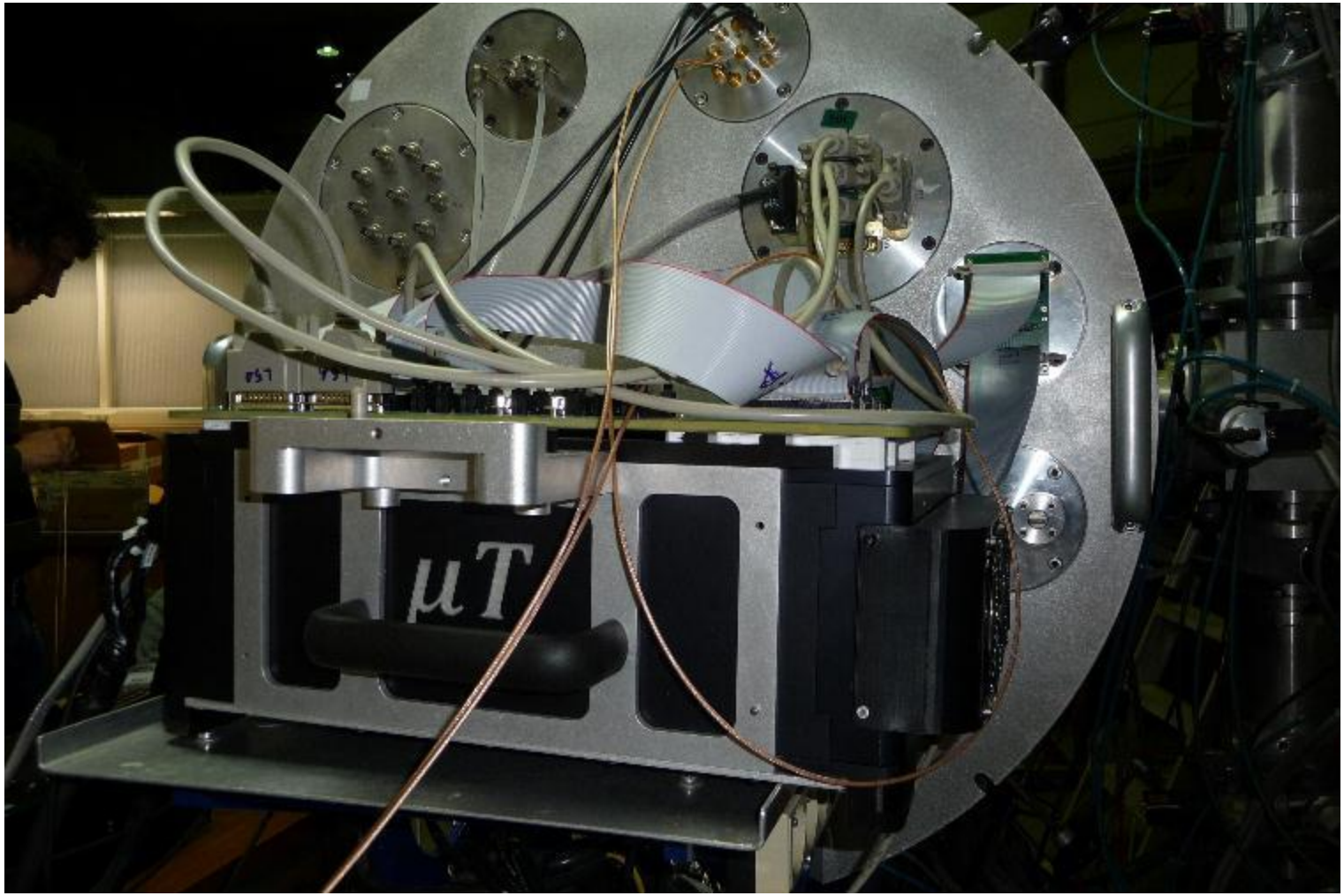
Reliability tests

- HTOL oven, capable of performing dynamic HTOL

TESTING SERVICE – HATINA FAMILY

- Brand of Microtest developed portable testers
- Latest member of the family: DMT (Digital Mixed Signal Tester)
- Fully configurable tester – suitable for radiation tests – ATE testing as well as bench testing

TESTING SERVICE - HATINA

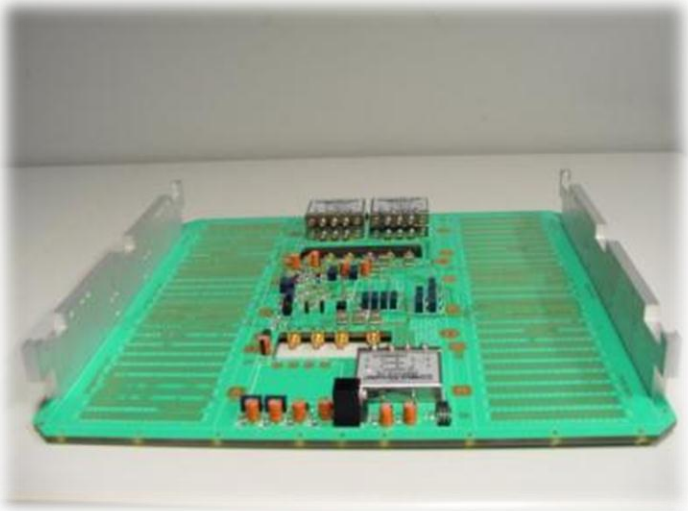


TESTING SERVICE

Test capabilities

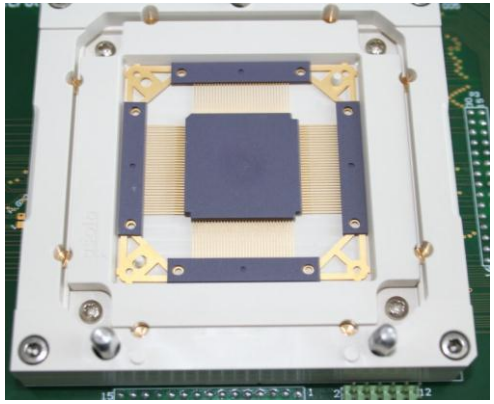
Test hardware & test program development

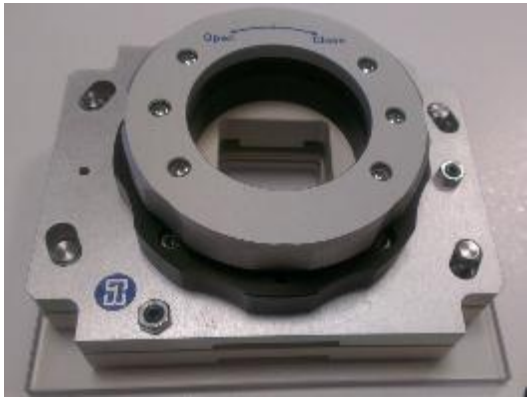
TEST DEVELOPMENT - HARDWARE



TEST DEVELOPMENT - HARDWARE

Dedicated sockets, high quality POGO sockets to guarantee signal integrity and minimize touch on package pins

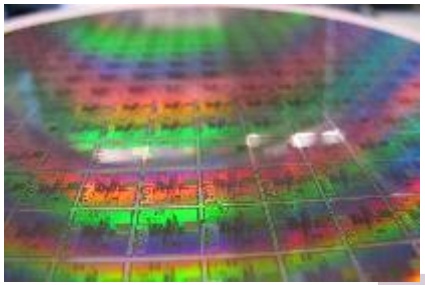


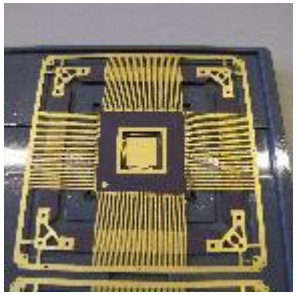


TEST DEVELOPMENT – TEST PROGRAM

- Characterization of the ASIC over samples
  - Purpose: Deep understanding of all ASIC specs
  - Histograms, statistical analysis, ...
- Production test program
  - Purpose: Screen out production failures
  - Flexibility to run the full program with a "push on the button"

ASIC SUPPLY CHAIN FLOW





Wafer foundry
- Dedicated mask-set
- MPW

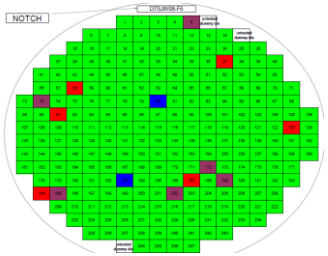
Test house
- Wafer level test
- Wafer map generation

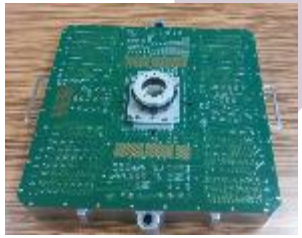
Assembly
- Package design
- According to chart F2
- Trace-ability with respect to wafer map
- SEM Inspection

Final Test
- Test on load board
- Test over temperatures

Screening and qualification
- Screening acc to Chart F3
- Qualification acc to Chart F4
- Radiation tests

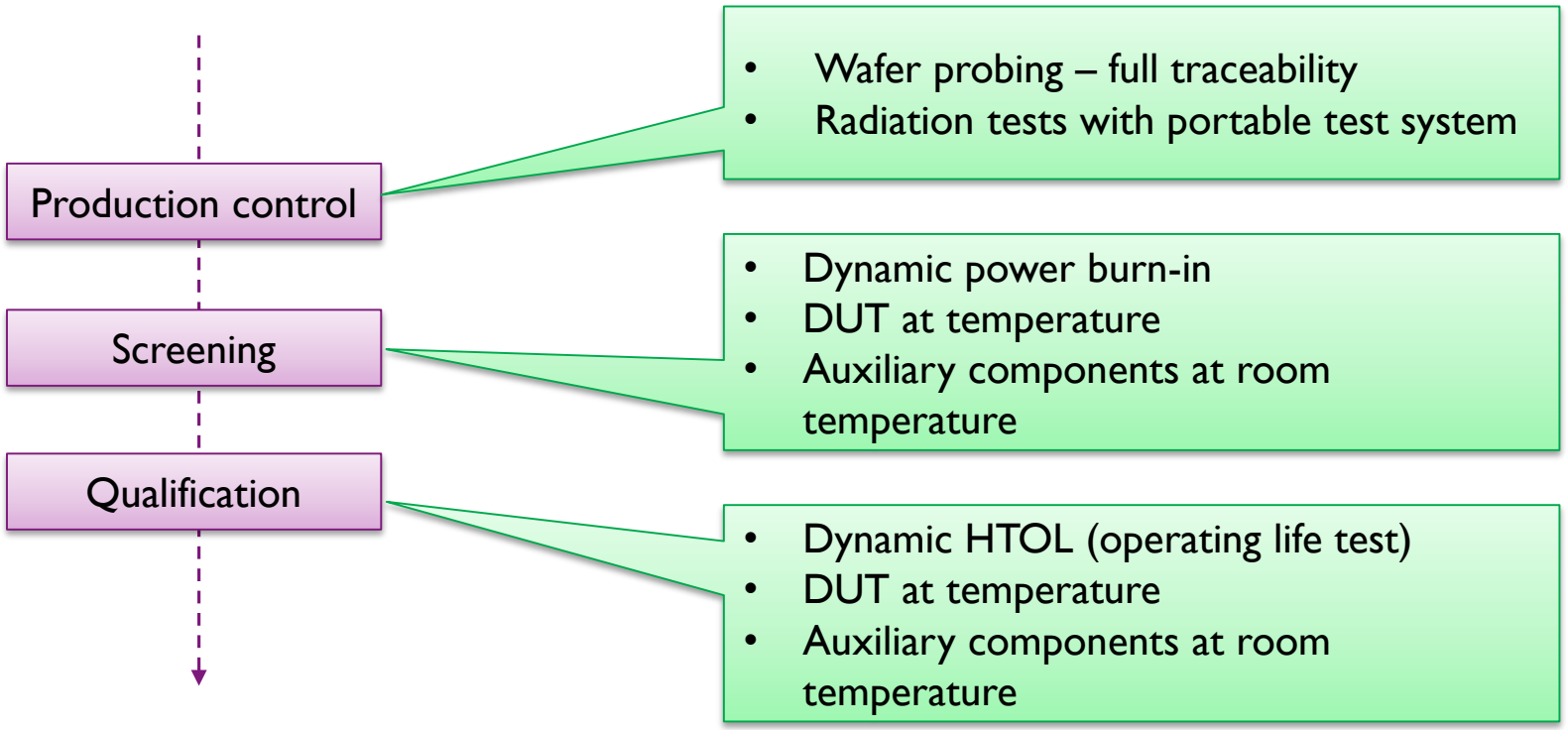
Delivery to customer



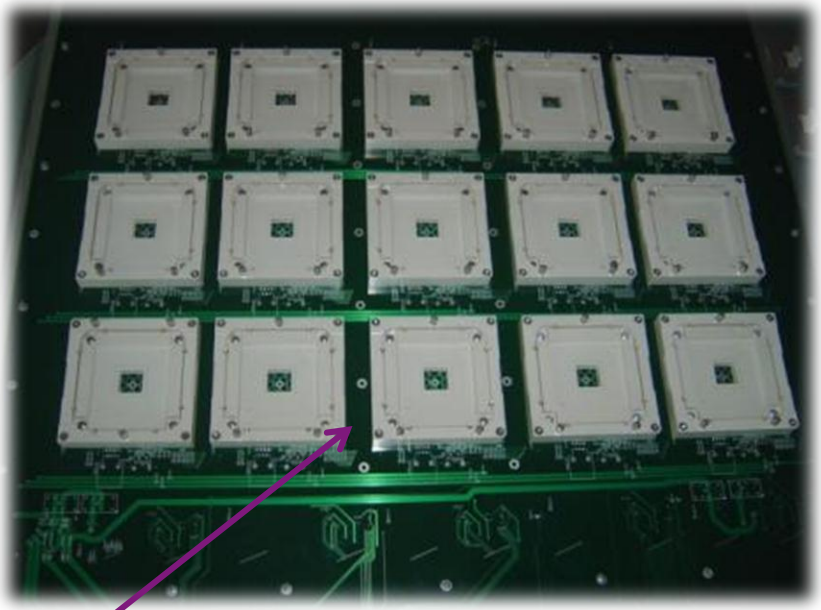


PROCUREMENT FLOW

Generic flow for qualification testing of ESCC 9000 compliant parts



PROCUREMENT FLOW – PBI/HTOL



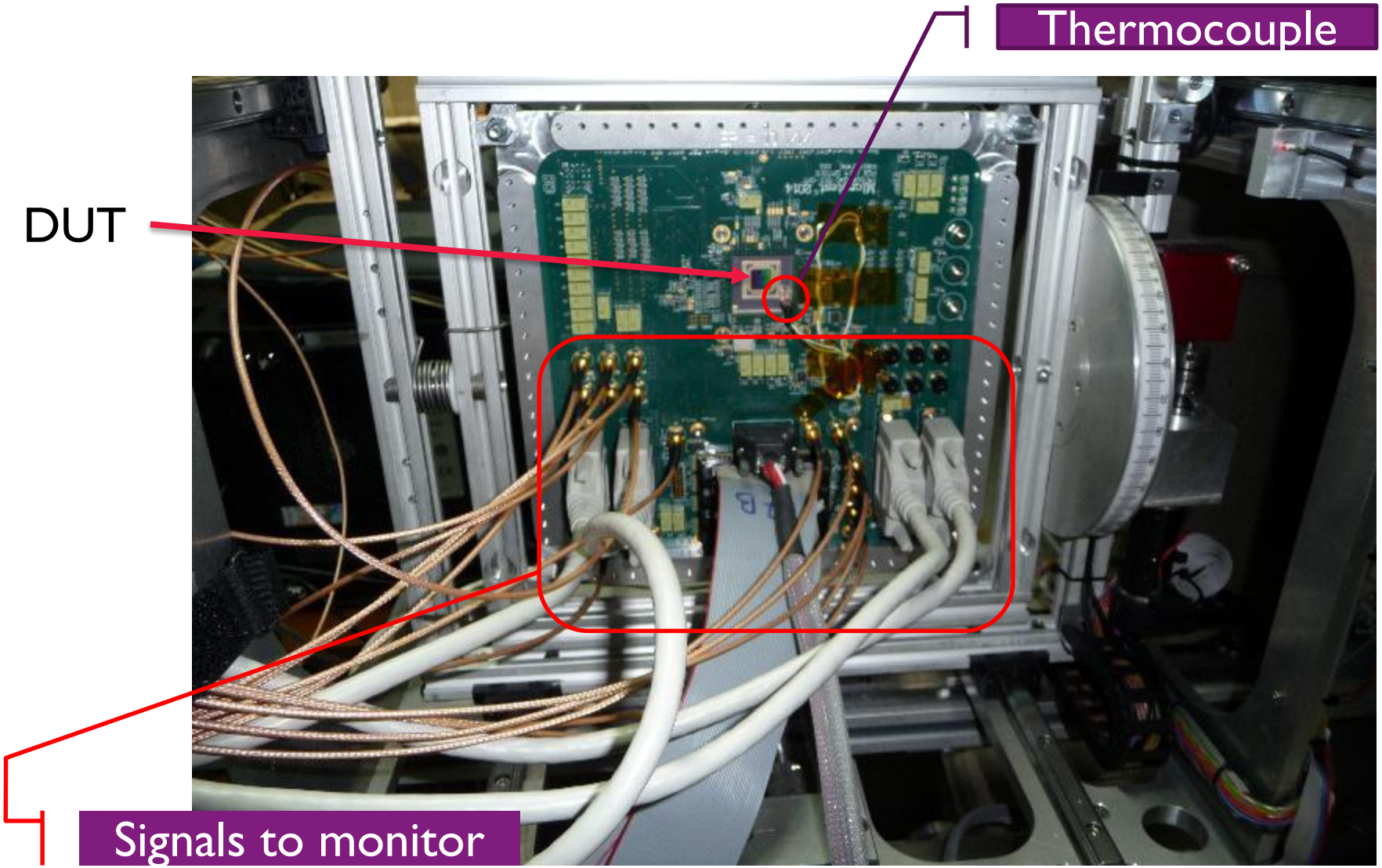
Top side

HTOL/Burn-in oven

ASIC is in functional mode – patterns running

Bottom side,
External comp's @RT

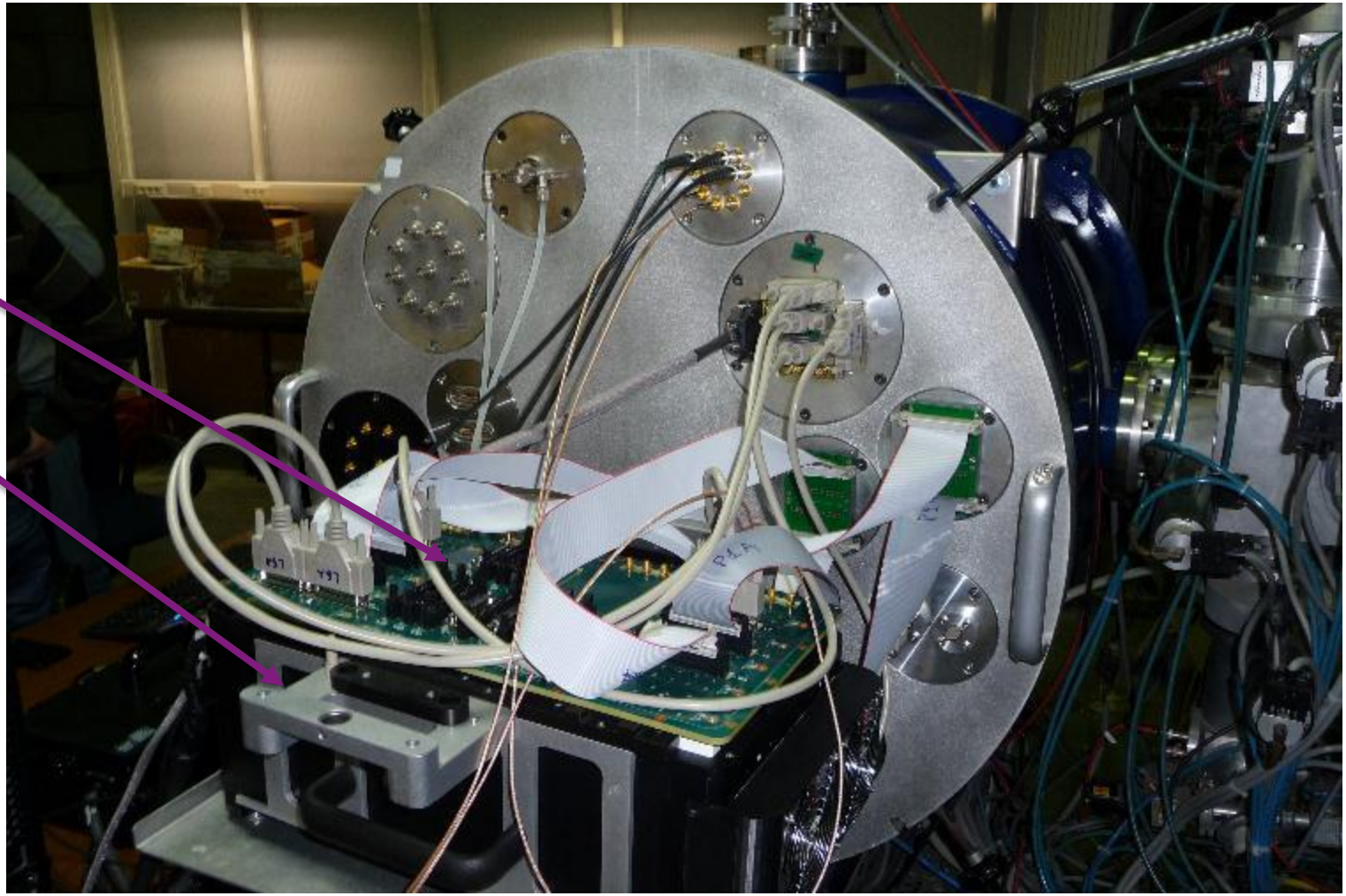
RADIATION TESTING - SEE



RADIATION TESTING - SEE

SEE DMT load board

DMT



RADIATION TESTING - TID

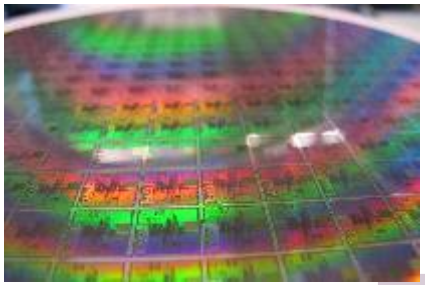
- In-situ testing with a production test program on Hatina DMT for deep understanding of the ASIC behavior under radiation

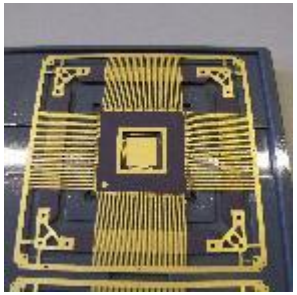
Dosimeters

TID load board,
10x devices

Intermediate test set-up, DMT

ASIC SUPPLY CHAIN FLOW





Wafer foundry
- Dedicated mask-set
- MPW

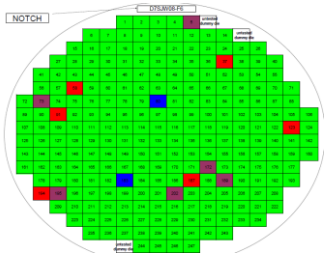
Test house
- Wafer level test
- Wafer map generation

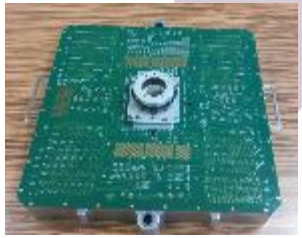
Assembly
- Package design
- According to chart F2
- Trace-ability with respect to wafer map
- SEM Inspection

Final Test
- Test on load board
- Test over temperatures

Screening and qualification
- Screening acc to Chart F3
- Qualification acc to Chart F4
- Radiation tests

Delivery to customer





TOPICS

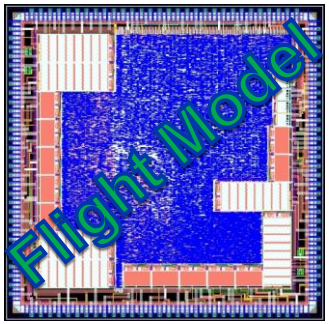
Imec, more than DARE

ASIC Supply Chain Flow

Test Success stories

Conclusions

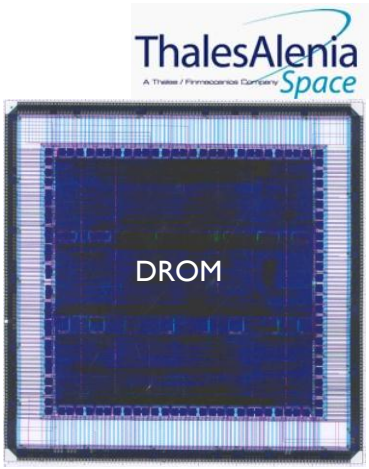
TEST SUCCESS STORIES



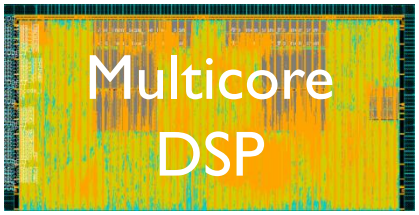
TESAT SPACECOM

ESA Qualified
to enter space

ADC & DAC
IP blocks



RECORE



TOPICS

Imec, more than DARE

ASIC Supply Chain Flow

Test Success stories

Conclusions

CONCLUSIONS

Imec IC-link

- is a specialized and tailored service provider
- capable of offering the services to design, produce and qualify your ITAR-free ASIC, from prototype to flight module
- Envisions to be a provider of custom "standard" packages
- Delivers a state-of-the-art test solution through best-in class subcontractors
- Aims to be an enabler of a European centered space compliant supply chain

QUESTIONS?

CONTACT PERSONS

ASIC Design manager

- Steven Redant: steven.redant@imec.be

ASIC volume production manager:

- Danny Lambrichts: danny.lambrichts@imec.be

Thank you for listening