



# imecDARE

## DAREI80UC

*UMC L180 CIS 1.8V/3.3V, DUAL POLY 4 METAL (2P4M), PSUB/TWIN-WELL CMOS*

**STATUS**



# STATUS

Application chips overview

ADK

Library

IP

Logistics

# STATUS

## Application chips overview

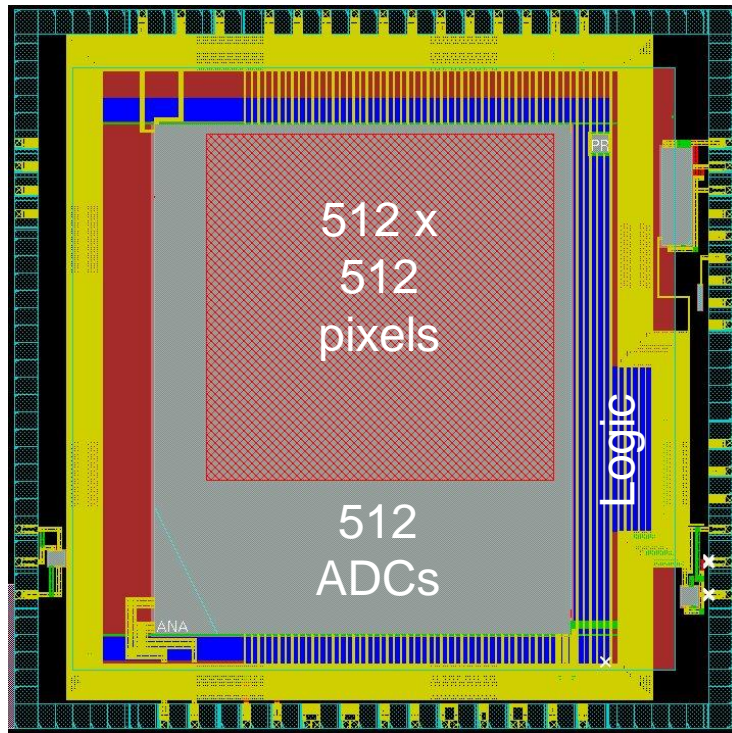
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# APPLICATION CHIPS OVERVIEW



SSoC

Tested



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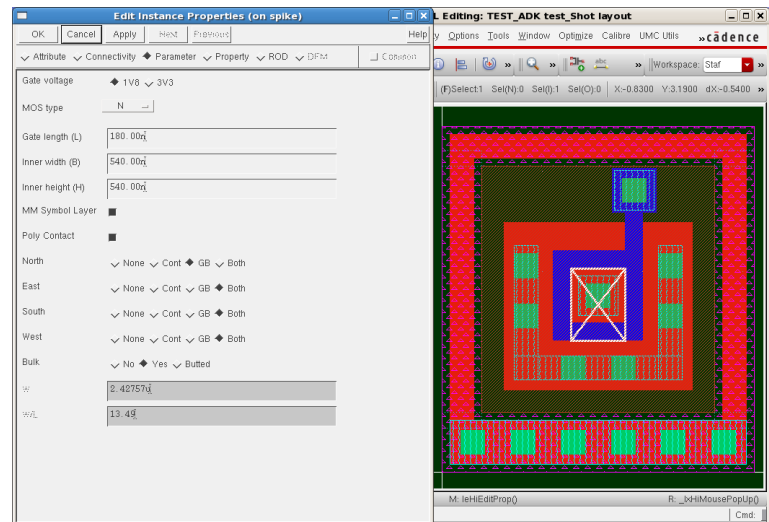
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# ADK

- Dedicated ELT layout/schematic Pcell
- LVS deck with ELT-recognition
- Improved ELT capacitance model in BSIM3v3 in collaboration with 
- RAD check



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# LIBRARY

## Releases

|      |          |  |
|------|----------|--|
| V1.0 | Sep 2009 | IC5, ELC, Encounter                                    |
| V2.0 | Sep 2013 | IC6, ALTOS, Encounter (based on DAREI80U release V5.4) |
| V2.1 | May 2014 | IC6, ALTOS, Encounter (cells added)                    |



# LIBRARIES

## ▶ **DAREI80UC\_CORE**

- same set of cells as DAREI80U\_CORE

## ▶ **DAREI80UC\_IO**

- Digital input/output/bidir, digital power/ground
- Breakers, fillers, corner, bonding pads, ...

## ▶ **DAREI80UC\_IOa**

- Analog input/output, 3.3V analog power/ground

## ▶ **DAREI80UC\_LVDS**

- Receiver, Driver, Biasmodule

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# IP

- ▶ Only 1 user of DAREI80UC with in-house analog design capabilities
- ▶ No active demand for analog IP compatible with CIS technology (no CIS user community)
- ▶ SRAM
  - No dedicated DAREI80UC SRAM compiler exists
  - DAREI80U compiler layouts are compatible with CIS technology
  - CIS transistor models and metallization parasitics are different => .lib is not correct and needs recharacterization
  - Extra floor planning effort due to reduced metal stack

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# LOGISTICS

- MTC-Online will disappear
- Data space per project or company for distribution of kits and other files.
- [dare\\_support@imec.be](mailto:dare_support@imec.be) is preferred way for DARE related support



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