imecDARE

DARE180U

UMC L180 MM/RF 1.8V/3.3V, SINGLE POLY 6 METAL (1P6M), PSUB/TWIN-WELL CMOS

esa

imec

STATUS

STATUS

Application chips overview

ADK

Library

IP

Logistics

STATUS

Application chips overview

ADK

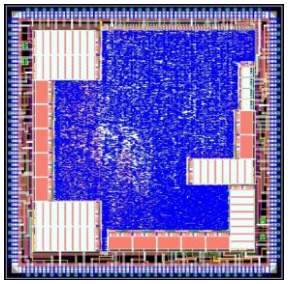
Library

IP

Logistics

APPLICATION CHIPS OVERVIEW I

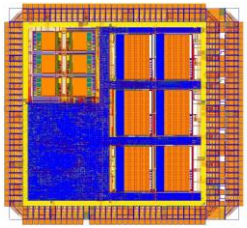
TESAT SPACECOM



KNUT

Flight Models
2nd lot qualified

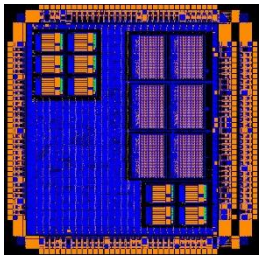
TESAT SPACECOM



LARS

Characterized

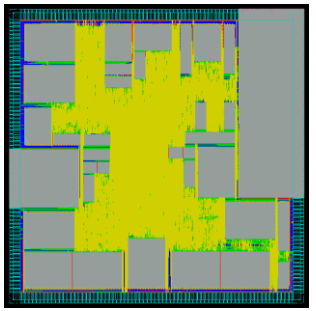
TESAT SPACECOM



LARS2

Taped out

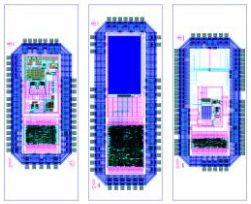
ThalesAlenia Space



DPC

Under Test

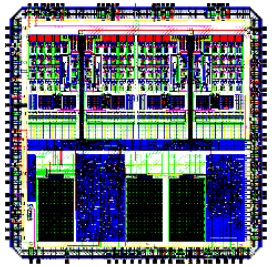
SRON Netherlands Institute for Space Research



Shamrock

Radiation Tested

SRON Netherlands Institute for Space Research



Cryogenic

FAIR

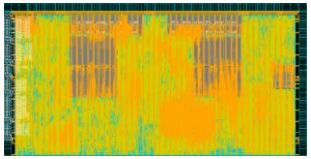
Samples delivered

esa

imec

APPLICATION CHIPS OVERVIEW II

RECORE



XentiumDARE

Tested (cf. DSP days)

ThalesAlenia Space

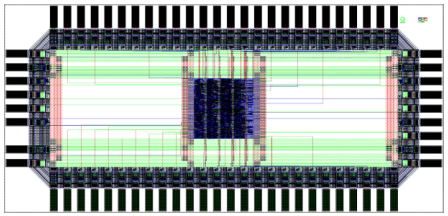
RECORE

2x Xentium +Leon

SSDP

Architecture Definition

ARQUIMEA



Digital companion to I3T80 chip

Built into Hybrid & qualified

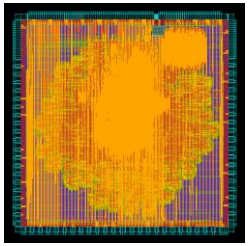
S.A.B.C.A.

CLP

CLP

Architecture Defined

AEROFLEX GAISLER



SpWRouter

Tested

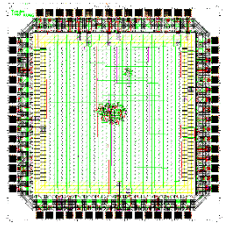
AEROFLEX GAISLER

Micro-Controller

uC

Architecture Definition

RUAG



Relco

Tested

esa imec

APPLICATION CHIPS OVERVIEW III

ALTER TECHNOLOGY

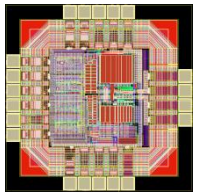
CNM CSIC

Fast ADC

Fast ADC

Detailed Design

esa



CAN transceiver

Tested

AEROFLEX GAISLER

LVDS Dual Transceiver

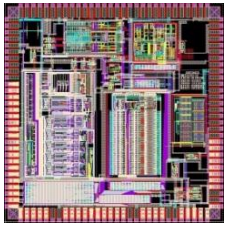
LVDS 4x4 Cross point Switch

LVDS

2nd test vehicle

Taped out

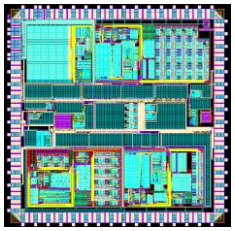
ARQUIMEA



HF configurable instrumentation front-end

Tested

ARQUIMEA



MF configurable instrumentation front-end

Taped out

esa imec

STATUS

Application chips overview

ADK

Library

IP

Logistics

DARE+ project:

- Device Test Vehicle
- Library Test Vehicle
- XentiumDARE Application ASIC

Final Present tomorrow @9AM

STATUS

Application chips overview

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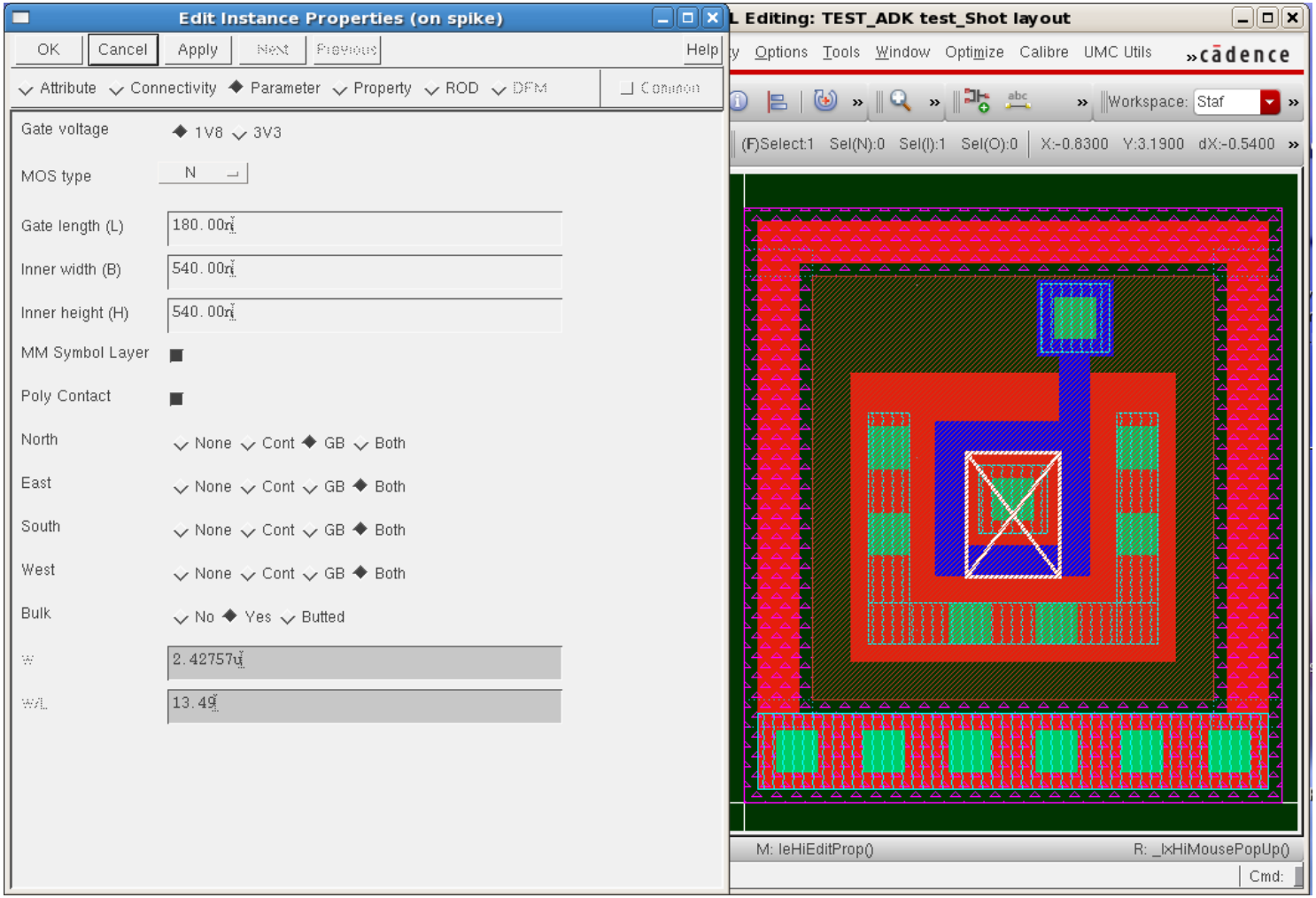
ADK
LAYOUT/SCHEMA PCELL



CERN formula also in excel sheet for design

ADK
LVS AND PARASITIC EXTRACTION

- Recognition of ELT models and W/L computation according to CERN formula
- Check inner-outer diffusion matching between schema and layout
- Improved transistor parasitics modeling in cooperation with CMOSIS image sensors

ADK
RAD CHECK

Additional check for:

- Poly crosses P+diffusion guard
- Nmos gate NOT enclosed
- 1.8V Leaky STRAIGHT N+diffusion regions
- 3.3V Leaky STRAIGHT N+diffusion regions
- 1.8V Leaky ELT N+diffusion regions
- 3.3V Leaky ELT N+diffusion regions
- Leaky Nwell-N+diffusion regions
- Leaky Nwell-Nwell regions

STATUS

Application chips overview

ADK

Library

IP

Logistics

LIBRARY

Releases

V3.1	Nov 2007	Orig. LEONDARE, Ocean/SLC, IC4,
V4.1	Oct 2010	IC5, ELC, Encounter
V5.3	Feb 2013	IC6, Altos, Encounter (DARE+ elements)
V5.4	Aug 2013	New & impr. I/O, LVDS characterization, PLL
V5.5	Dec 2013	IBIS models, docs update, EM optimization in I/O

LIBRARY UPDATES

- **DARE180_CORE**
  - MULLERCRLSH added
  - XICGD2, XICGD4 and XICGD9 added
  - AOI21D0, OAI21D0 and SRMUXI21 added
  - *D6 invertors and buffers added
  - Input stage *D4 and *D9 buffers updated to D2
  - Name update: AOI21* to AOI22*, OAI21* to OAI22*
  - ME1 abutment fix TIEH and TIEL
  - Decap cells added
  - Guidelines for radiation hardened (front-end) design

LIBRARY UPDATES

- **DARE180_IO**
  - Bonding pads separated from IO
  - 2.5V cells removed
  - Diodes removed between 1.8V and 3.3V
  - ESD protection to VDD updated
  - BREAKER_ALL and FILLER_ESD added
  - Schmitt trigger levels adjusted
  - SRC versions added
  - 8mA and 16mA drive strength added
  - 5VT input stage updated
  - Nwell strap at VDD removed
  - 20KA compatibility

LIBRARY UPDATES

- **DARE180_LVDS**
  - No integrated bonding pads
  - Extended Common Mode Input Range
  - Power down added
  - Selectable reference

STATUS

Application chips overview

ADK

Library

IP

Logistics

IP

All soft IP can be used in rad-hard aware back-end flow like LEON3, EDAC, SpW IP, ...

SRAM

Single port compiler

Parameter	Minimum	Typical	Maximum	Unit
Junction Temperature	-55	27	145	°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	bits
Word Count	32	-	8192	words
Word Length	8	-	256	bits
Write Mask Granularity	8	-	-	bits
Operating Frequency	-	-	200	MHz
SRAM Cell Cross-section	NA	33×10^{-9}	NA	cm^2

Silicon Proven

Dual port compiler

Parameter	Minimum	Typical	Maximum	Unit
Junction Temperature	-55	27	145	°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	Bits
Word Count	32	-	8192	Words
Word Length	8	-	256	Bits
Write Mask Granularity	8	-	-	bits
Operating Frequency	-	-	TBD	MHz
SRAM Cell Cross-section	NA	120×10^{-9}	NA	cm^2

Silicon Proven

SRAM

Single port compiler

Parameter	Minimum	Typical	Maximum	Unit
Junction Temperature	-55	27	145	°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	bits
Word Count	32	-	8192	words
Word Length	8	-	256	bits
Write Mask Granularity	8	-	-	bits
Operati				MHz
SRAM C				cm^2

After .lib/.db generation, each new instance will be verified through PVT corners.

Silicon Proven

Parame			n	Unit
Junctio				°C
Supply Voltage	1.62	1.8	1.98	V
SRAM Size	256	-	262144	Bits
Word Count	32	-	8192	Words
Word Length	8	-	256	Bits
Write Mask Granularity	8	-	-	bits
Operating Frequency	-	-	TBD	MHz
SRAM Cell Cross-section	NA	120×10^{-9}	NA	cm^2

Silicon Proven

esa imec

STATUS

Application chips overview

ADK

Library

IP

Logistics

LOGISITCS

- MTC-Online will disappear
- Data space per project or company for distribution of kits and other files.
- dare_support@imec.be is preferred way for DARE related support

imecDARE

imec