Title:	Single GaN Chip HPA/LNA for Radar Applications		
Contract type	TRP	**Budget** *(K€)*	**319**
Company (-ies) *(including country)*	VIPER RF, UNITED KINGDOM		
Team *(name of the participant in the project)*	**Dr J Mayock, Dr S Chan, Dr T Vo, Mr T Le Toux, Dr Q Sun**		
(*) **Speaker (s)**	Jim Mayock	**Email**	Jim.mayock@viper-rf.com
Short Speaker Information *(experience and involvement in this project)*	Jim Mayock is Director and the Co-Founder of VIPER RF since 2008. Previously, he was Design Manager at Filtronic Compound Semiconductors. He has a B.Eng and PhD in Electronic Engineering from the University of Leeds. He is Technical Lead on this project.		
Summary of the activity *(maximum 400 words)*	The scope of this project is the feasibility and design of a Single-Chip Front-End (SCFE) for C-Band radar applications. Some of the key requirements include generating high levels of transmit power (>40W) and a low-noise and robust receiver structures on a single-chip. Gallium Nitride (GaN) on Silicon Carbide (SiC) technology is thus the optimum candidate for this application and exhibits the technical requirements such as high power-density and low-noise performance. In order to develop high power and high efficiency transmit power extensive characterisation has been carried out on a 0.25um GaN technology. This has included an iterative active load-pull scheme to generate the optimum conditions for maximum PAE. This approach is required to ensure that the TX PAE specifications are achieved and to minimise power dissipation thus reducing channel temperature and improving reliability. The load-pull has been carried out on a range of cell size and several power supply options. Hybrid LNAs have also been developed in the projects to investigate the effect of various technology and design factors on RF performance and robustness. A range of single-stage LNAs using foundry sample cells have been designed, manufactured and characterised for gain, noise, linearity and robustness. Also switch cells have been characterised to understand power handling and robustness. In each case performance has been compared to the foundry models to support the design phase. A set of MMIC SCFEs have been designed, simulated and layouts generated in-line with the required specifications. The designs are based on foundry models and the verification/characterisation carried out during the project. Also individual HPAs, LNA and switches have been developed to support the future development of the MMIC. A follow-on phase of the project would be to manufacture and characterise the designs presented.		

(*) The speaker needs to do the registration through the website