BUILDING BLOCKS FOR FUTURE RTUs (a survey)

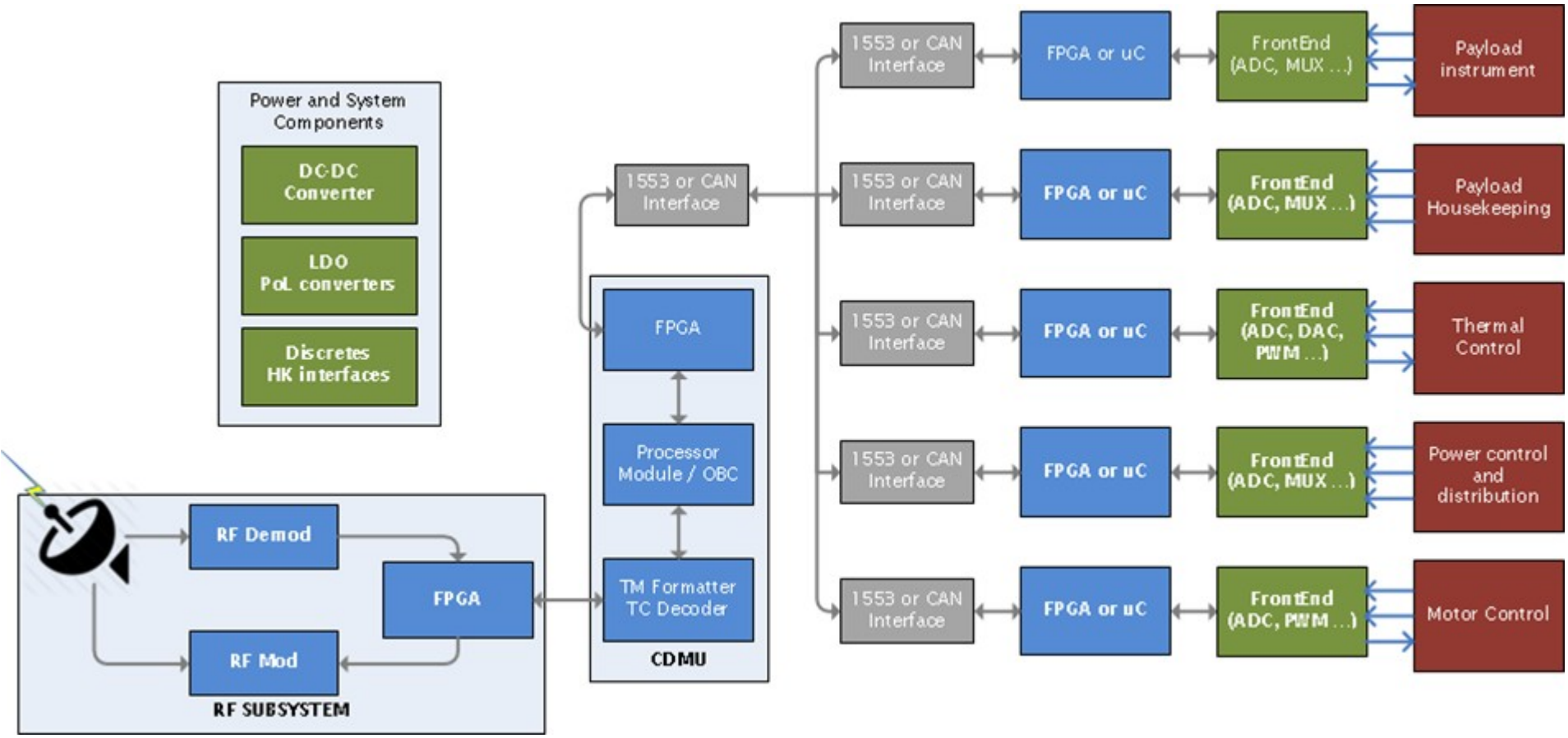
Gianluca Furano, Marco Rovatti
Ferdinando Tonicello
ESA-ESTEC Data System Division

ADCSS 2015 – Day 3
ESTEC - 21 October 2015

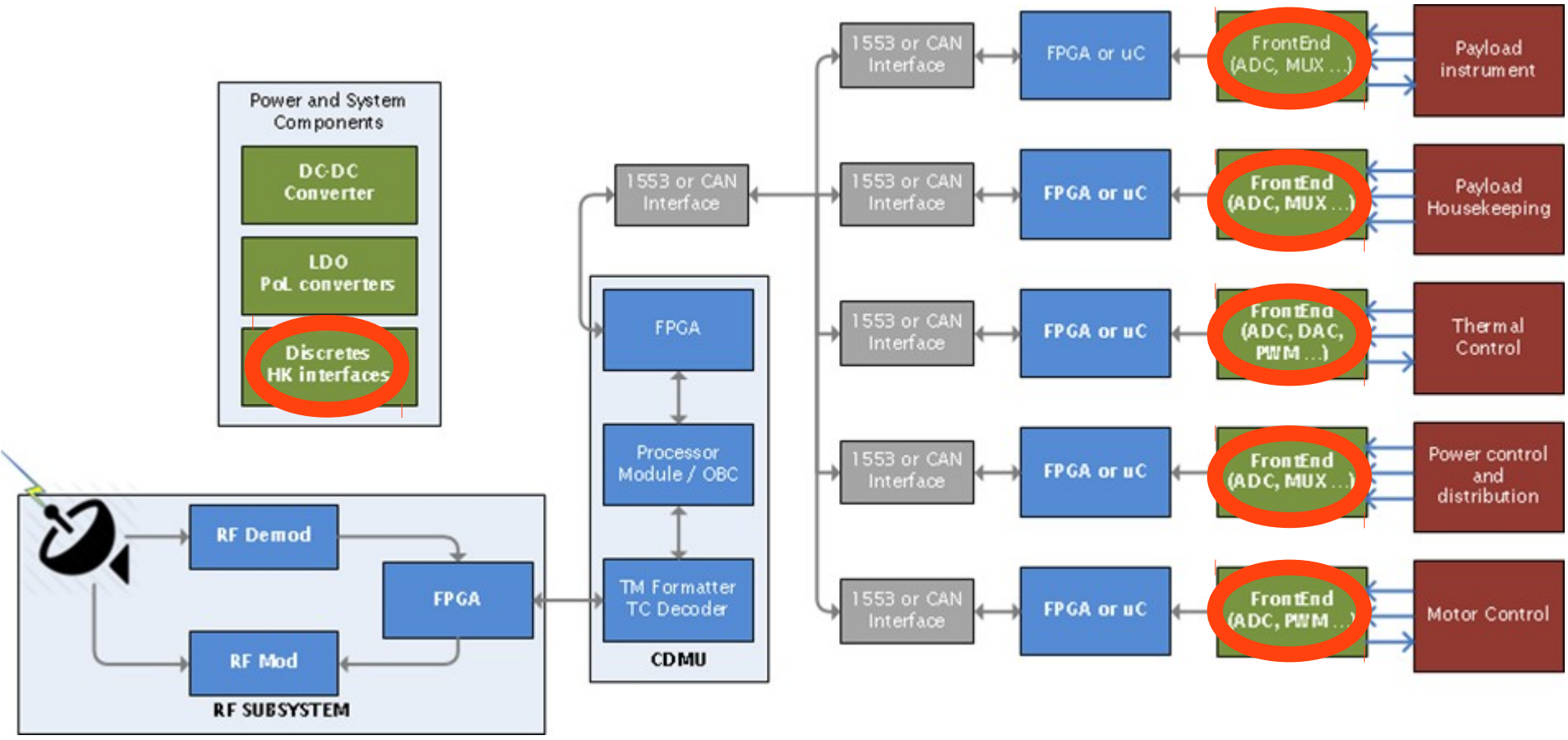
We will focus on three categories of Building blocks

- **Logic**
  - FPGA and Microcontrollers
- **Mixed Signal Front Ends**
  - Space System Managers
  - Transducer ASICs
- **Rad-Hard Power Management**
  - PoL

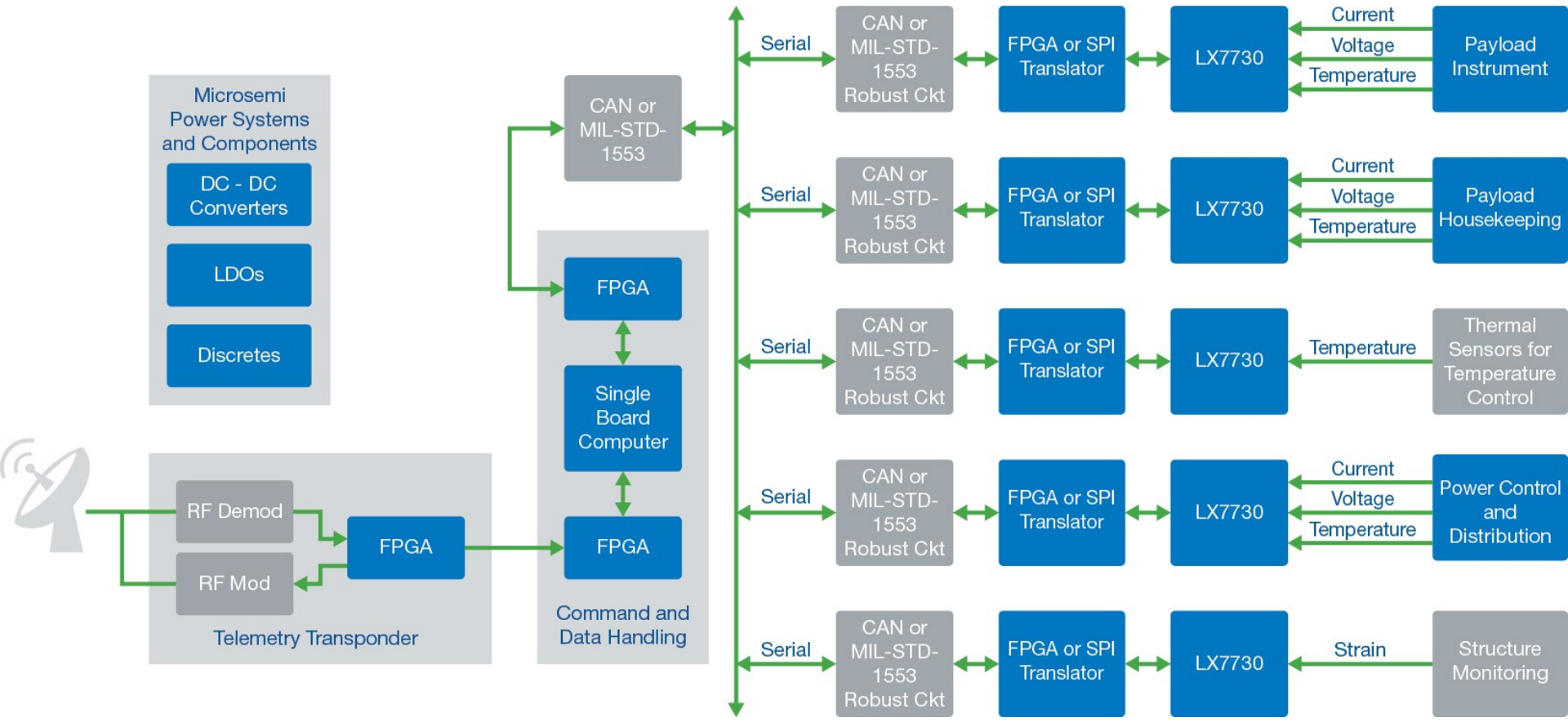
Building block MAP of RTUs functions



Building block MAP of RTUs functions

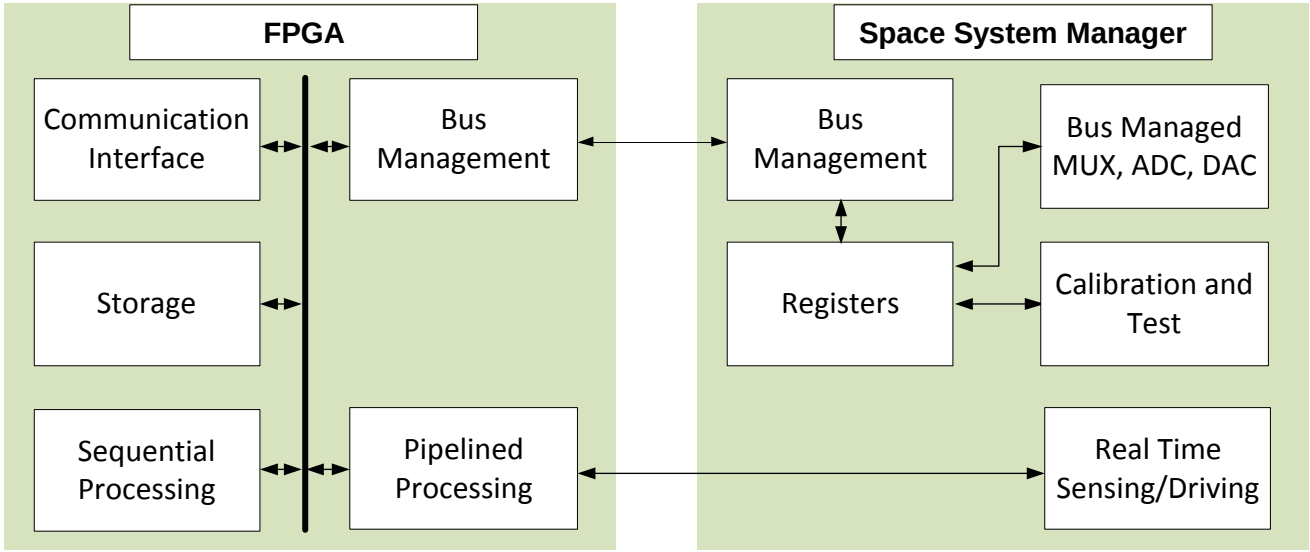


Microsemi vision on building blocks usage in RTUs



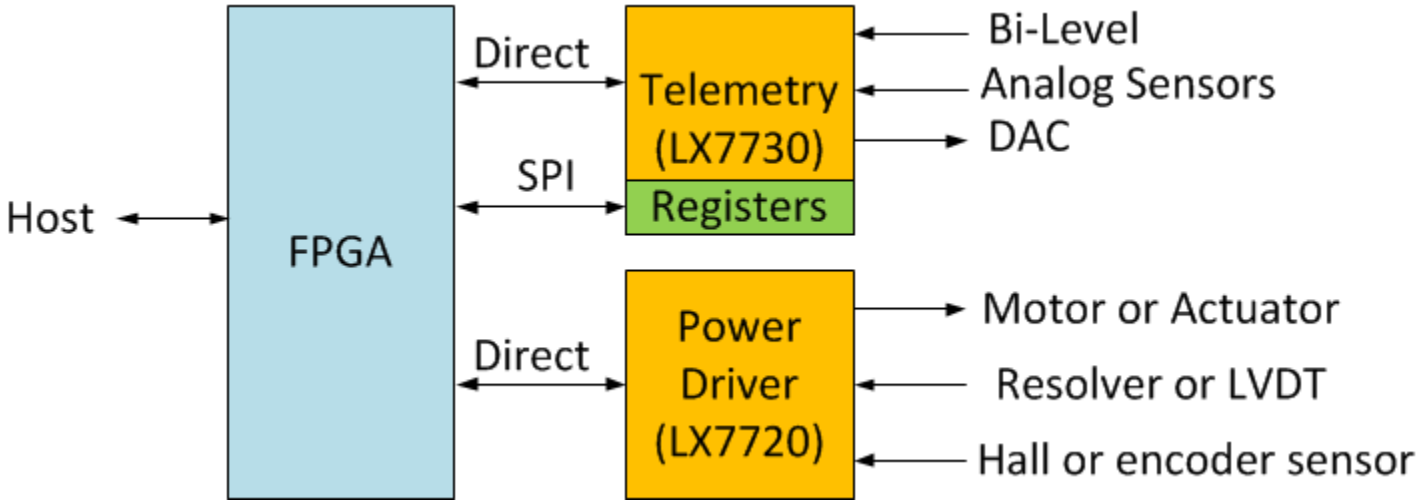
Space System Manager Concept

- Space System Manager (SSM) is a special purpose analog or power IC
- The SSM IC is intended to work with an FPGA:
  - I/O levels and timing are compatible.
  - The SSM has a minimal amount of hard coded internal logic.

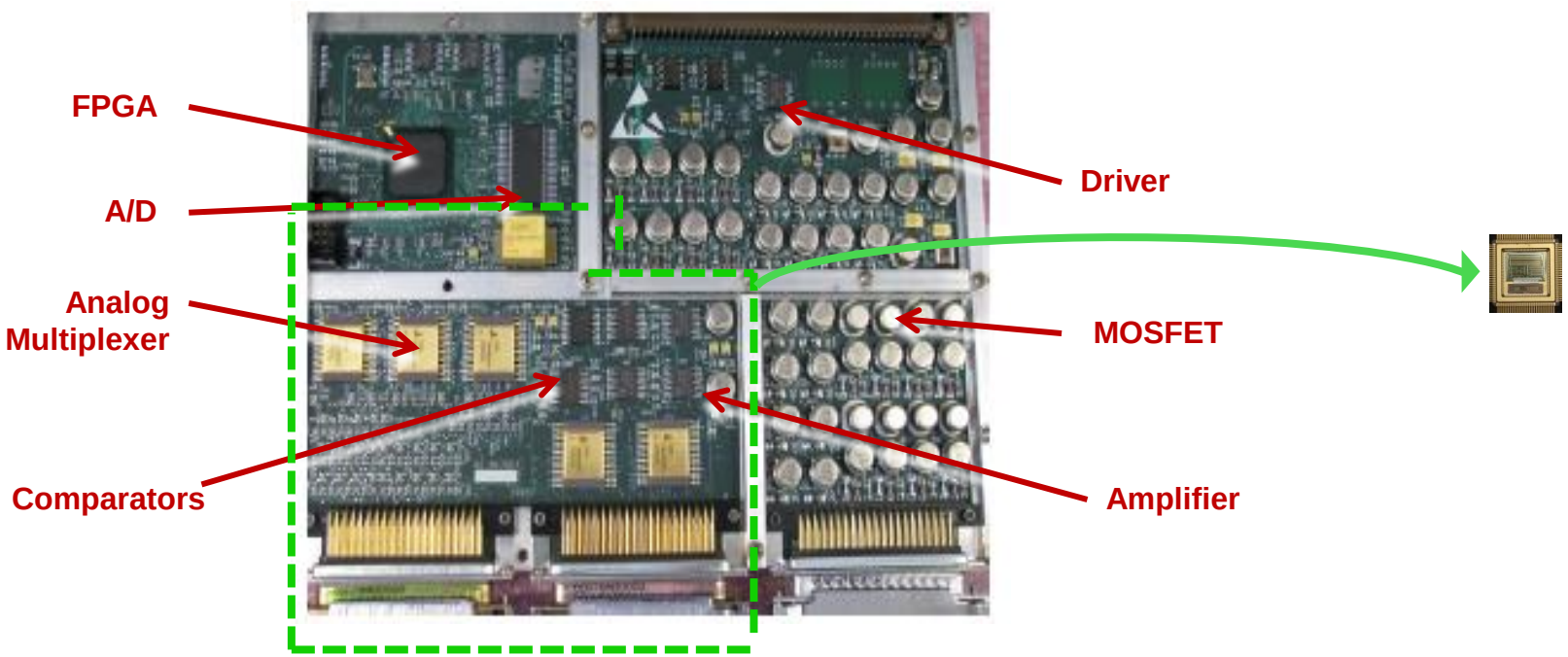


Space System Manager Characteristics

- Both the Space System Manager and the FPGA are standard parts that are space qualified and DLA listed.
- The SSM standard attributes are:
  - Radiation Tolerant: 100krad TID; 50krad ELDRS, SE tolerant
  - Inputs are cold spared and dielectrically isolated
  - ESD and overvoltage clamping



Space System Manager vs. Discrete Components



- A typical circuit uses an FPGA with analog interface functions implemented with many single function ICs and discrete components.
- SSM integrates commonly used functions into one package to reduce circuit board area and weight.
- Although utilization may not be 100% for the space system manger, it is still likely to be a more compact solution.

The Essential Telemetry (ETM) ASIC

A low-power, Rad-Hard ASIC for autonomous data acquisition.

Features:

- Autonomous scanning and sampling of discrete Analogue & Digital inputs
- 12-bit Analogue to Digital conversion (ADC)
- Built-in Rad-Hard Voltage Reference
- Sampling frequencies: 20 mHz - 4 kHz.
- Sampled data formatted into Space Packets

Interfaces:

- 32 differential analog inputs
  - 4 groups independently configurable for voltage or temperature measurements.
- 16 differential digital inputs
- CAN and PacketWire IF

The Essential Telemetry (ETM) ASIC

Applications:

- Essential telemetry collection without SW support for on-board computers/instrument control units.
- Spacecraft autonomous analogue to digital conversion and data collection.
- Remote Terminal Unit (RTU) in space data acquisition systems.

Characteristics:

- Low power < 15 mW (including CAN)
- Rad-hard to TID >1 Mrad
- SEL immune to LET > 67 MeV.cm2/mg
- SEFI immune to LET > 67 MeV.cm2/mg
- SEU free up to an LET of 40 MeV.cm2/mg

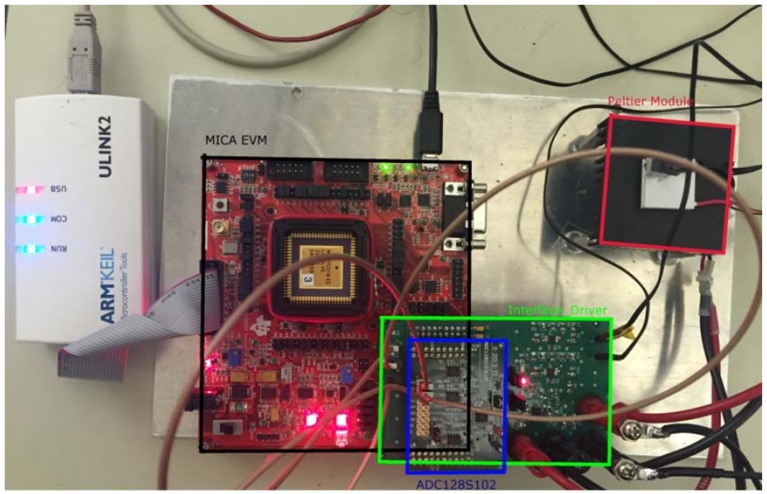
Contact: *SPACE-ASICS S.A., Athens, GR*
esarris@space-asics.gr, www.space-asics.gr

Space Grade:
Low Power, 8-channel, 12 bit, 1 MSps ADC
Peltier Thermal Management Demo

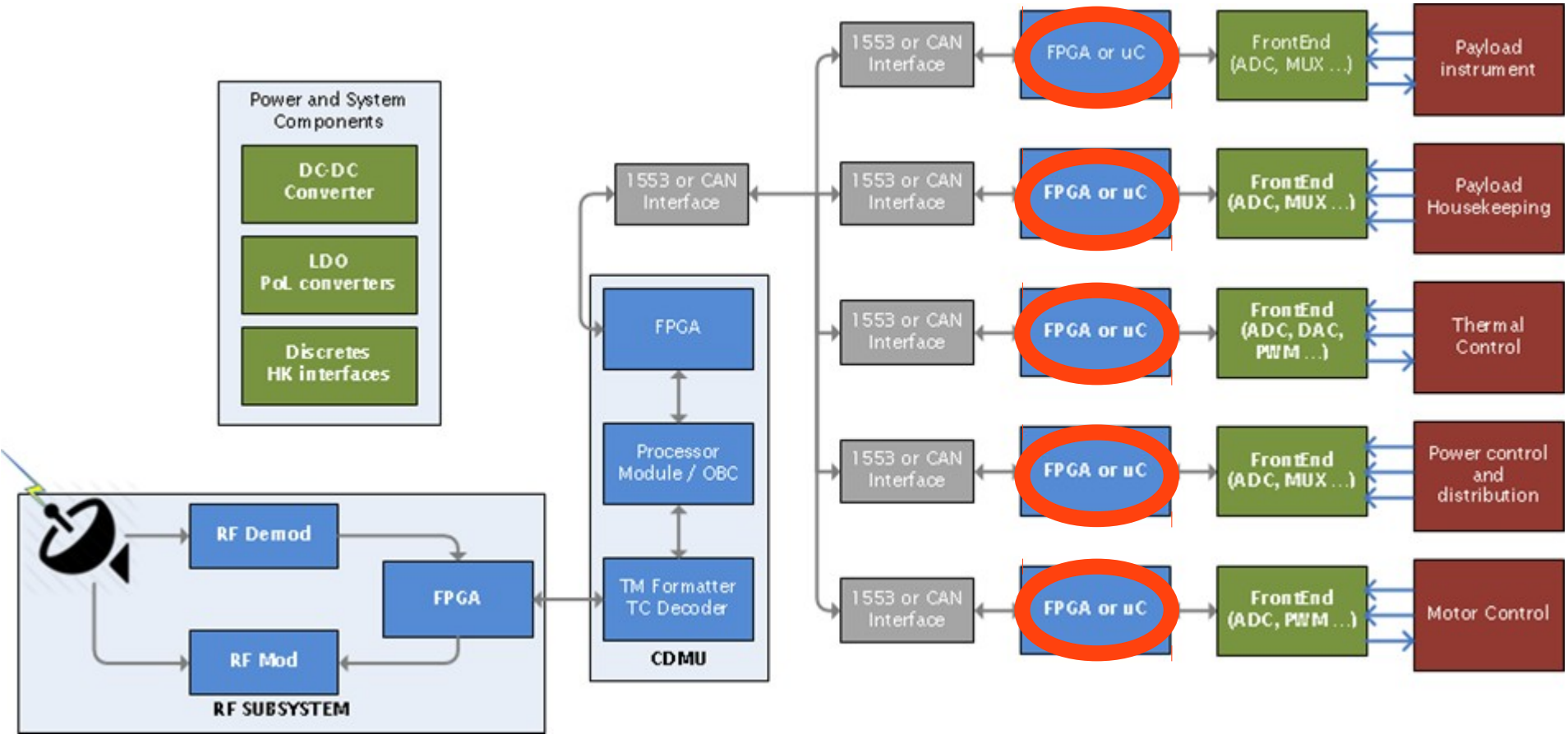
Texas Instruments

ADCSS ESA 2015

SEE THE DEMO LIVE AT THE EXHIBIT



Building block MAP of RTUs functions

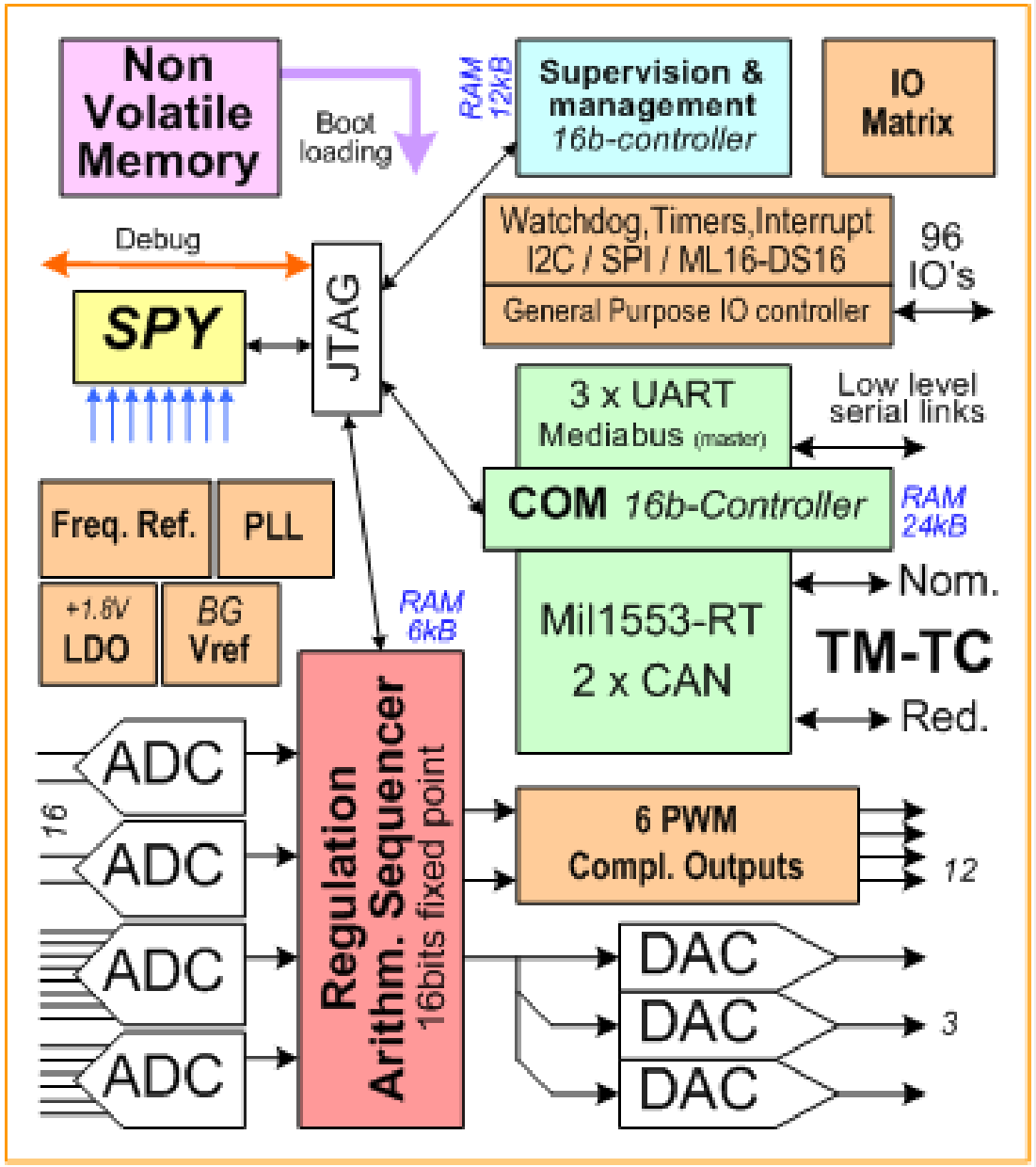


Main Features

- Triple 16 bits µC cores with embedded SRAM
- 6 independent PWM generators with complementary outputs
- 16 ADC inputs (13 bits, up to 1 MHz)
- 3 DAC outputs (12 bits, up to 1 MHz)
- 108 configurable general purpose IOs (LVCMOS & LVTTL up to 8mA)
- Hardware support for MIL-1553, CAN, UART, SPI, I²C, ML-16 & DL-16
- On chip band-gap & PLL & ref. oscillator
- Consumption: 120…550mA on 3.3V
- SEL free (to at least 78.2 MeV.cm²/mg)
- SEU: SRAM immune, registers immunity LET_{th} 40 MeV.cm²/mg, σ_{sat} 11e-3 µm²
- Total dose > 60krad(Si)
- -55°C to 125°C operating t° range
- Support of common development tools (Eclipse, gcc, gdb)
- Support of Python direct command interface for HW application debugging
- Reference kit (DRK) & FM plugin modules (DPM) available
- Not subject to US export regulations

- **Applications**
- The DPC circuit targets several applications mostly related to sensing and power conditioning
- Power conversion: DC-DC, AC-DC, DC-AC and AC-AC converters
- Motor control: DC (brushed or brushless), stepper motors & AC up to 6 phase motors
- Intelligent remote sensor: one example of such function is decentralized control of sensors
- Distributed bus client in power conditioning
- Data bus protocol translation (gateway): aggregation & concentration of connections to several clients and interface through e.g. standard mil-1553B or CAN buses.
- **Background**
- Products : RTU (Ceres), C-RTU (ExoMars), SDIU (satcom avionics)

Architecture



Atmel Aerospace – European Space Qualified solutions

Rad Tolerant Microcontrollers

AVR ARM

- SEL LET >60Mev
- SEU LET 3 to 10Mev
- TID 20 to 50KRad

- *Space grade QML*

Flex Matrix w QoS

DSP Co-processing

AES crypto

QFP48 to QFP144

ECC

Ethernet

TCM

LIN

-55°C & up to 150°C

DAC

PWM

SERCOM

CAN

3 to 5V

ADC

ATmega AVR8

20 MIPS
512B to 384KB Flash

SAMD21 SAMC21 Cortex-M0+

45 DMIPS
8KB to 256KB Flash

SAM4 Cortex-M4 + FPU

180 DMIPS
512KB to 2MB Flash

SAMV7 Cortex-M7 +FPU

600 DMIPS
512KB to 2MB Flash

SAMA5 Cortex-A5 NEON

850 DMIPS

SERCOM = Serial Communication Module, Configurable UART, TWI, SPI,…

RT development ongoing

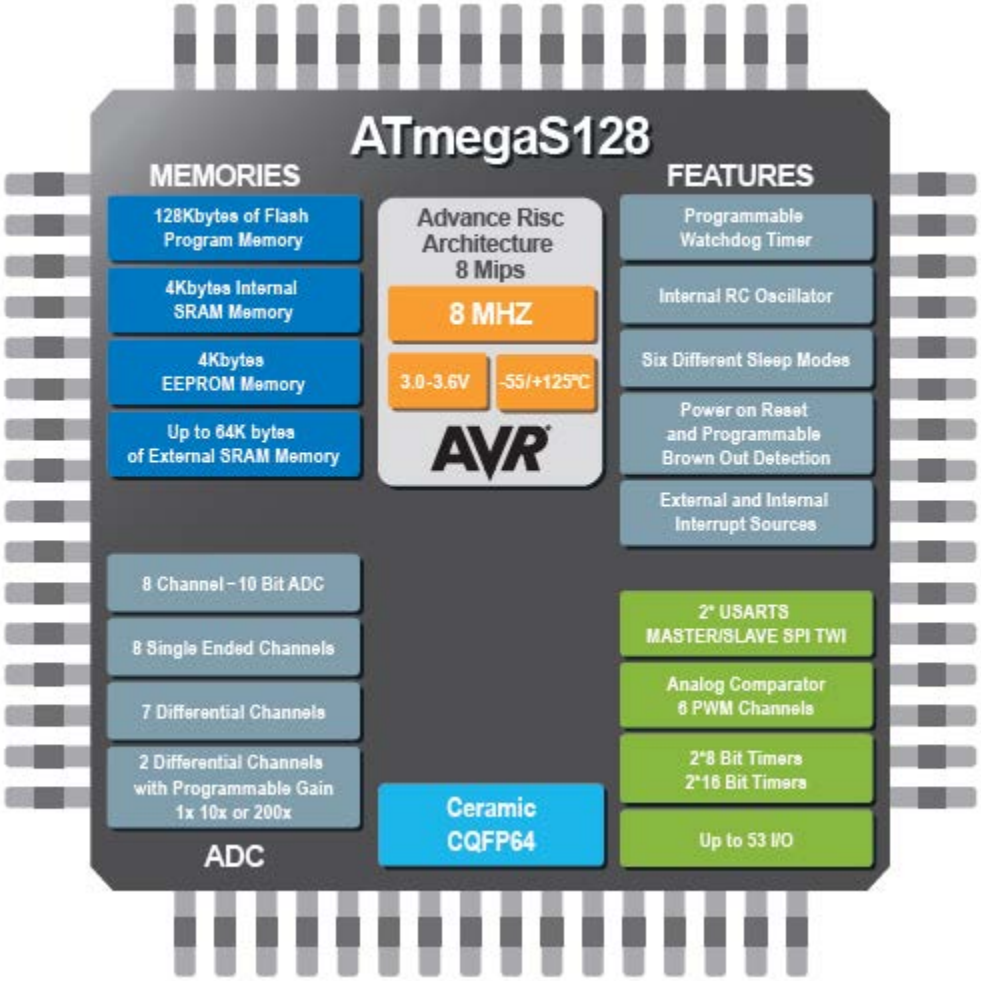
Atmel

ATmegaS128 Space Rad Tolerant Microcontroller

- **Technical Specifications**
  - ✓ 8bits mega AVR core up to 8Mips
  - ✓ Embedded Flash and Sram memories
    - 128 Kbytes of In-System Self-programmable Flash
    - 4 Kbytes EEPROM
    - 4 Kbytes Internal SRAM
    - Up to 64Kbytes optional external memory space
  - ✓ 2x UART, Master Slave SPI interface, TWI
  - ✓ 8 channel, 10-bit ADC with Programmable Gain
  - ✓ 1x 8 bit and 2x 16bit timer (with compare and capture mode)
  - ✓ 6 PWM Channel with Programmable Resolution from 2 to 16 Bits
  - ✓ Programmable Watchdog Timer with On-chip Oscillator
  - ✓ On-chip Analog Comparator
  - ✓ On-Chip Debug support
  - ✓ Power-on Reset and Programmable Brown-out Detection
  - ✓ External and Internal Interrupt Sources
  - ✓ Six Sleep Modes
  - ✓ JTAG (IEEE std. 1149.1 Compliant) Interface
  - ✓ 53 Programmable I/O Lines

- **Operating conditions & Package**
  - ✓ **3.3V / 8MHz - CQFP64 Ceramic Package**
  - ✓ **-55/125°C extended temperature**

ATmegaS128 – Block Diagram



ATmegaS128 Radiations Performances

- ***Single Event Latch-up***
  - No Latch-up up to 62.5 MeV/mg/cm2 @ 125°C
- ***Single Event Upset***
  - 3 MeV/mg/cm2 @ 125°C
    - 1 upset every 400 days in LEO (400km)
    - 1 upset every 15 days in MEO GEO
- ***Total dose***
  - Tested up to 30 Krad (Si)

European Microcontroller development

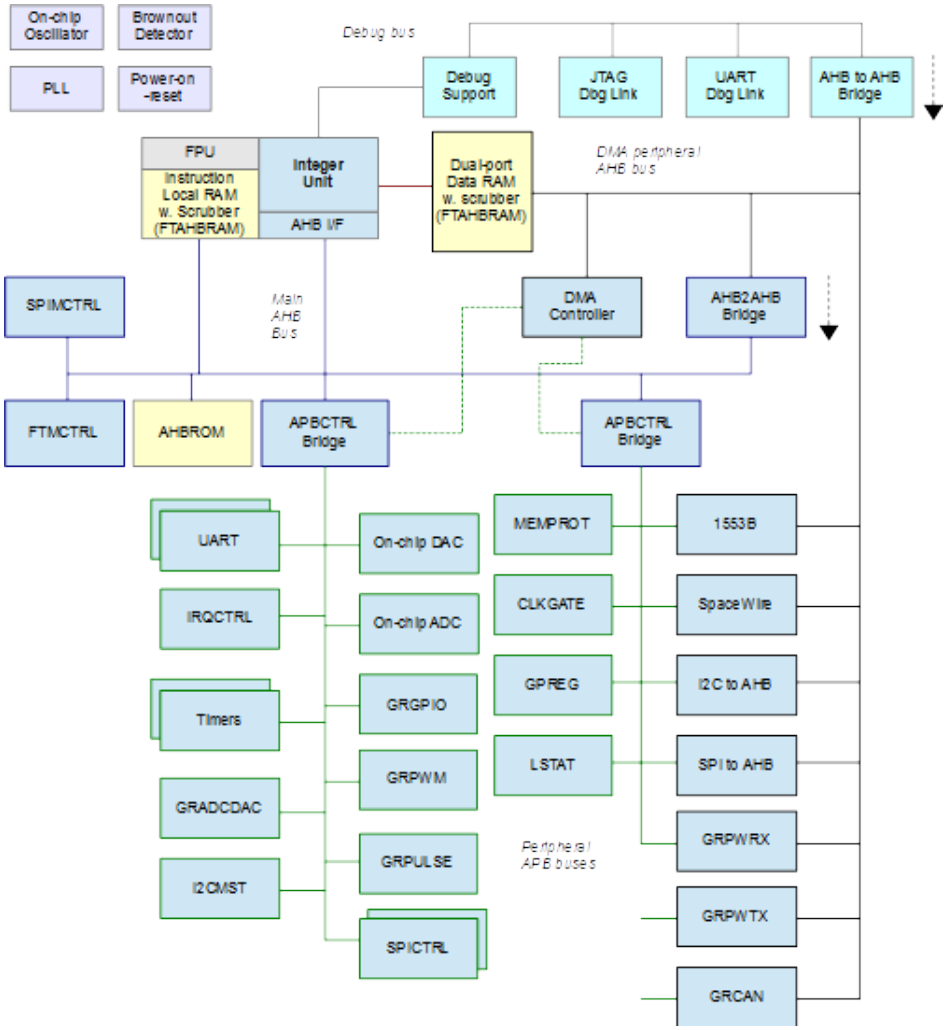
Fact sheet

- 180 nm UMC / DARE180+ radiation tolerant library
- Fault-tolerant LEON3 with 16-bit instruction set
- Double precision IEEE-754 floating point units
- On-chip DAC, ADC, Power On Reset, Brown Out Detection and Oscillator
- 192 KiB EDAC protected on-chip memory
- UART, SPI, I2C, GPIO, Timers & Watchdog, Interrupt controller, Status registers, JTAG
- SpaceWire
- MIL-1553B
- CAN-FD Support
- PacketWire
- Configurable I/O switch matrix
- Support for single 3.3V supply

European Microcontroller development

Digital subsystem

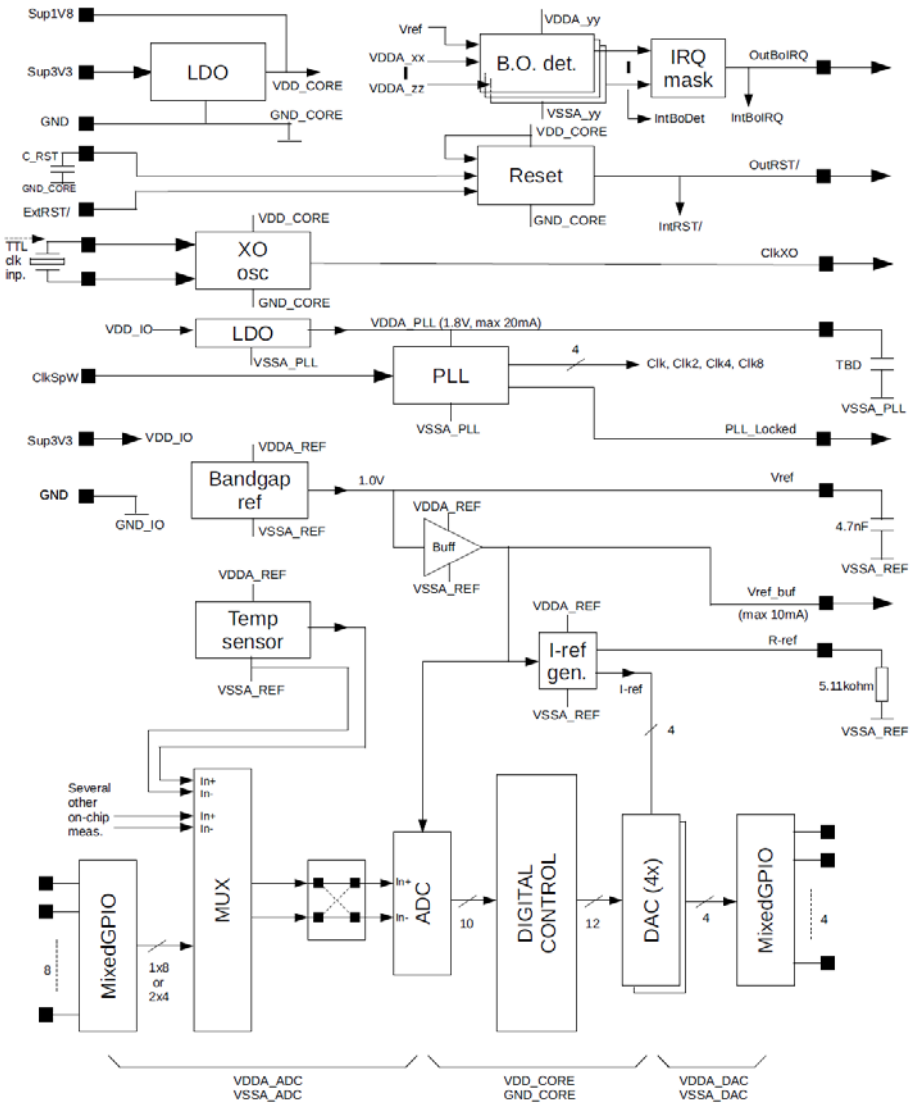
- LEON3FT with 16-bit instruction set
- Floating-Point Unit
- Deterministic software execution
  - Through local processor RAMs
  - Non-intrusive debugging
  - Reduced interrupt latency
- Fault-tolerance
  - EDAC on all on-chip memories
  - EDAC on external memory i/f
- Boot from external SPI, I2C, FLASH or SRAM
- Boot via SpaceWire, CAN, SPI, UART or I2C
- DMA Controller for processor off-loading
  - Event driven and programmable
- Atomic bit operations
  - Set, clear, xor, set&clear for on-chips rams and APB peripherals
- CRC HW Accelerators
- Pattern generation on outputs at CPU speed
- PWM and pulse generators
- Flexible clock scheme
  - Ultra low power mode (unused interface disabled by clock gating)
  - Low power mode (processor and selected peripherals disabled until event occur)
- Configurable I/O switch matrix



European Microcontroller development

Analog architecture overview

- On-Chip LDO for single 3.3V supply
- Reset and BrownOut detection
- On-Chip ADC channels
  - 10-bit 200KS/s
- On-Chip DAC outputs
  - 12-bit 100KS/s
- Integrated Temperature sensor
- Integrated PLL
- Mixed signal general purpose IO
  - Internal pullup/pulldown resistor
- Internal and external voltage references
- All analog blocks are Rad Hardened

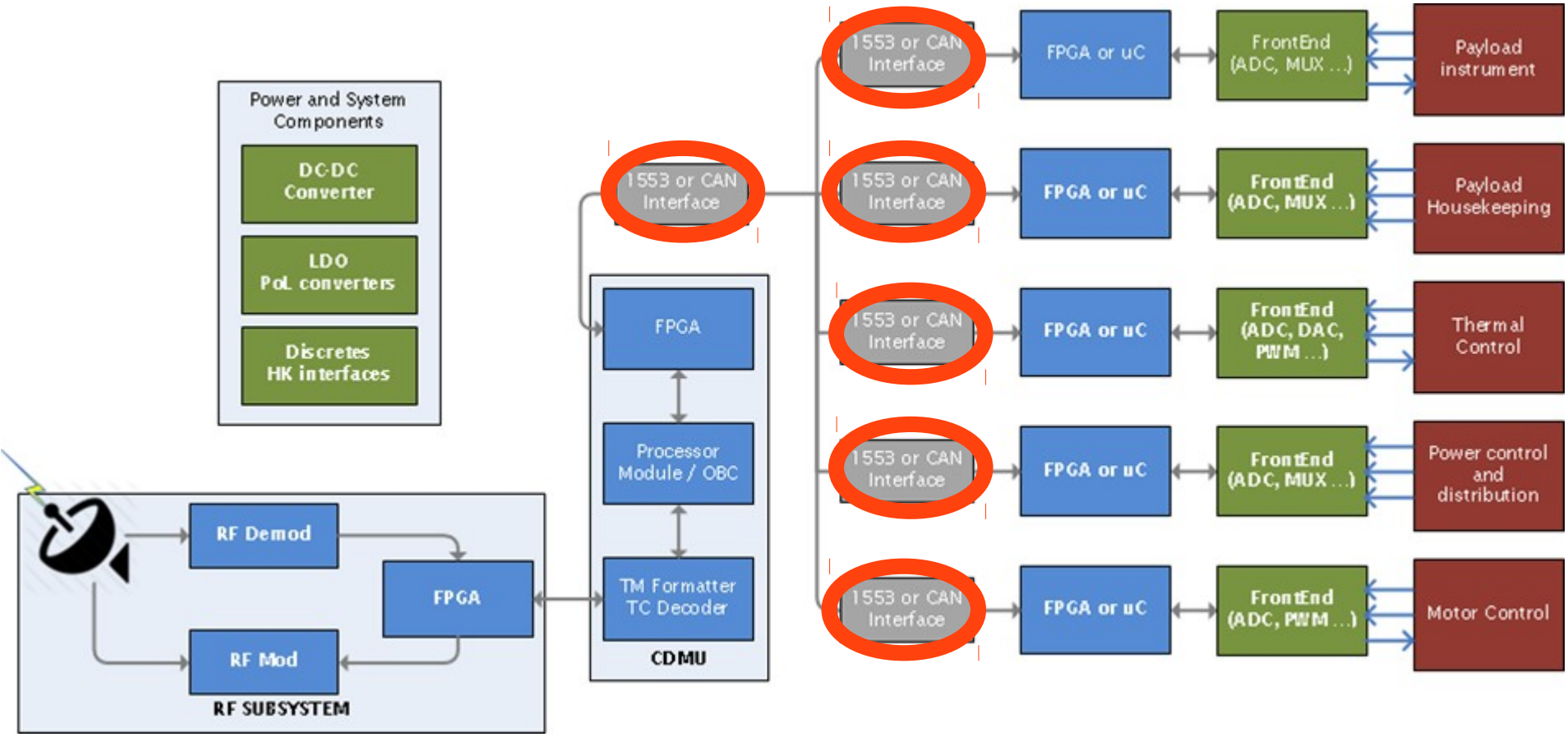


European Microcontroller development

Time plan

- Digital and analog architecture set and reviewed
- Mixed digital and analog verification is ongoing
- Layout and verfication of new analog IP cores are ongoing
- Tapeout planned to Q1 2016
- Verfied devices available Q3 2016

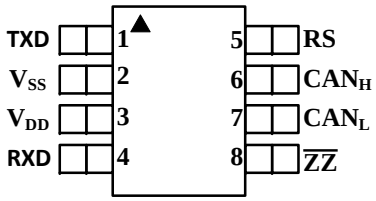
Building block MAP of RTUs functions

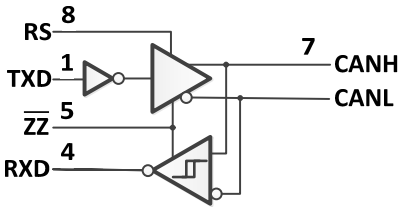


Introduction to Cobham CAN Transceivers

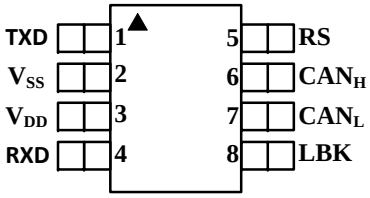
UT64CAN333x

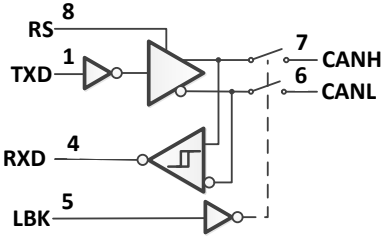
- 3 Options
  - UT64CAN3330
    - Sleep Mode



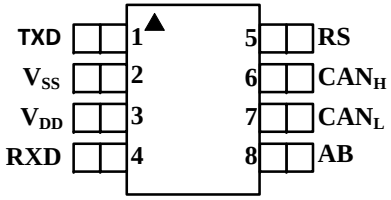


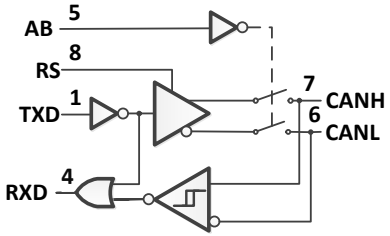
  - UT64CAN3331
    - Diagnostic Loopback





  - UT64CAN3332
    - Auto baud Loopback



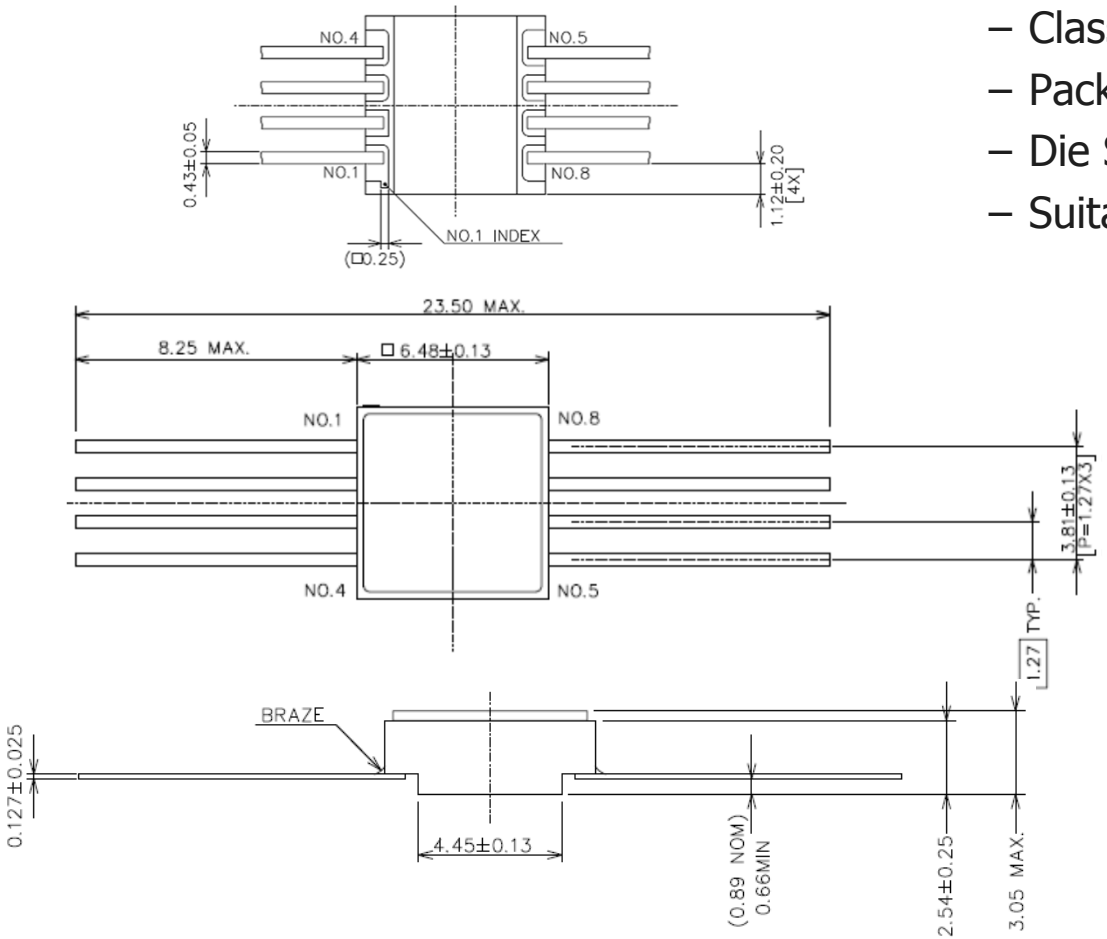


- Key Specifications and Features:
  - Max Power: <200mW
  - Digital I/O: 3V (5V tolerant)
  - Baud Rate: 10Kbps to 8Mbps
  - Supply Voltage: Single 3V
  - Bus Fault Protection: ±16V
  - Common Mode Range: {-7, 12}
  - Bus Transient Protection: {-60V, +40V}
  - Differential Input Impedance: 40KΩ
  - Differential Input Capacitance: 15pF
  - Worst Case Loop Propagation Delay: 100ns
  - CAN Bus Output Drive: Up to 100mA
  - Compliant with ISO 11898-2
  - TID: 100 krad(Si)
  - SEL: ≤100 MeV-cm^2/mg
  - SEU immune
  - QML Q and V Pending

Introduction to Cobham CAN Transceivers

UT64CAN333x

- Packaging: 8-lead ceramic flat pack



- Key Specifications and Features:
  - Cold Spare of digital I/O
  - Class 3B ESD for CAN bus pins (8000V)
  - Packaging: 8-lead ceramic flat pack
  - Die Sales to be supported
  - Suitable replacement for RS-485

UT64CAN333x Value Proposition

Summary

- Technology info – Base technology (0.35µm mixed signal) is QMLV qualified with several parts in production
  - Additional qualification required for high voltage elements
  - Qual plan under internal TRB review
- Our advantages
  - Guaranteed radiation performance (100krad, 100 MeV-cm^2/mg)
  - Product offering through the SMD (QML-Q, QML-V)
  - Compatible with ISO 11898-2 (1Mbps) and 11898-5 (CAN-FD, 8Mbps) operations
  - Comparable performance and features to commercial products
  - Provides debugging capabilities with a small footprint

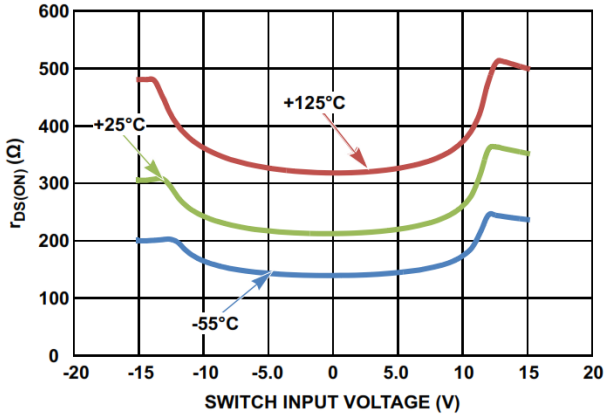
Controller Area Network Milestone Schedule

Milestone	Status	Plan	ECD	Comment
Tape Out	Complete	4QCY14	January 2015	
Wafer Fabrication	Complete	1QCY15	March 2015	
Engineering Samples for Launch Customers	Complete	1QCY15	May 2015	Available
Characterization	Complete	1QCY15	2QCY15	
Proto-OOE Assembly	**Complete**	**1QCY15**	**3QCY15**	**09-24-15**
Qualification Start	In progress	2QCY15	3QCY15	On schedule
Qualification QML-Q	Pending	1QCY16	4QCY15	On schedule
Qualification QML-V	Pending	1QCY16	3QCY16 - July	On schedule

ISL71840/1 (Next Gen 1840) MUX w/Cold Spare

/PROTO available NOW
DLA Release = Q4/15

- **Features**
  - –Abs Max Supply: +/-20V
  - –Operating Power Supply Range: +/-10.8V to +/-16.5V
  - –Cold Sparing: +/- 25V
  - –Overvoltage Protection: +/- 35V
  - –Overvoltage Safety Feature: Disable Individual Input in OV Condition
  - –Ultra Low R_{ON} < 500Ω (typ): rail-to-rail
  - –500ns Propagation Delay
  - –Low 100nA Leakage
  - –ESD: HBM 8kV
  - –Radiation Tolerance
    - •High Dose = 100krad(Si), Low Dose = 50krad(S
    - •SEL/B Immune up to 86MeV
  - –32 Channels = 48ld Quad Flatpack (14mm x 14mm) /
  - –16 Channels = 28ld Flatpack (18.8mm x 14mm), P-t-P with HS-1840RH



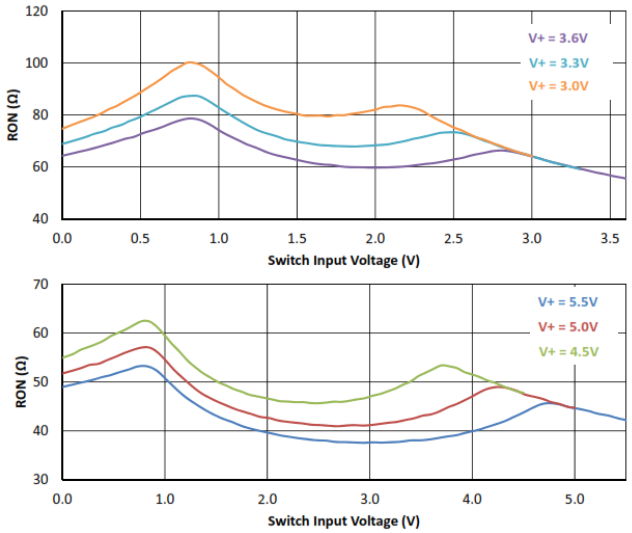
ISL71840SEH vs HS-1840RH

- **Spec Changes**
  - –ISL71840SEH has rail-rail operation with much lower RON across the board.
    - •If a customer had some in-line resistors for current protection, then the lower RON of the new switch may affect that protection.
  - –In an input overvoltage condition the ISL71840SEH shuts off the switch, whereas the HS-1840RH would just clamp the voltage.
    - •Reduce power loss and limit the shutdown to that one switch instead of the whole IC.
  - –The ISL71840SEH offer lower leakage currents and path is to GND
  - –Faster propagation and timing delays
- **New Features**
  - –The ISL71840SEH has triple redundant decoders that provides much better SET performance compared to the HS-1840SEH

ISL71830/1 16/32CH 5V MUX w/Cold Spare

/PROTO Available Now
DLA Release = Q4/15

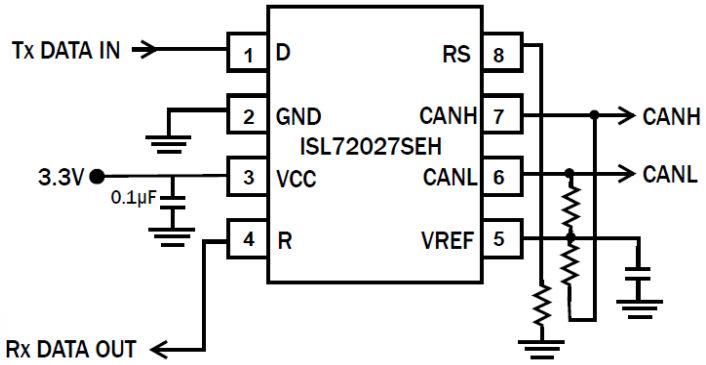
- **Features**
  - –Abs Max Supply: 6.9V
  - –Operating Power Supply Range: 3.0V – 5.5V (single supply)
  - –Cold Sparing On or Off up to 7.0V Abs Max
  - –R_{ON} < 100Ω: rail-to-rail
  - –Under/Overvoltage Protection: -1.5V to 7.0V
  - –Break-Before-Make Delay
  - –Propagation Delay: 40ns (typ)
  - –Leakage: 30nA worst case without OVP
  - –ESD: HBM 5kV
  - –Radiation Tolerance
    - •Low Dose = 75krad(Si)
    - •SEL/B Immune up to 60MeV
  - –32 channels = 48ld Ceramic Quad Flatpack (14mm x 14
  - –16 channels = 28ld Flatpack (18.8mm x 14mm)



ISL72026/7/8SEH 3.3V CAN Bus Transceiver

•Features

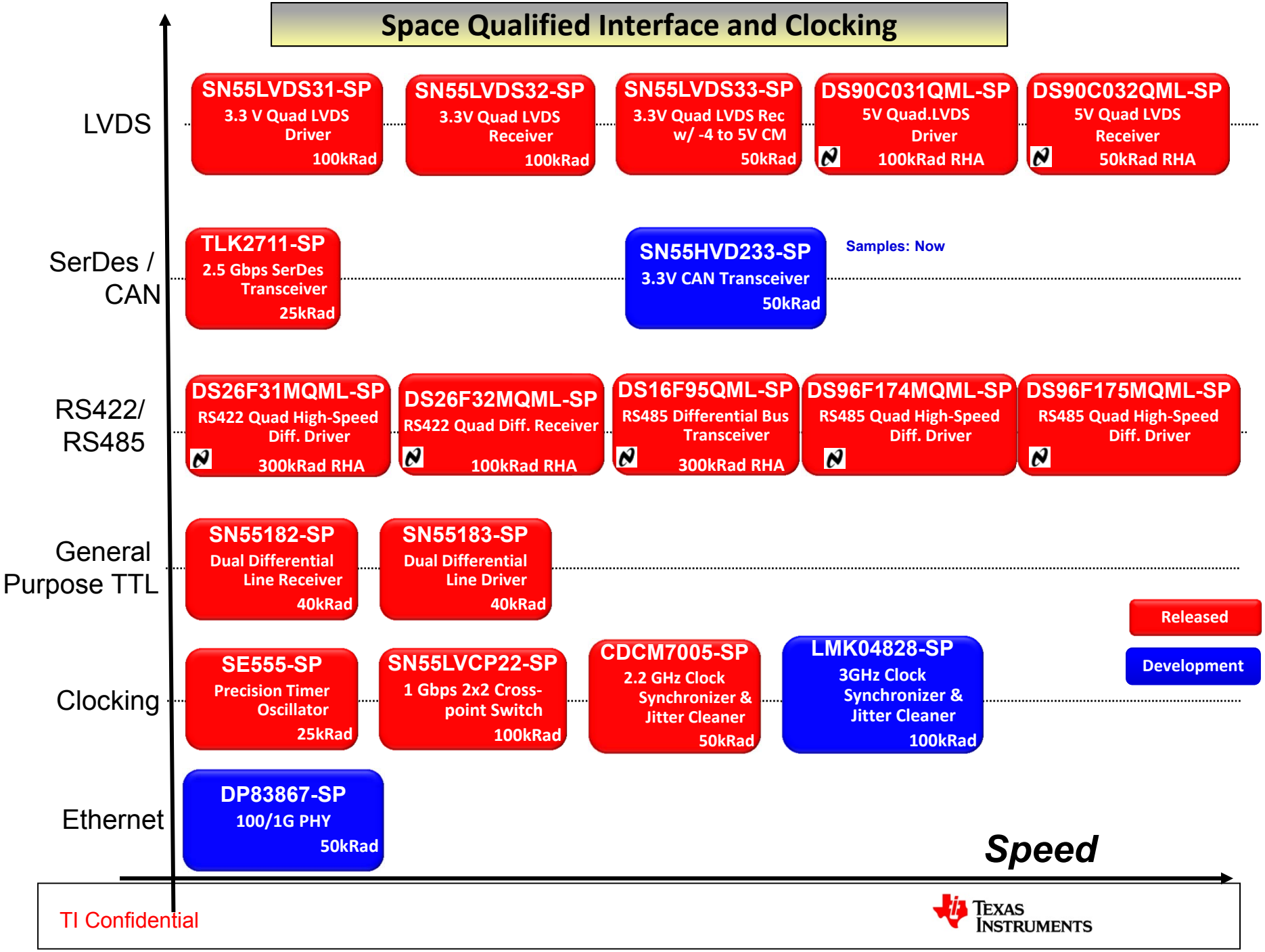
- –Operating Supply Range….3V to 3.6V
- –Compatible to ISO 11898-2
- –4kV HBM ESD
- –Bus fault protection…+/-20V (Not under beam)
- –Cold Spare capability ideal for N+1 applications
- –Three selectable driver rise/fall time
  - •Data Rates: >1Mbps, 500kbps, <250kbps
- –Current fold-back fault OC protection
- –Common Mode range ……. -7V to +12V
- –Available Modes:
  - •ISL72026SEH: Listen Mode and Loopback
  - •ISL72027SEH: Listen Mode and Split Termination Output
  - •ISL72028SEH: Low Power Shutdown and Split Termination Output
- –Shutdown/Listen mode/Operating currents ……. 24µA/2mA/6mA
- –SEE immune to LET 86MeV
- –High/Low dose rate guaranteed…..100krad/50krad



Samples= Now
DLA Release=Q4/15

intersil

Space Qualified Interface and Clocking



Texas Instruments

SN55HVD233-SP

+3.3V CAN Transceiver

Features

- Bus pin short-circuit protection to **±36V**
- ESD protection exceed **16kV**
- Designed for signaling rates up to **1 Mbps**
- High Impedance
- 3.3 V supply
- Glitch free power up & power down protection
- -55° to +125°C
- 10 Pin CFP (HKU)

Benefits

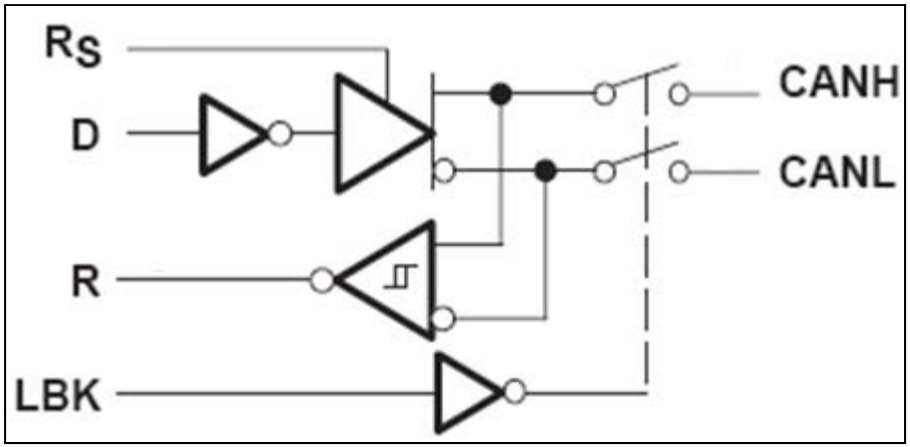
- Device is unharmed by shorts to these voltages
- Compatibility with existing signaling schemes
- Up to 120 nodes on bus
  - Drastic improvement in integration time at satellite integrator
- Ideal for microcontrollers and DSPs
- Hot pluggable without data corruption
- Loopback for Diagnostic Functions Available
- Highly reliable communication link
- Very low power standby mode
- No 5V power requirement in system

Applications

- Satellite Backplane Communication
- CAN Data Bus

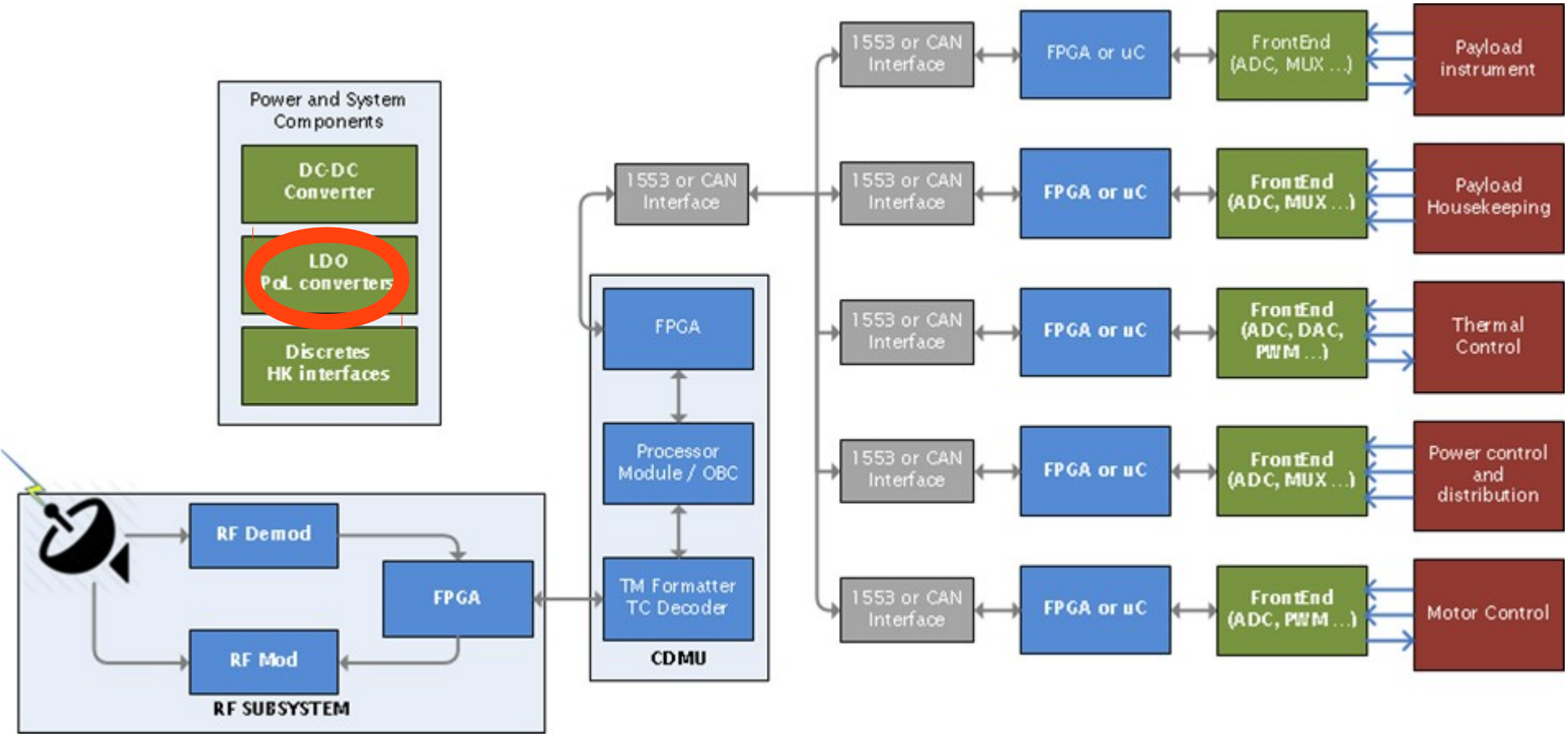
Rad Performance

- TID = 50kRad(Si)
- SEL Immune to LET = 60MeV @ 125°C



Functional Block Diagram

Building block MAP of RTUs functions

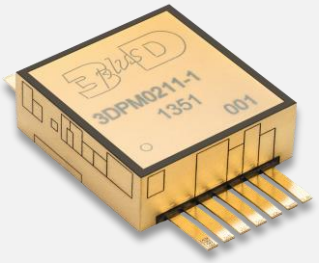


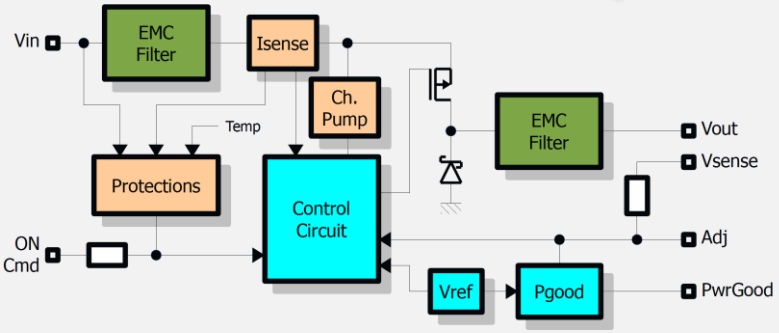
EU Point of Load converters developments

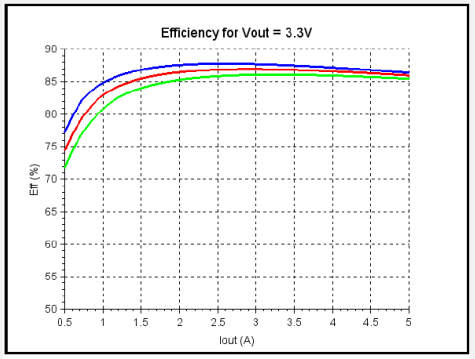
1. 3D-Plus (F), 3DPM0211
2. ÅAC Microtec (S), uPoL
3. Space-IC (D), SPPL12420RH
4. STM (I, F), RHFPOLS01

3DPM0211 - PoL 10% - Main Features

- ✓ Input Voltage: 5V ± 10%
- ✓ Adjustable Output Voltage: 1.25 to 3.8V ; Iout < 5 A
- ✓ **Efficiency: 88 %** (3.3V/3A)
- ✓ Fast transient response under load change (di/dt=10A/µs)
- ✓ Fixed switching frequency
- ✓ Integrated input and output EMC filters
- ✓ **Fully Protected**:
  - Input UVD
  - Output Over-Current
  - Internal Temperature
- ✓ Automatic restart in case of overload
- ✓ Soft Start, ON/OFF Command, Power Good signal
- ✓ Enhanced ESD protection
- ✓ Radiation Hardened by design
- ✓ SOP-14 (26.5 mm x 25mm x 10mm & 15 g)







Efficiency @ 3.3V for Vin = 4.5V (blue), Vin = 5V (red), Vin = 5.5V (green)

3DPM0211 - PoL 10% - Protections

Overload:

- ✓ Iout >6A ➔ PoL switched OFF (200µs)
- ✓ Automatic restarts (every 3ms)

Input Under-Voltage:

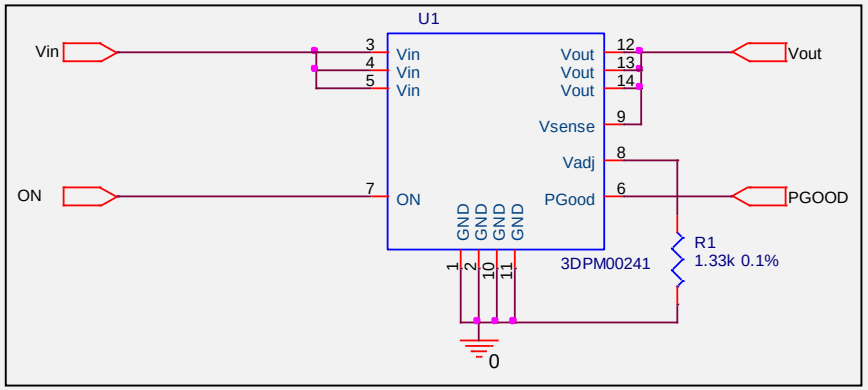
- ✓ Vin < 4.2V ➔ PoL switched OFF

Internal Over-Temperature:

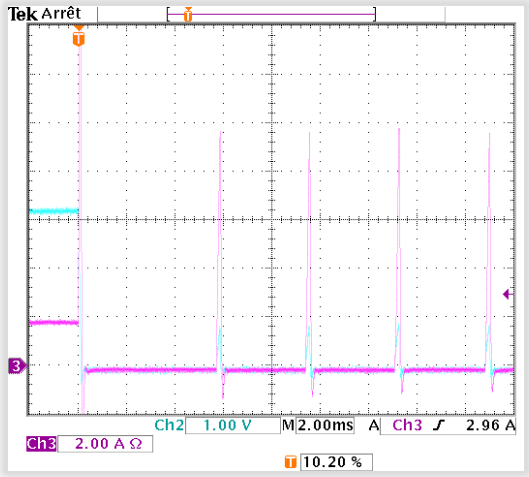
- ✓ T > 125°C ➔ PoL switched OFF

Radiation Tolerance:

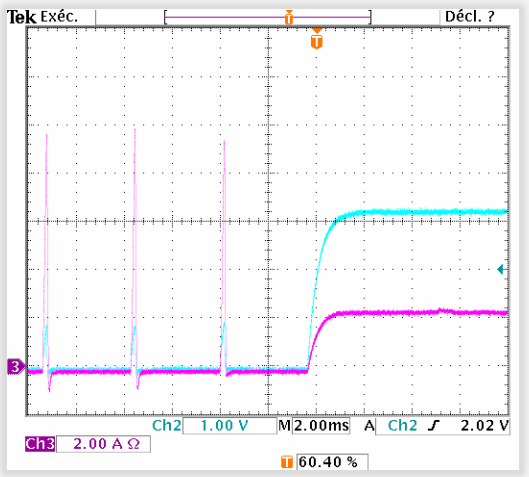
- ✓ SEL/SEGR tests (each basic device):
  LET Threshold 80 MeV.cm²/mg
- ✓ SET test:
  LET Threshold 80 MeV.cm²/mg
- ✓ TID tests (each basic device):
  50 Krad(Si)



Typical Application's schematic with 3D PLUS POL Converter



PoL – Overload condition detected
CH2 = Vout, CH3 = Iout



PoL restart - Short circuit removed
CH2 = Vout, CH3 = Iout

µPOL

Technical characteristics:

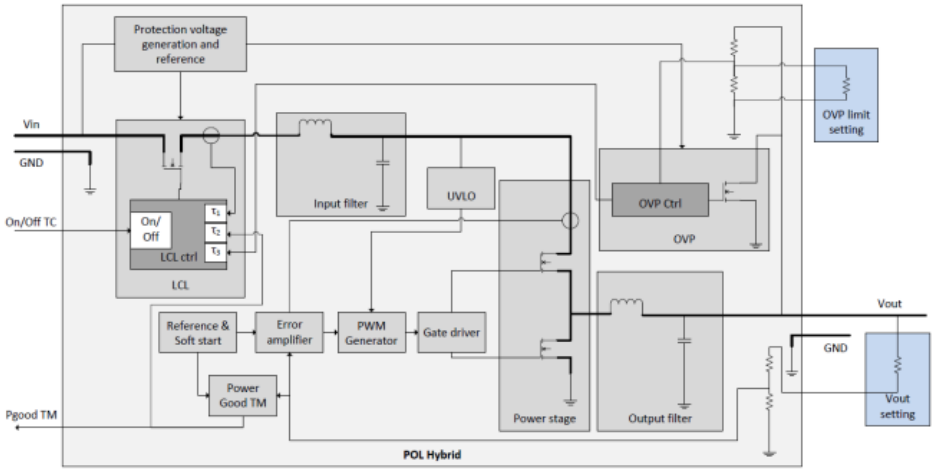
- Synchronous rectification buck converter

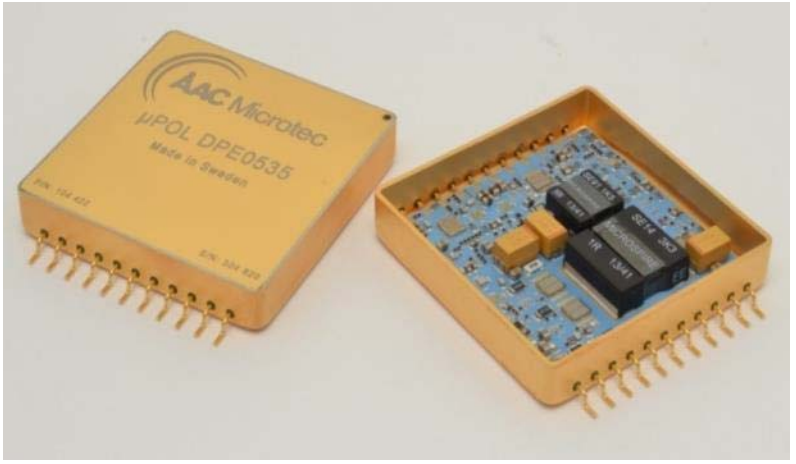
- 4.8 – 6.2V input voltage
- 1.2 – 3.5V output voltage
- 3.5A output current
- 50x50mm SMD package
- -40°C to +80°C Operation

- Integrated input filter and output inductor/capacitor
- Integrated LCL on input
- Integrated OVP on output

- Up to 86% efficiency, including protection and filter losses.

- Short circuit protected
- On/Off Control / Power good telemetry

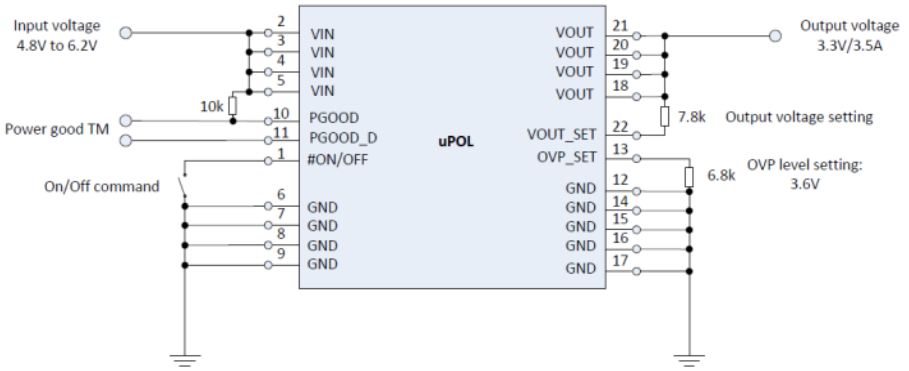




µPOL

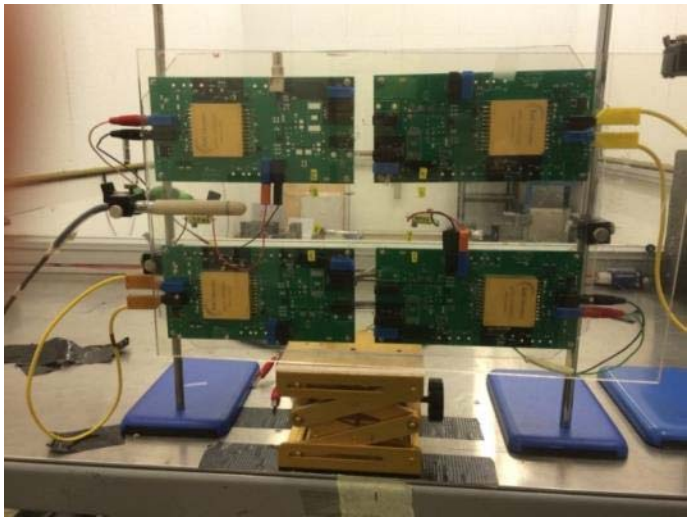
Key features:

- Only two external resistors needed to create a fully protected low voltage rail with filtered input current.
- ITAR Free



Current status:

- Radiation tested to 45kRad with no noticeable parameter drifts.
- Preliminary life tests (500h, >125°C) have been performed with no failures or parameter drifts.
- Different qualification options are currently being investigated.

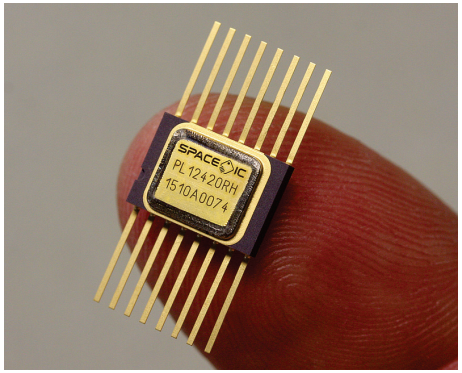


POL Converter

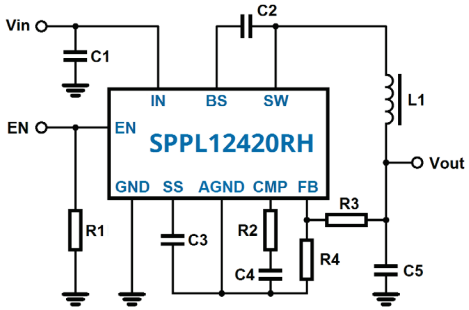
ESA SME
Innovation Award 2014

Features

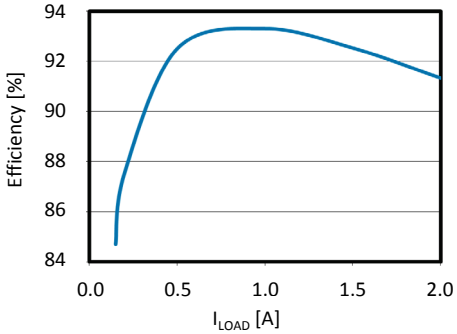
- Ceramic hermetic flatpack package
- Latch-up immune SOI technology
- 2A continuous output load current
- 4.5V to 24V input voltage
- 0.923V to 21V output voltage
- >90% efficiency
- 340kHz fixed switching frequency
- ESD rating 4kV (HBM)
- -55°C to +125°C extended temperature range (target)



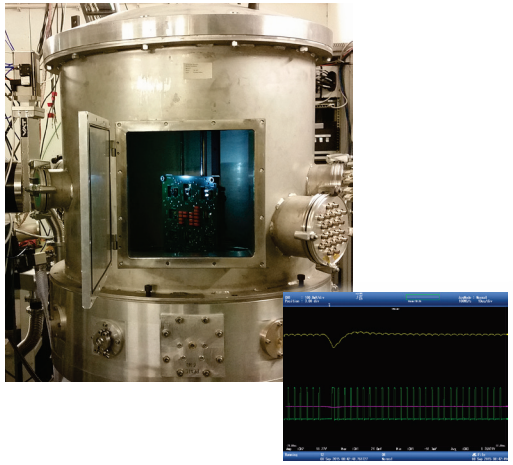
Application



- High-Density Point-of-Load Regulators
- Distributed Power Systems
- High-Voltage Power Rail Architecture
- Satellite Systems
- Launch Vehicles



Rad Hardness



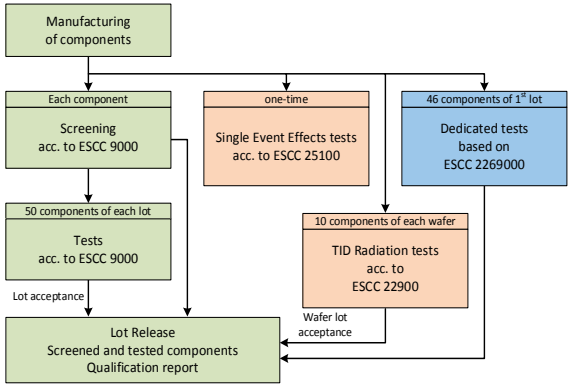
- TID > 100 krad (Si) - unbiased
- TID > 40 krad (Si) - biased
- SEL immune due to full isolated SOI technology
- Free from any SEE-fails at:
  - $V_{IN} \leq 11V$, LET ≤ 85 MeV·cm²/mg
  - $V_{IN} \leq 13V$, LET ≤ 60 MeV·cm²/mg
- SET-free at LET ≤ 35 MeV·cm²/mg
- No critical SETs at LET > 35 MeV·cm²/mg

POL Converter

ESA SME
Innovation Award 2014

Quality

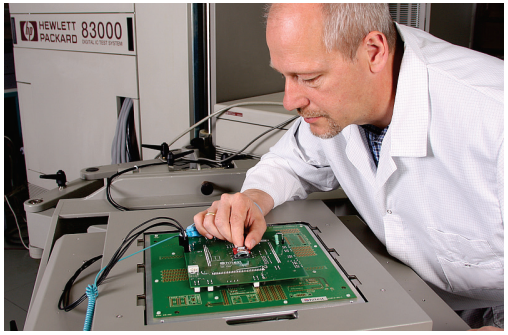
- Screening according to ESCC9000
- Lot acceptance testing according to ESCC9000
- Radiation testing according to ESCC22900 and ESCC25100
- Dedicated tests according to ESCC2269000



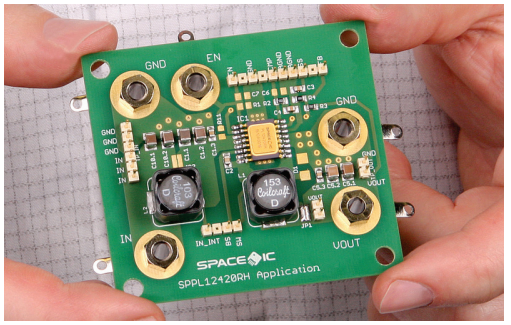
Status

- IC development _____ complete ✓
- Hermetic power flatpack ___ complete ✓
- TID evaluation testing _____ complete ✓
- SEE evaluation testing _____ complete ✓
- Lot screening _____ complete ✓
- Lot qualification testing ____ ongoing ⏳

- About to apply for EPPL listing
- Follow-up ESCC certification intended



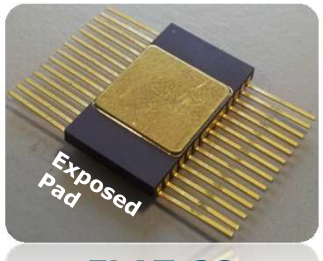
Availability



- Now available:
  - Engineering Models
  - Qualification Models
  - Evaluation Kits
- ~ Dec 2015:
  - Expected release of Flight Models production lot

RHFPOLS01 – Rad-Hard Switching regulator

MAIN FEATURES



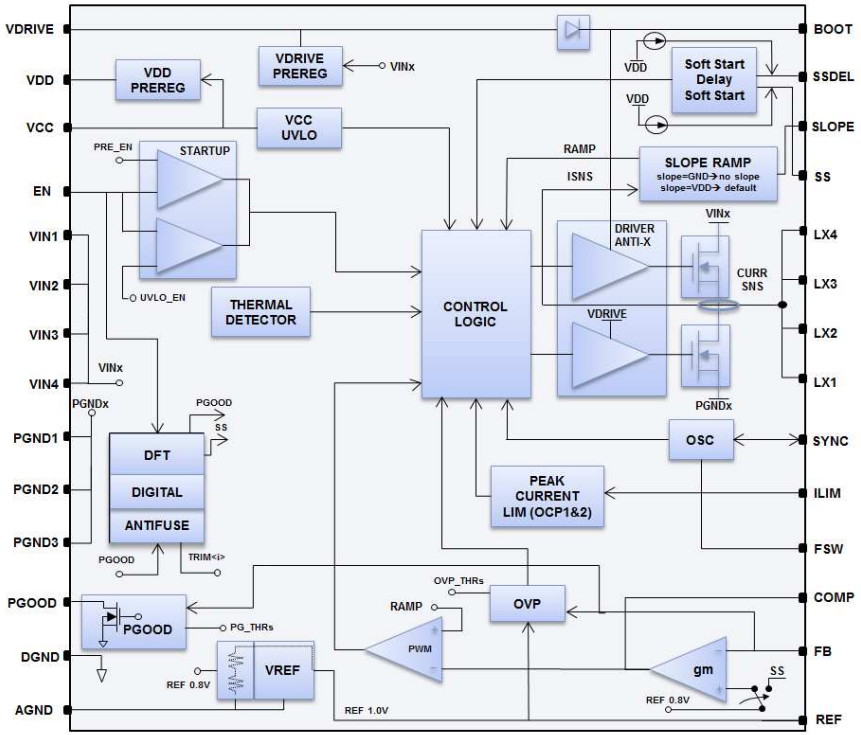
FLAT-28

- 3.0V to 12V input operating voltage range
- 0.8V to 0.85*V_{IN} Output voltage range
- ±1% accuracy 1.0V internal reference
- Up to 7A Output current for T_J<+150° C
- Current sharing configuration for higher load requirements
  - ✓ 14A using Current Sharing with 2 Parts
- Operating temperature range -55° C to +125° C
- Integrated NCH MOSFETs for synchronous step-down conversion
- Integrated BOOT diode
- Efficiency up to 95% (Optimized for V_{IN}=5V & I_{OUT} =2÷4A)
- Programmable switching frequency from 100kHz to 1MHz
- Fast load transient response and simple loop compensation based on PCM control
- Easy synchronization with 180° out-of-phase (up to 2 ICs) management
- Lossless current sensing based on sense-FET
- Not-latched adjustable output over voltage protection
- Adjustable Dual Threshold output overcurrent protection (semi latched **(*)** HICCUP implementation)
- Fully Configurable Soft Start
- Semi-latched **(*)** over temperature protection (155° C, 20° C hysteresis)
- Power good Flag output pin (±10%)
- Loop compensation Access for easy stabilization
- RH_OTP (One Time Programmable) circuit embedded for Rum Trimming
- FLAT28Power Hermetic ceramic package with connected lid

(*) Semi-latched means that the alarm is latched after a certain number of events.

BLOCK DIAGRAM

Design In Progress



SHORT DESCRIPTION

The RHFPOLS01 is a single phase, step-down monolithic switching regulator with high precision internal voltage reference and integrated power MOSFETs for synchronous conversion.
The regulator converts 3.0V~12V input voltage to 0.8V~0.85*V_{IN} output voltage. It has been designed to supply FPGA, DSP, MCU and ASICS in general for space application or other harsh environment application.

The controller is based on peak current mode architecture which ensures a fast load transient response and very stable switching frequency.

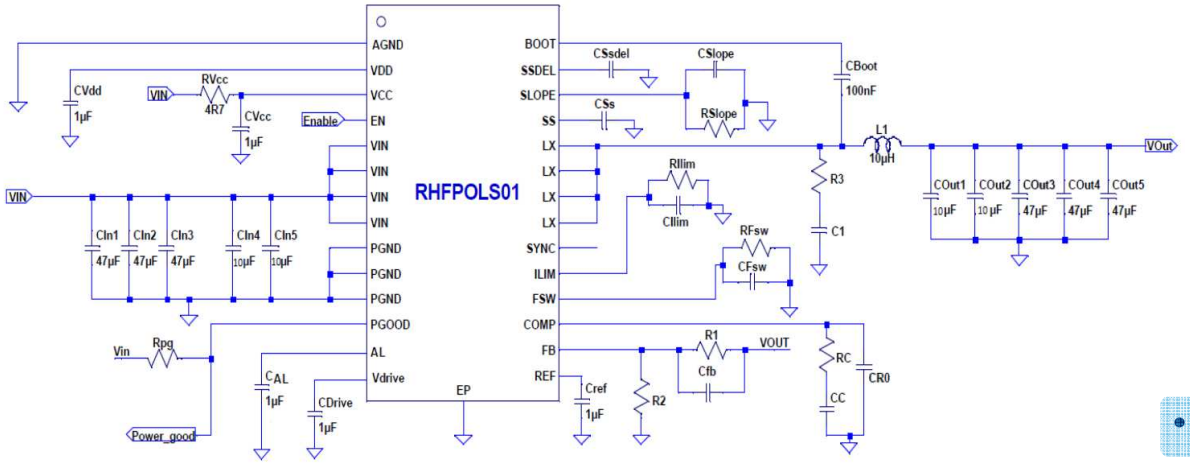
life.augmented

- **In development under ESA Contract**

RHFPOLS01 – Rad-Hard Switching regulator

Design In Progress

TYPICAL APPLICATION CIRCUIT

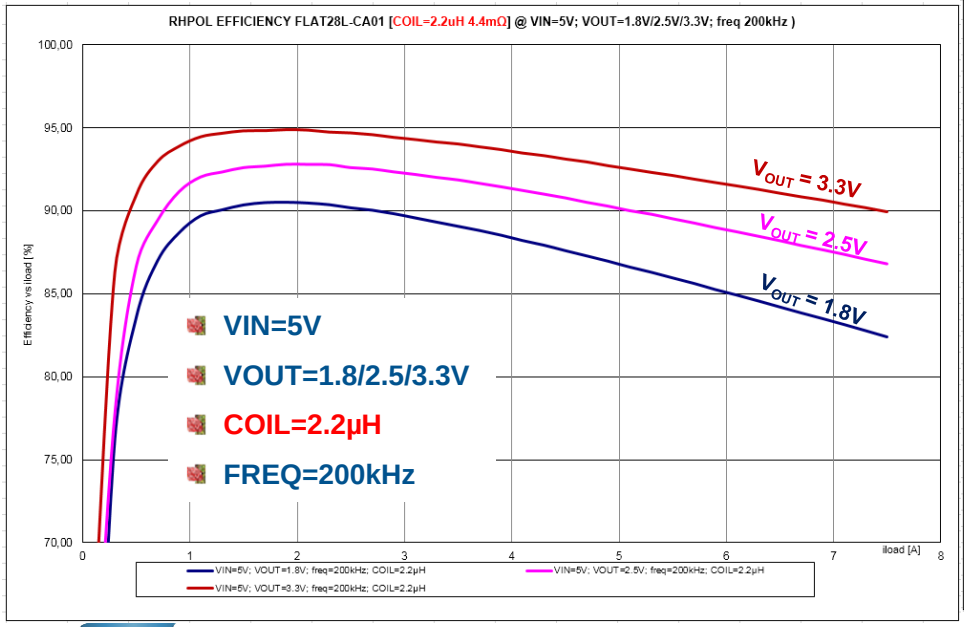


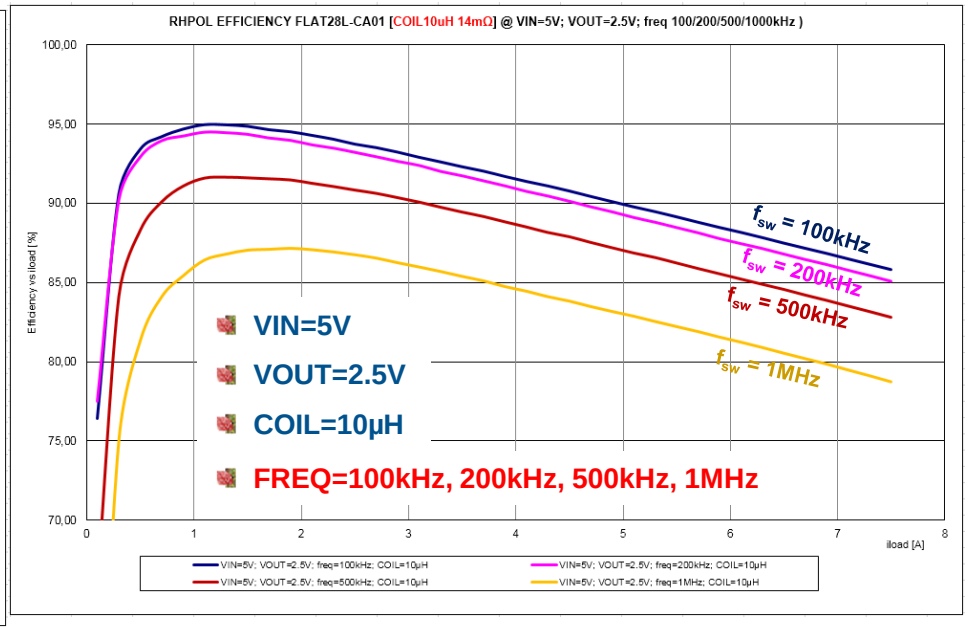
External Components
- Few Only
- Space Version Available

RADIATION TARGETS
- ELDRS free, 100krad (Si) total dose
- SEE free at 60MeV/mg/cm2
- SET Characterization

APPLICATIONS
- Point of Load Regulation for Space Application
- FPGA, DSP, CPU and ASICs Supply
- Low Voltage, High Density Distributed Power System

- **In development under ESA Contract**





life.augmented