Research & Technology activities in on-board data processing domain

ADCSS 2015 – Avionics Technology Trends Workshop
ESA/ESTEC in Noordwijk, The Netherlands
October 21st 2015

Olivier Notebaert
Airbus Defence and Space
Space Systems – Orbital Functional Avionics – On board processing and S/W (TSOEF2)
Toulouse Office Z#606 - olivier.notebaert@airbus.com

AIRBUS DEFENCE & SPACE

Spacecraft systems

Satellites

- Earth Observation
- Science
- Telecommunications
- Navigation

Space exploration

- Cruise vehicles
- Specific manoeuvers
- Surface exploration (rovers)

Space Transportation

- Orbit service vehicles
- Manned Flight
- Launchers

Philae

Various space systems

Common technology solutions

Outline

Introduction

State of the art space processing technologies

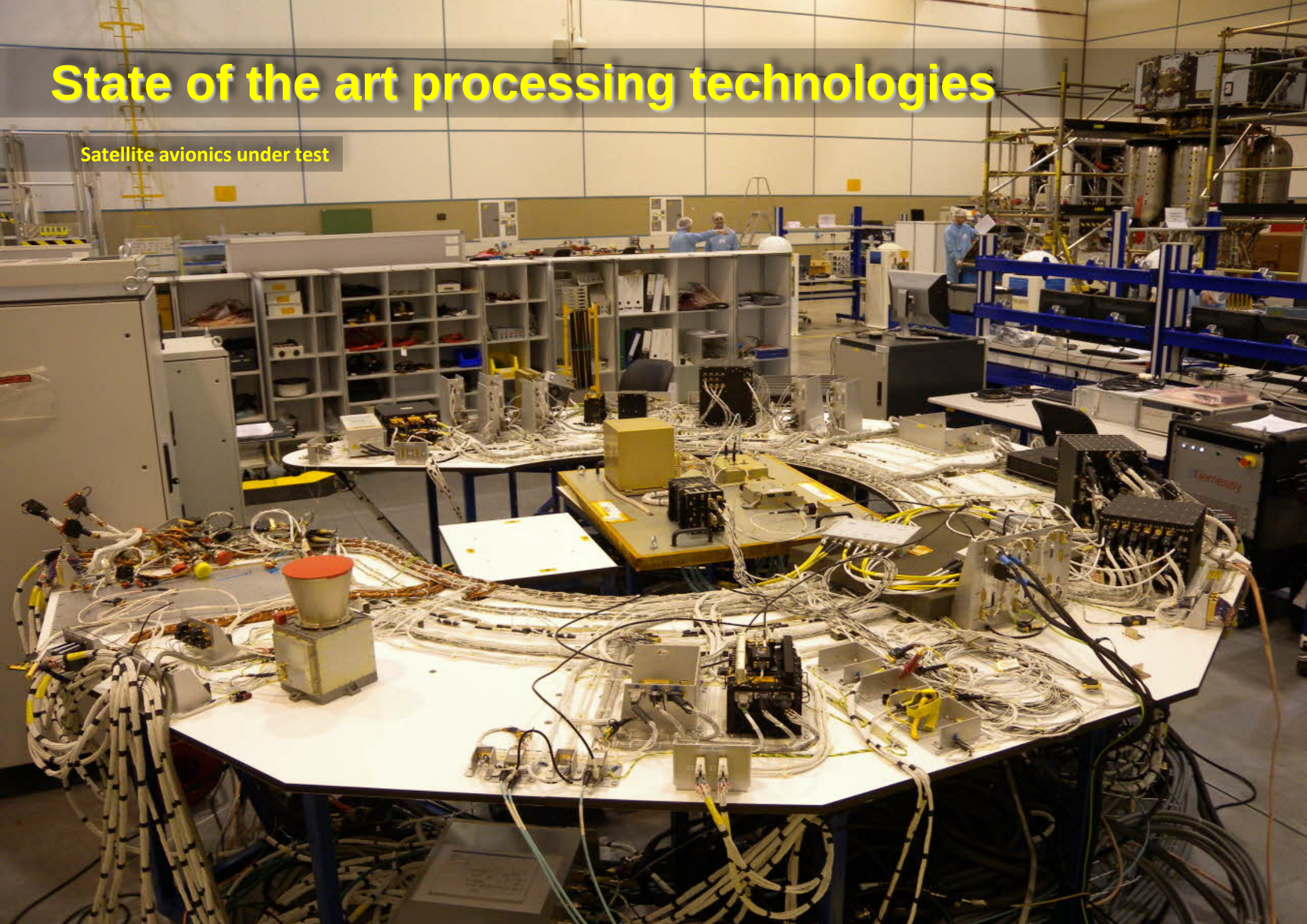
Space systems on-board processing technologies

Future needs and technology development strategy

On-board processing technology trends

Main research targets for Airbus Defence and Space

State of the art processing technologies



Satellite avionics under test

State of the art processing technologies

On-board Processors

Mil-Std-1750

- Mil-STD-1750A standard architecture, many implementations
- 16 bits, typically 1 Mips @ 25 MHz
- Missions: ISS ATV, Envisat, Rosetta, LansSat…
- 3-1750 recent implementation still in use on Eurostar 3000 telecom satellites

OBSOLETE

© Airbus Defence and Space

Eurostar 3000 SCU
(3-1750 processor)

ERC-32

- Sparc V7, 32 bits, typically 20 Mips @ 25 MHz (0,5µm)
- Missions: ISS ATV, Ariane 5, Vega Pleiades, HerschelSar, Herschel, Gaia, Galileo

OBSOLETE

© RUAG Space

Vega On-Board Computer
(ERC-32 processor)

LEON 2 and LEON 3

- Sparc V8, 32 bits, 80 Mips @ 100 MHz (0,18nm)
- Spacecraft Controller on a Chip
  - Leon 2 or Leon3
  - Specialised functions such as TM/TC, Reconfiguration, Modem
  - Space standard I/O's: for 1553, SpaceWire, Can Bus
- Selected on almost all new Spacecraft

© Airbus Defence and Space

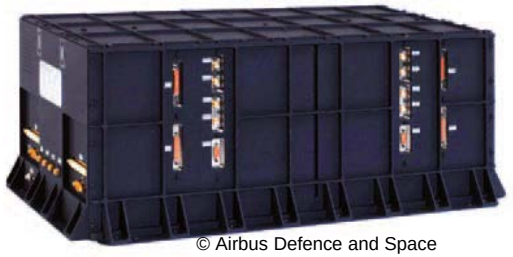
OSCAR Computer
(LEON-3 processor)

State of the Art

Key data processing components

Memories

- Commercial grade components with ECC's (EDAC or Reed Solomon)
- SDRAM or non volatile FLASH memory components



© Airbus Defence and Space

Solid State Recorder
Flash memory technology

FPGA (*)

- Rad hard components
  - ACTEL RTAX (anti-fused technology: programmable only once)
- Rad tolerant components
  - Use in the short term future of reprogrammable devices (SRAM based) such as RTG4 from MicroSemi

ASIC (**)

- Space components developed in rad-hard technologies:
  - Standard products: Spacecraft Controller on a Chip, I/O devices, memory control, Compression, FFT, GNSS processing,…
  - Specialized functions when processing performance cannot be reached through reprogrammable devices (e.g. Telecom P/L)
- Rad-Hard libraries derived from commercial technologies :
  - 180nm from ATMEL
  - Aeroflex 90 nm
  - STM 65 nm after 2016 (Commercial technology: 14nm)

© Airbus Defence and Space

CORECI recorder
Image compression, cyphering and storage

(*) Field-Programmable Gate Array
(**) Application Specific Integrated Circuits

State of the art

Buses and Networks technologies

Field bus or direct connections to many sensors and actuators

- Typical bandwidth: 10 to 100 Kbps
- Connections to local Remote Terminals or directly to on-board computer

► CAN bus, RS422, analogues

Spacecraft control bus

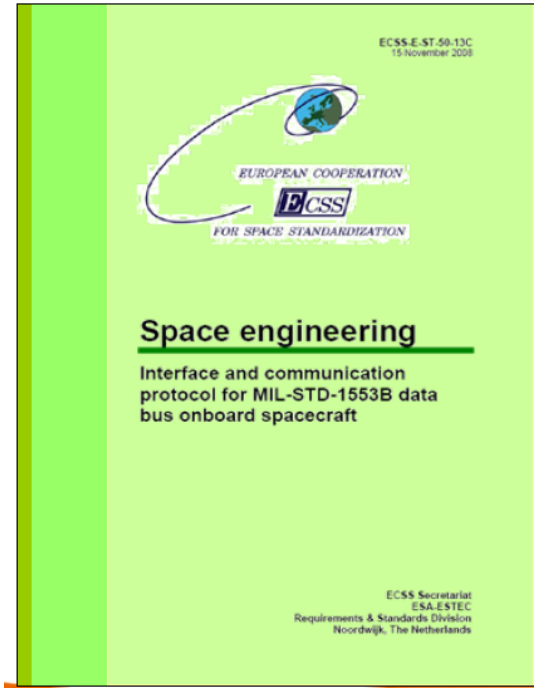
- Main data link between the on-board functional sub-systems
  – On Board Computers, remote terminals, sensors and actuators
- Key properties: reliability, real-time & dependability
- Typical data rate: 0,1 to 1 Mbps

► Mil-Std-1553B

Payload data network

- For instruments data processing and storage
- Key properties: reliability & performance for data throughput
- Typical data rate: 10 Mbps to 1 Gbps
- Direct links or network topology

► SpaceWire



ECSS (European Cooperation for Space Standardisation)
⇨ European technology interoperability and harmonisation
⇨ SpaceWire, MIL-STD-1553 and CAN bus

Space systems on-board processing technologies

Future needs and technology development strategy

On-board processing technology trends

Main research targets for Airbus Defence and Space

Philae landing on the comet

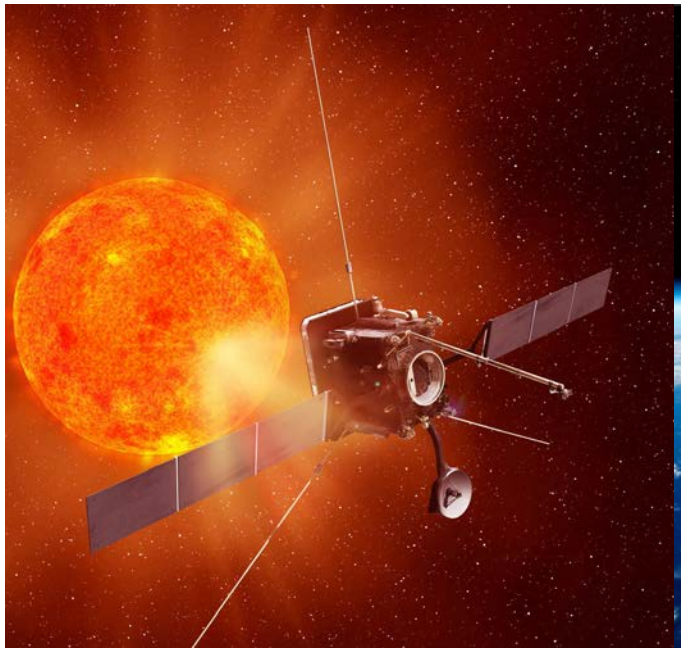
Future missions

In development

- Space science and exploration program – Bepi-Colombo, Solo, Euclid, Juice…
- Metop-SG
- Next generation telecom
- Ariane 6
- Human Flight: ORION
- Large constellations (OneWeb)

Longer term

- Machine to Machine services
- Multi-service payloads
- Highly flexible and autonomous systems
- Space exploration robotic systems
- Vision based navigation
- Reusable launchers
- Space plane
- …



Future Needs

Challenging requirements…

- New on-board functions, autonomy and flexibility
- Missions with high availability requirements
- High data throughput increasing with instruments technology
- Payload with many instruments…

➲ Rapidly growing on-board data processing performance requirements

Constraints

- Ground space communications limited bandwidth
- Limited power, volume & mass
- Harsh environment (mechanical, thermal, radiations…)

➲ Cost and competitiveness

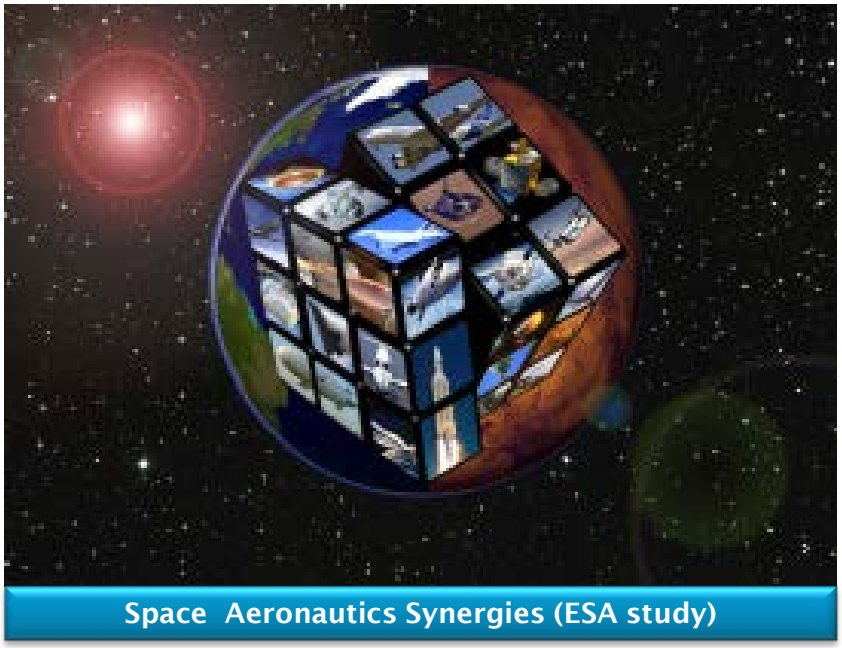
Context

- Increasing technology gap between space and ground electronics
- Limited choice of space-grade components
- Space is a niche market (business model)

➲ Limited Budget for technology development

Space technology development strategy

- **Fill the technology gap without re-inventing the wheel for space**
  - Synergies between Space, Aeronautics and other domains
  - Enable use of commercial electronics (COTS)



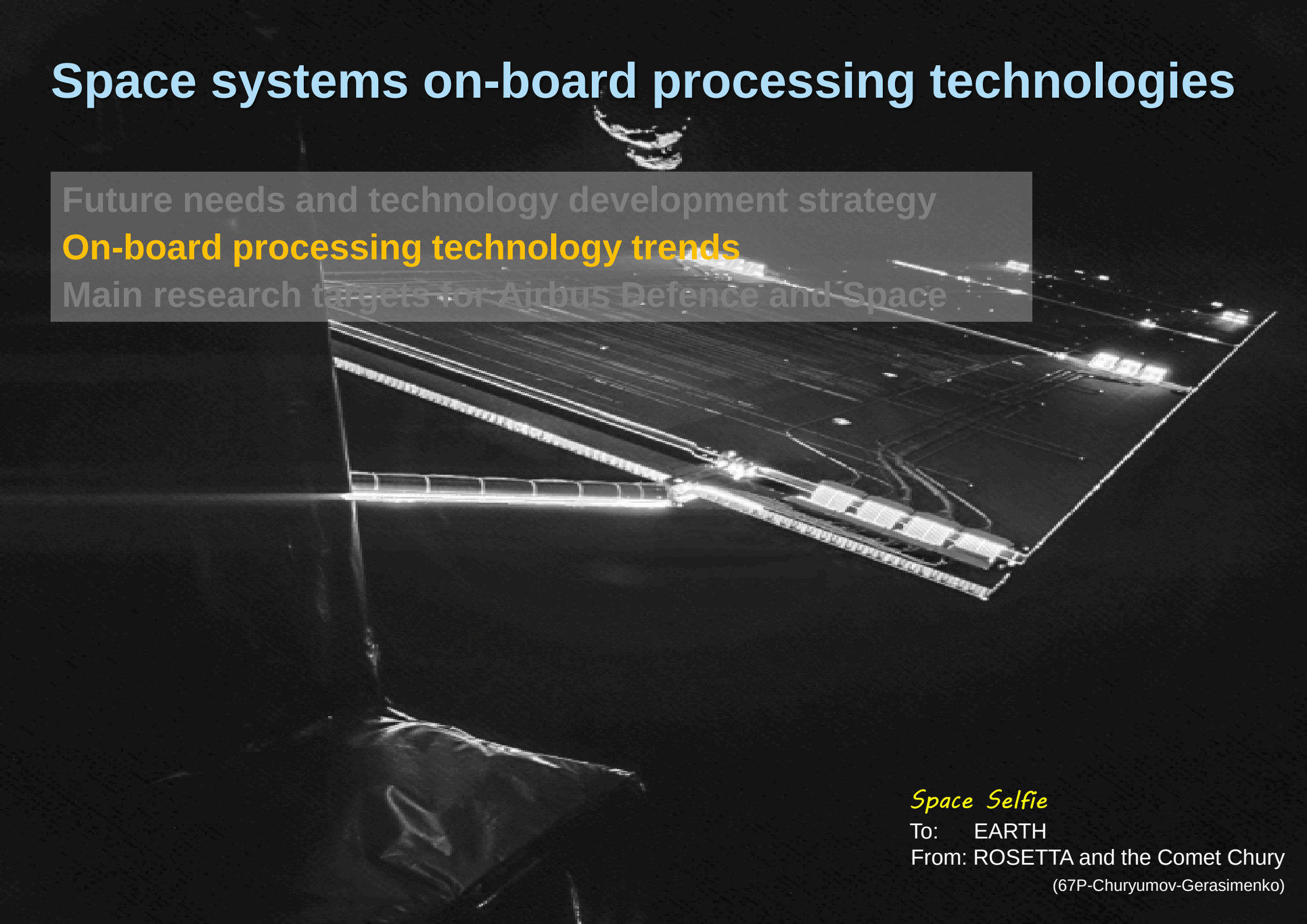
- **Technology developments focus on competitiveness and Non dependancy**

Space systems on-board processing technologies

Future needs and technology development strategy

On-board processing technology trends

Main research targets for Airbus Defence and Space



Space Selfie

To: EARTH

From: ROSETTA and the Comet Chury

(67P-Churyumov-Gerasimenko)

On-board processing technology trends

On-board processing technology

Miniaturisation Low Power Flexibility Performance Availability Image processing SW radio Obsolescence Signal processing FDIR Reprogrammable FPGA's Rad-hard ASICs NGDSP Many Cores HPDP NoC's Robotics Autonomy AOCS/GNC Integrity Determinism Reliability Safety Security FD-SOI 28 nm 65 nm DARE 180 nm 90 nm DSP GPP HiP-CBC BRAVE SPINAS ARM4Space AvionicX Networks I/O's Optical links MISSION NGMP ASCOT OSRA SpW AOCS SOIS studies OBC-SA KARS N-MaSS IMA4Space UWB4Space MOST PROXIMA SpCKeT Multicore Dual Core Quad Core SoC's LEON ARM PowerPC P4080 GR720 SCoC 3 Zynq DSP 6727 Maxwell PPC 750 GR740 MDPA (NGMP) Atom RTG4 Virtex Spartan Interoperability Data buses CAN bus HSSL 1553 Sensor Networks Wireless Routing Switches SpaceWire SpW-D SpW-RT RMAP Gateways AFDX SpaceFibre Ethernet AVB TTE SRIO cPCI serial ECSS Execution Platform TSP PikeOS RTEMS Separation Kernel AADL Seamless design flow Codesign SystemC Co-Simulation Modelling Methodology COTS SmartIO Components Radiations Mitigation techniques Latch-up SEU Total Dose SysML Process Testability Validation Qualification Debug Observability Tools Configuration Integration Framework Co-engineering Autocoding Formal methods TASTE AMP SMP S/W Parallelism WCET AIR Standardisation IMA Middleware Xtratum Interfaces Harmonization SAVOIR Architecture CCSDS SOIS FMS PnP COST Verification Certification OSRA Building Blocks OSRA-P PUS MO Investment Recurring Cost ROI NRC Regulations ITAR Export Control NDA's Contracts SAFI CFDP IPR Geo Return Business Model Quality EGSE

ARM Processor

ARM processor

- Could be a basis for a next generation processor
- Efficient architecture
- Low Power consumption

AvionicX project (CNES)

- ARM based breadboard computer with TTE interfaces
- Evaluation on launcher and satellite use cases

ARM4Space project (H2020)

- Rad-Tolerant ARM based architecture for space use

ASCOT project (CNES)

- Definition of a next generation Spacecraft controller on a chip based on ARM Cortex
  - All embedded spacecraft control function as current SCoC
  - High Speed interfaces
  - New embedded processing functions (e.g. GNSS)

ARM is selected for Ariane 6 on-board computer

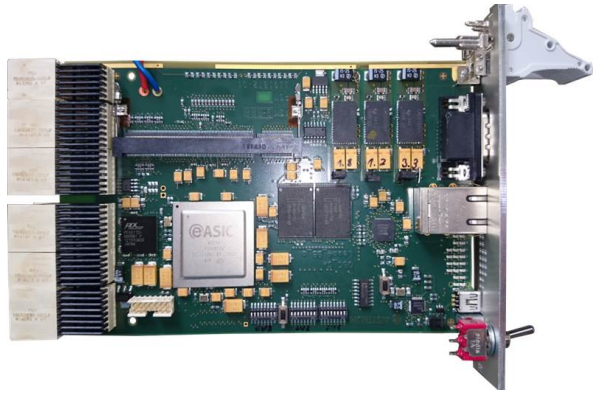
Candidate for OneWeb constellation

The AvionicX Breadboard with embedded ARM Cortex 5

Software on Multicore processors

Multicore is a good way to go for increased general purpose processing performance while keeping power and thermal dissipation in check

- LEON based multicore processors for space are available
  - GR712 available (dual core processor)
  - GR740 (quad Core SoC) Rad-hard EM prototypes available in Q1/2016)
- Almost all COTS high performance processing devices now include several cores



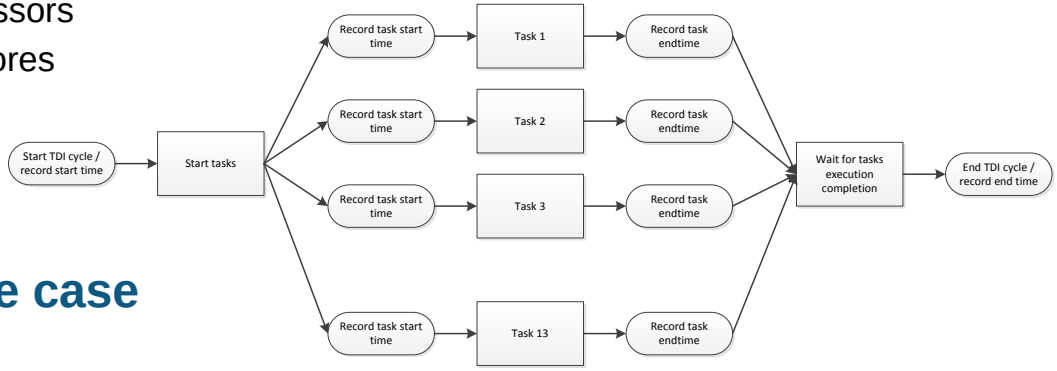
LEON4-N2X quadcore processor
Airbus DS

Efficient programming of a multicore processor is tricky !

- Even in the mainstream industry the transition took quite some time!
- Needs to be taken into account both at RTOS and application level
- Hard real time, highly deterministic execution is really difficult to achieve (really)

Software programming environment to be adapted

- Improving RTEMS and Hypervisors support for multicore processors
- Methods, tools to optimize software parallelisation on several cores
- Development of runtime libraries for parallel programming
- Investigating new techniques for schedulability analysis
- Well supported by Agencies (ESA, CNES…)

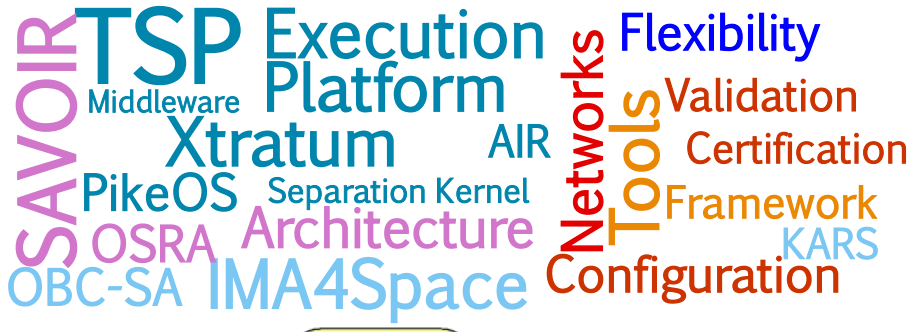


Parallelization scheme of the GAIA VPU application

Evaluation of Leon multicore on application use case

- GAIA VPU algorithms on GR740 prototype boards and GR712
  - Parallelization of the application was straightforward
  - Performance is limited by our ability to effectively load all processing cores
  - With a GR740 @ 250 MHz, GAIA VPU application runs as fast as on Maxwell SCS750 with much better power efficiency (1/3)

IMA and Software Partitioning



Hypervisors for time an space partitioning

Project IMA for Space (ESA)

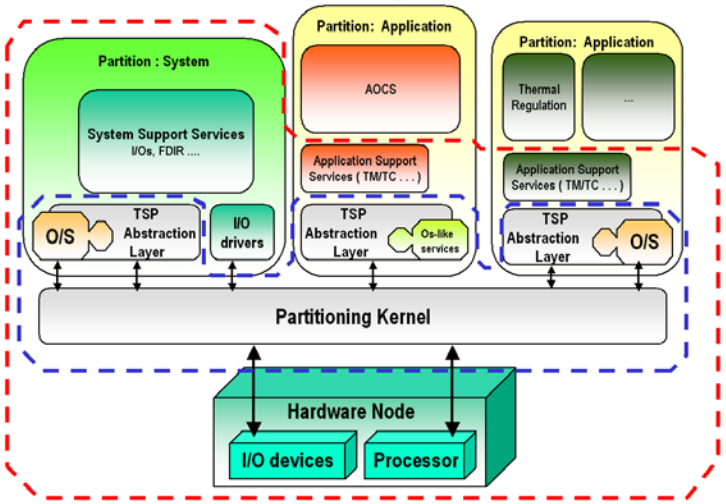
- defined the partitioning concept for space
- evaluated feasibility with several use cases and hypervisor technologies
- Baseline for SAVOIR reference architecture

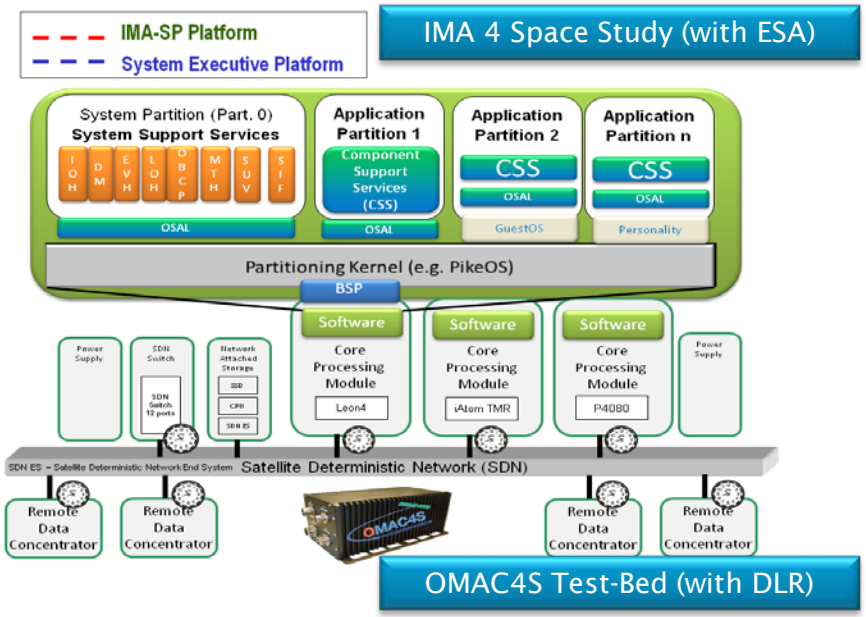
Project OBC-SA (DLR)

- Development of the OMAC4S test bed

IMA Kernel Qualification

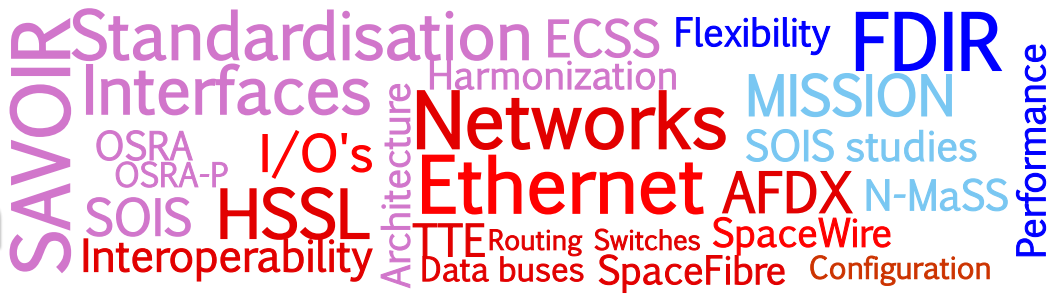
- Specification of Hypervisor functions and qualification requirements
- Adaptation of hypervisors to targets:
  - Multicore (ARM, NGMP…)
  - RTEMS and other operating systems
- Space qualification planned in 2016 for Xtratum, PikeOS,…





AIRBUS DEFENCE & SPACE

On-board communications & Interface Standardisation

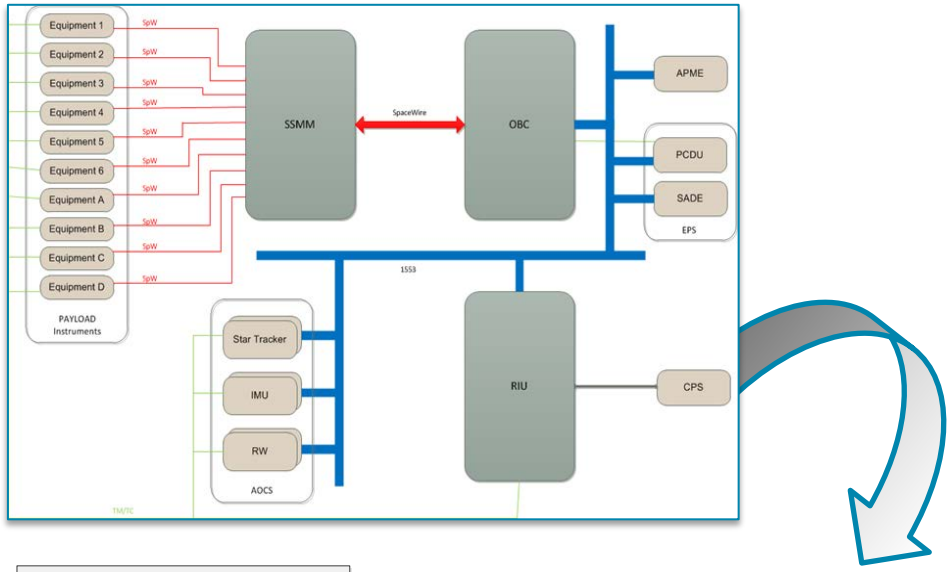


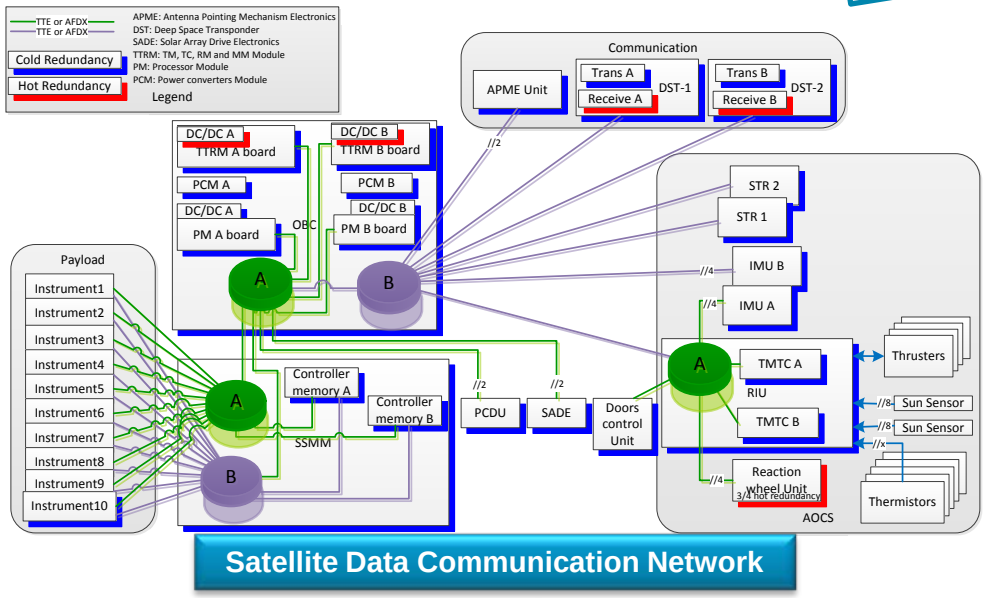
Satellite Data Communication Network

- **Common standard network interface**
  - Platform and payload on satellites
  - Command control and telemetry on launchers
  - Reduces costs to adapt products for a given mission
- **Simplify interface with Ground Test equipment (EGSE)**
- **Network Configuration, Verification, Qualification, Security and Certification issues**
  - Embedded support functions (Network management, FDIR, debug, security functions..)
  - Engineering support tools: modeling simulation, network analysis, formal proof…
- **Evolution of SpaceWire with SpaceFibre**
- **Switched Ethernet with different protocols/QoS**
  - AFDX (Mission project), Time-Triggered Ethernet, Standard Ethernet
  - Synergy with aeronautics and Ethernet I/F included in several COTS components
  - Ariane 6 and Orion/MPCV selected TT-Ethernet

Sensor Networks

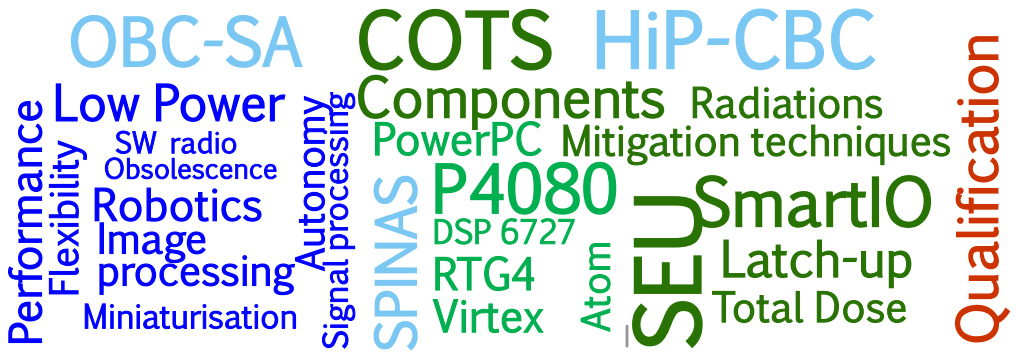
- Many simple terminals (e.g. thermistors) on spacecraft: lots of wires
  - Digital sensor networks (low complexity terminal, many sensors, low bandwidth…)
- Wireless
  - Main issues are with EMC and power autonomy, not with data handling & protocols





Satellite Data Communication Network

COTS Based Computing Architecture



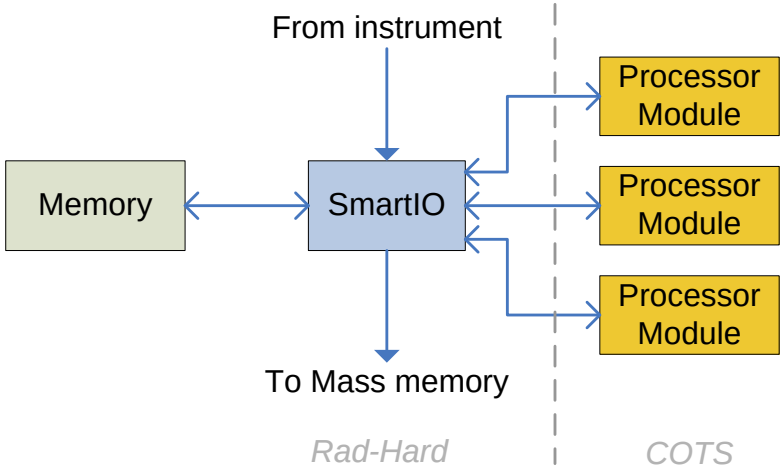
High Performance COTS Based Computer (ESA)

Concept

- Rad hard SmartIO component is in charge of the interface between the COTS world and the rad hard world. It implements the fault mitigation.
- COTS components are managed by SmartIO shared memory mechanisms
- The SmartIO buffers instrument data in a fast local memory, and replays it in case of error
- Several COTS based Processing Module (PM): µP or FPGA

Benefits

- SmartIO / PM link is a standard HSSL such as SpW, SpFi, SRIO, PCIe_serial, Gbit_Ethernet…
  → flexibility, processor independence
- PM's are slaves of the SmartIO : simplicity of the fault model
  → reduced radiation campaign
- SmartIO includes HW+SW to manage fault mitigation
  → versatility
- Batch processing and results checks with signature
  → performance
- Scalable Architecture
  → adaptable to mission requirements

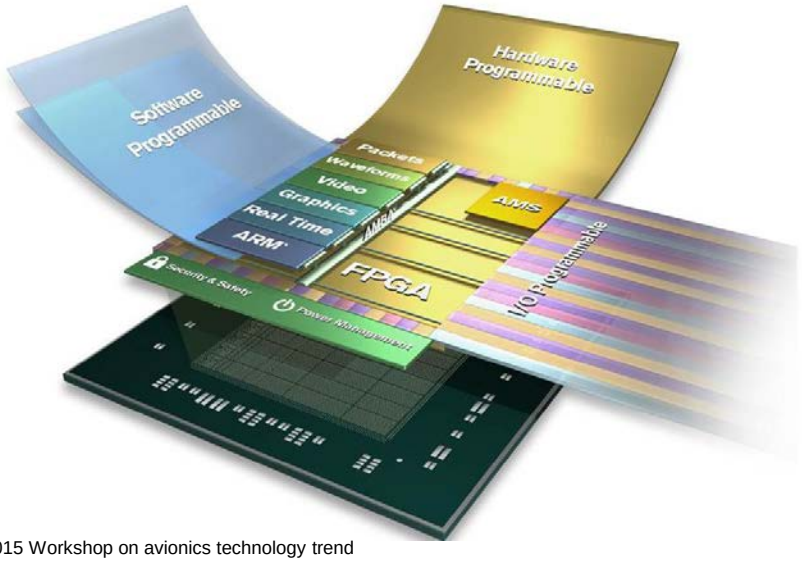


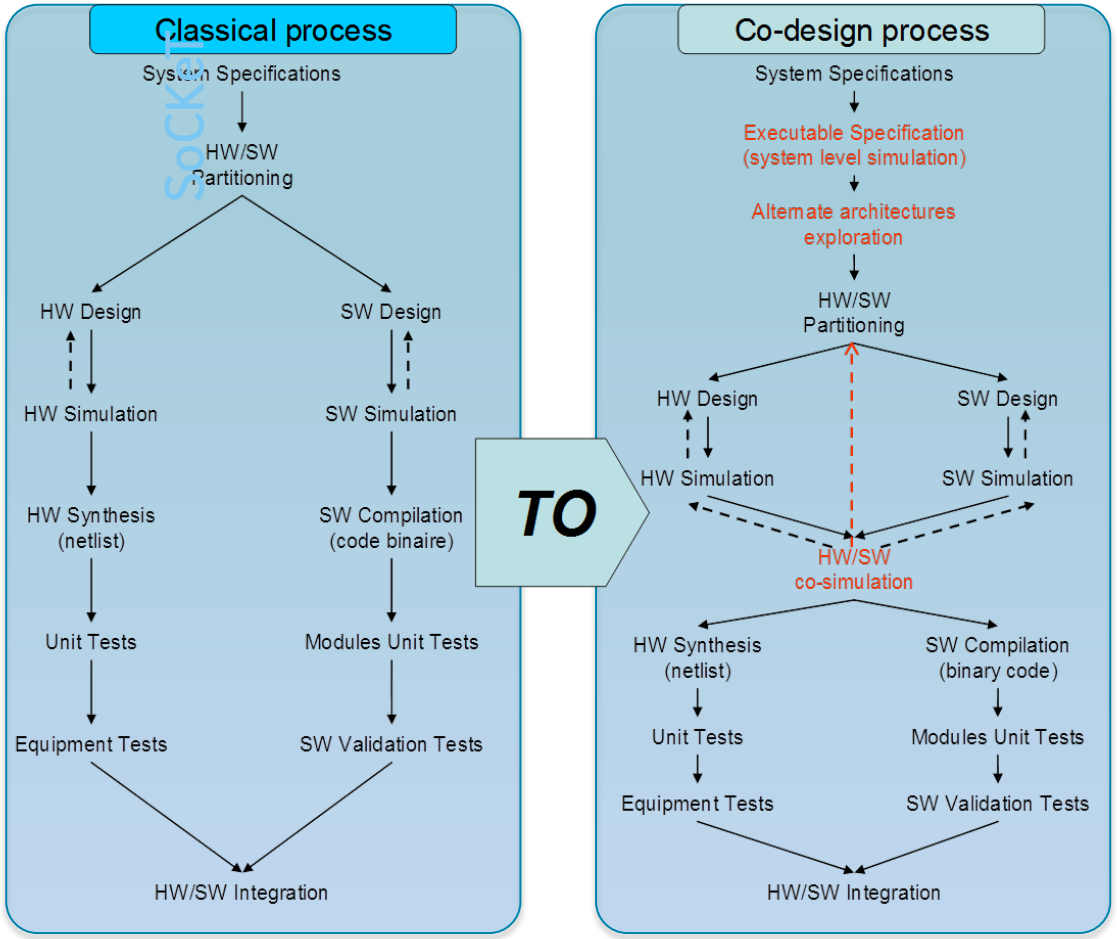
High Performance COTS Based Processor board developed with TI DSP C6727 (ESA study)

HW/SW codesign

CoDesign Process for parallel S/W and HW functions development

- Trans-domain collaboration (Socket, Projet P, IRT projects)
- Modelling techniques (System C)
- Co-simulation HW/SW
- Coherent development of HW and SW
- Seamless design flow
- Autocoding
- Very efficient on hybrid execution platforms such as Zynq



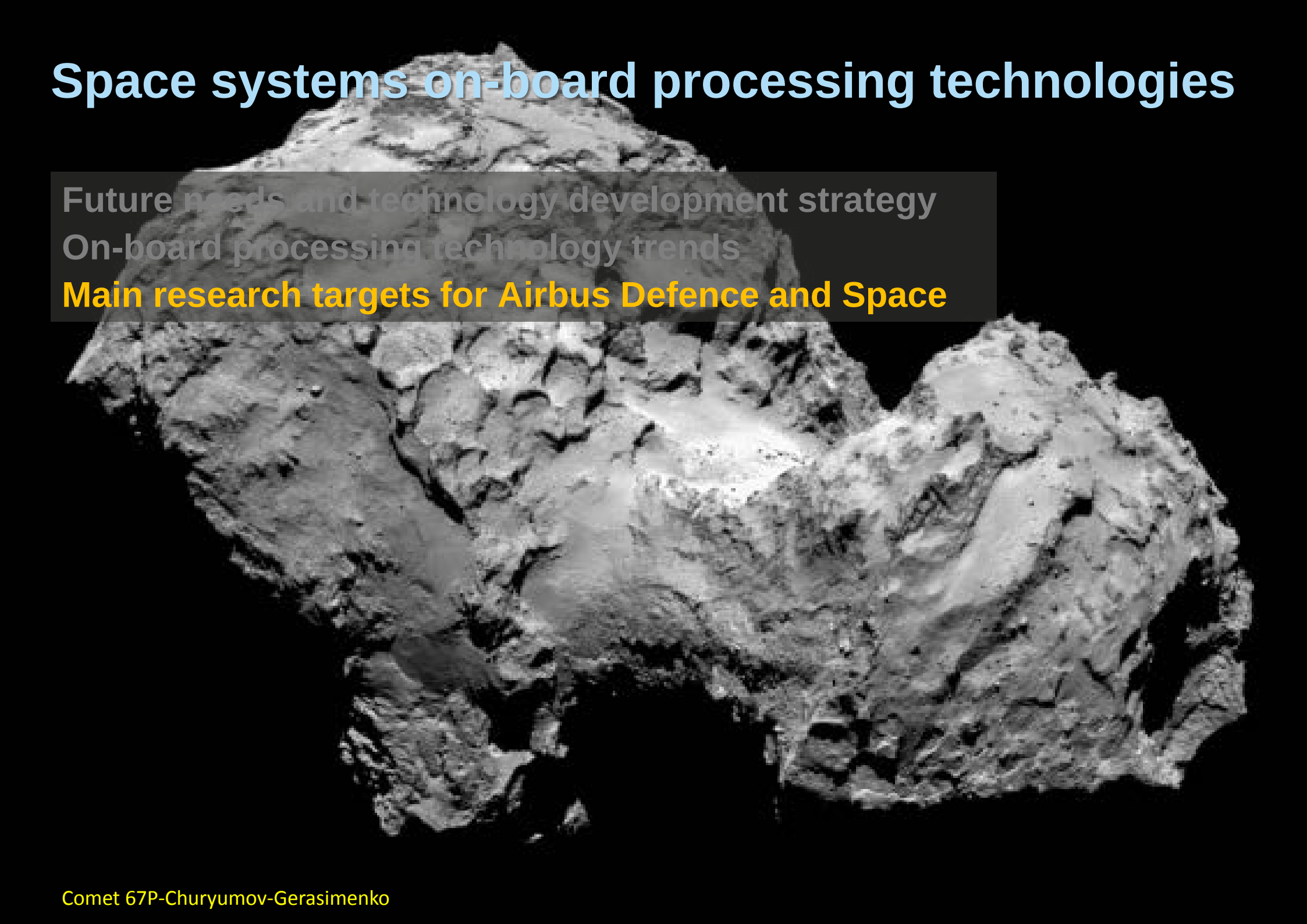


Space systems on-board processing technologies

Future needs and technology development strategy

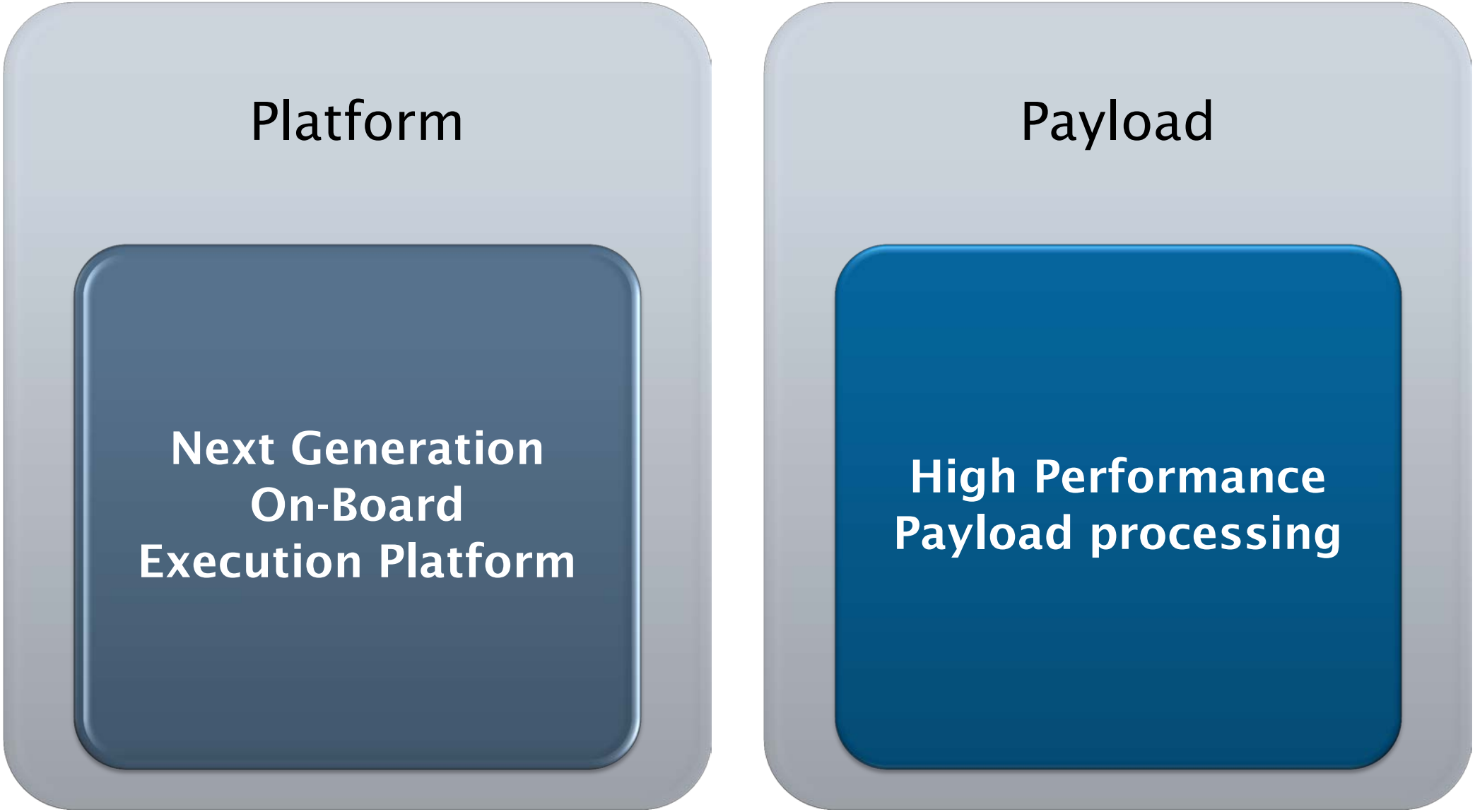
On-board processing technology trends

Main research targets for Airbus Defence and Space



Comet 67P-Churyumov-Gerasimenko

Main research targets



Next Generation execution platform

Multi-core processors and COTS processors

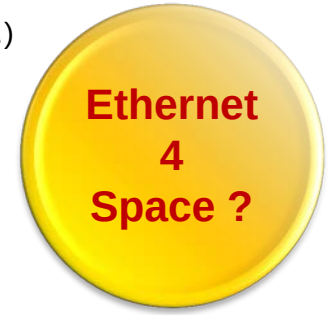
- **ARM Multicore**
- **GR740 (NGMP 4-cores Leon) in the short term**

Secured partitioning software execution platform for central computer

- **Time and Space Partitioning (enabling technology)**
- **Hypervisor, operating system, Software on multicore issues etc…**
  - Separation Kernel Qualification in preparation
  - Several R&T in progress
- **On-Board Software framework based on reusable product lines**
  - Execution platform with hypervisor, Real-Time Operating System and standard I/O's handling
  - Data Handling Software and operational standards (PUS, FMS, CFDP…)
  - Auto-coded AOCS application + integration of third party software

Satellite Data Communication Network (SDCN)

- **Communication standards with common API to execution platform**
  - Legacy interfaces (1553/SpW/Can) to comply with current satellites equipment product lines
  - New interfaces supporting higher data-rate and lower cost with convergence toward COTS technologies (e.g. Ethernet)
- **Future SDCN technology**
  - ESA studies on platform command and control centralisation with SpaceWire (SpaceWire-D, SpaceWire based AOCS, N-Mass…)
  - FP7 Mission project « AFDX for Space »
  - Ethernet 4 Space
    - Ariane 6 decision on TTE technology → available reusable building blocks
    - ESA road map for Ethernet:
      TTE protocol targeting launchers and manned flight, including ECSS standardisation and Devices characterisation for the physical layer
    - Ethernet based solution for spacecraft is supported by Airbus R&T with CNES/DLR/ESA studies in the pipe



High Performance Payload Processing

State of the art

Custom ASIC's

e. g. image compression (MCITHI), FFT (FFTC)

- ► **High performance**
- ► **Limited to specific applications**
- ► **High non-recurring cost**
- ► **Outdated silicon technology**

Rad-hard programmable components

e.g. FPGAs RTAX2000, RTG4, LEON processors, 21020 DSP

- ► **Medium performance**
- ► **High recurring cost**

COTS based processors

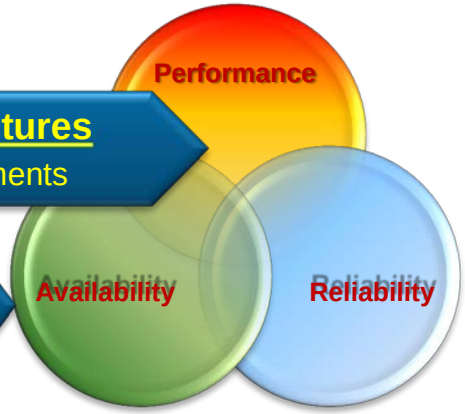
(e.g. Maxwell SCS750 on GAIA VPU)

- ► **Medium performance**
- ► **High RC and US dependant technology**

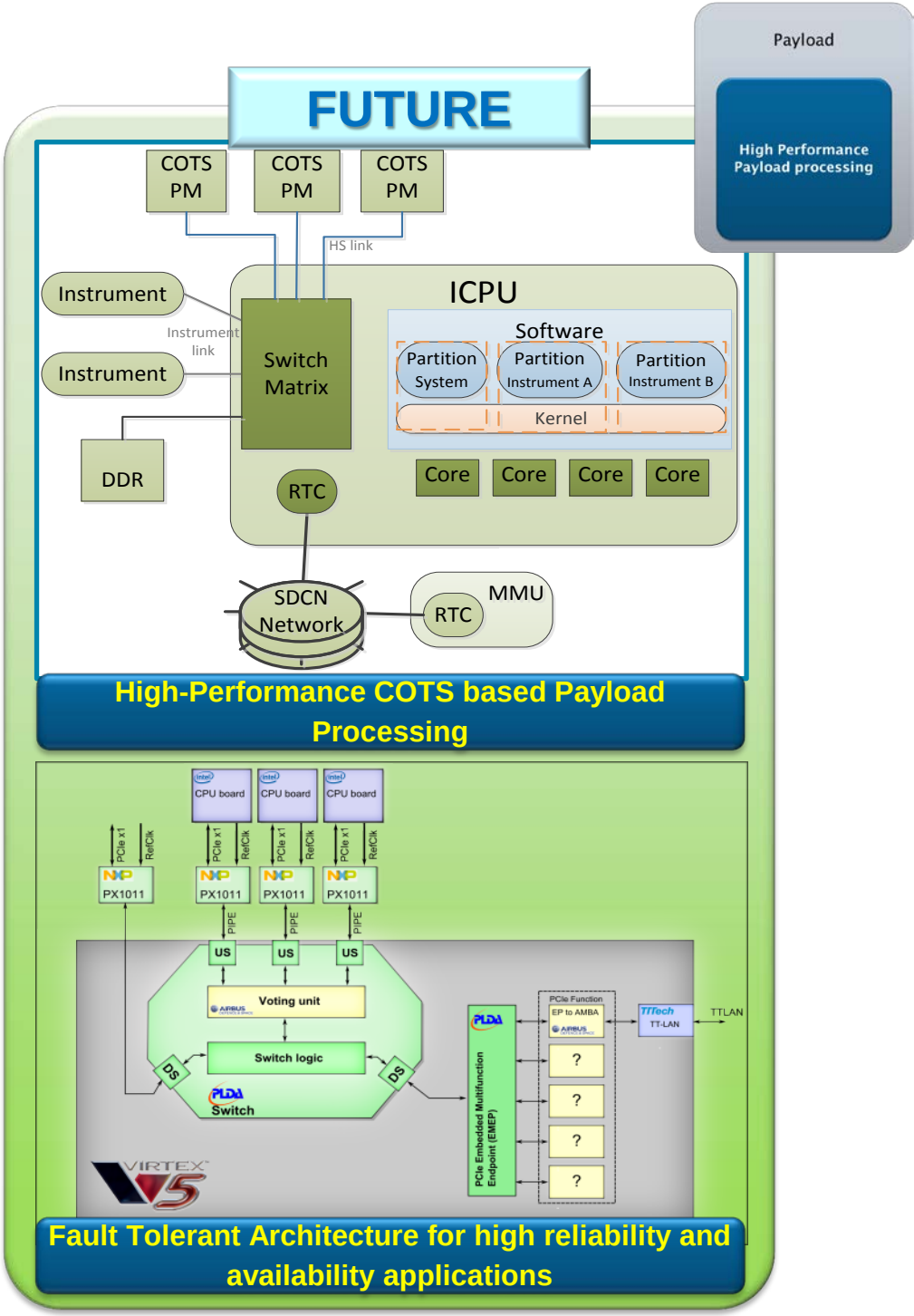
Need for flexible generic processing at lower costs

COTS based computing architectures
Adapted and tailored to mission requirements

Space grade key components
NGMP and BRAVE



FUTURE



Summary - Main research targets for Airbus Defence and Space

Platform data processing

- Higher performance On Board Computers at lower cost
  - Multicore Leon (GR740/NGMP)
  - COTS based (ARM)
- Secured Partitioned Software Execution Platform on Multicore Leon and ARM
  - Hypervisor/Separation Kernel(s) (Xtratum, PikeOS,…)
  - Software engineering maturity, tools, methodology for multicore and Arm
- Equipment interoperability through interfaces standardisation
- High data rate Satellite Data Communication Network with Switched Ethernet

High Performance Payload Processing

- High Performance Space Grade reconfigurable FPGA (BRAVE)
- Multicore Leon (GR740/NGMP) when relevant for specific missions/instrument
- COTS based high performance computers including µP and reconfigurable FPGAs
- Radiation mitigation techniques for COTS Based Computers (SmartIO)

More COTS @ Less COST

Functional Centralisation

Interfaces Standardisation

Space Aeronautics Synergy

Reconfigurable FPGA's

COTS Based Computers

Non-dependancy

Thank you for your attention

Questions ?

AIRBUS
DEFENCE & SPACE