On Board Computer System Architecture

Avionics Technology Trends

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ESA/ADCSS Days Noordwijk 20-23.10.2015

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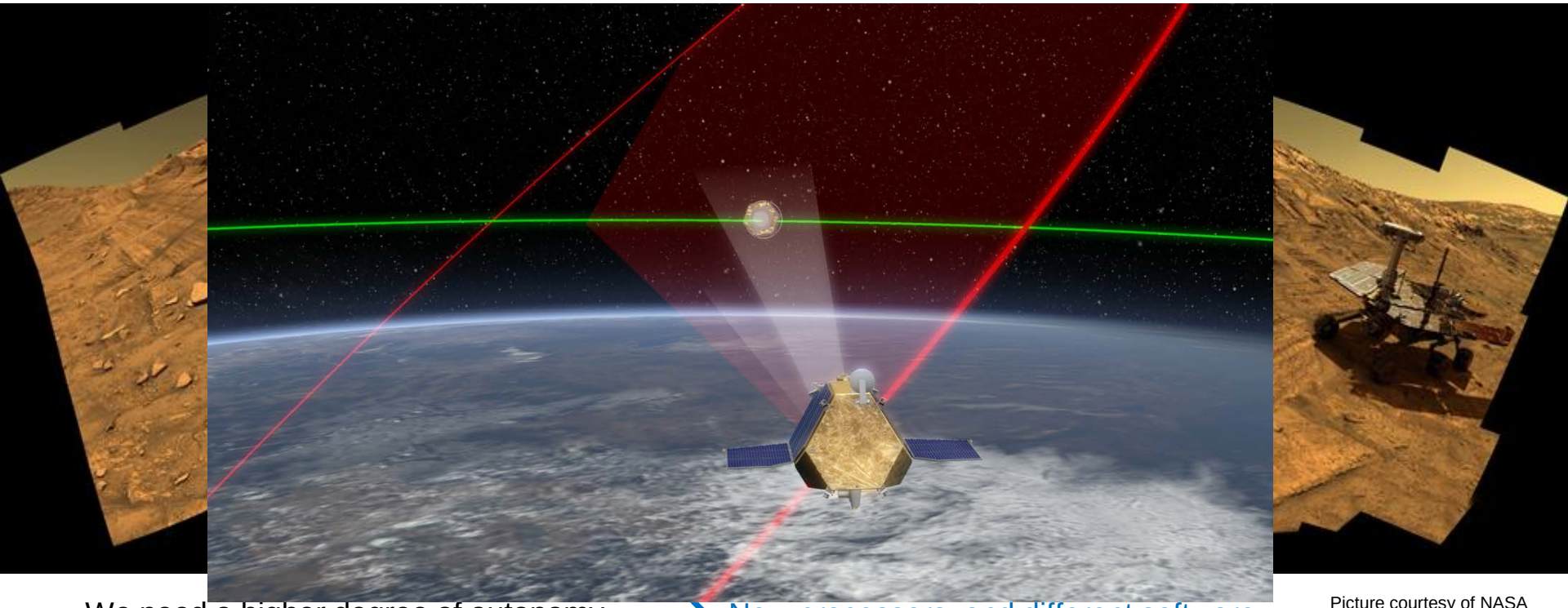
Why do we need new avionics for space applications ?



Picture courtesy of NASA

- We need a higher degree of autonomy
- We need high performing busses
- We need real time sensing

➔ New processors and different software
➔ Reliable networks
➔ Sensors
- Viewing ➔ Cameras
- Communicating ➔ Down/Up-links
- Environmental measurements ➔ Smarts sensors

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Outline

Current avionic technologies

Avionic ingredients for new designs

Future consolidated system architectures

Picture courtesy of ESA

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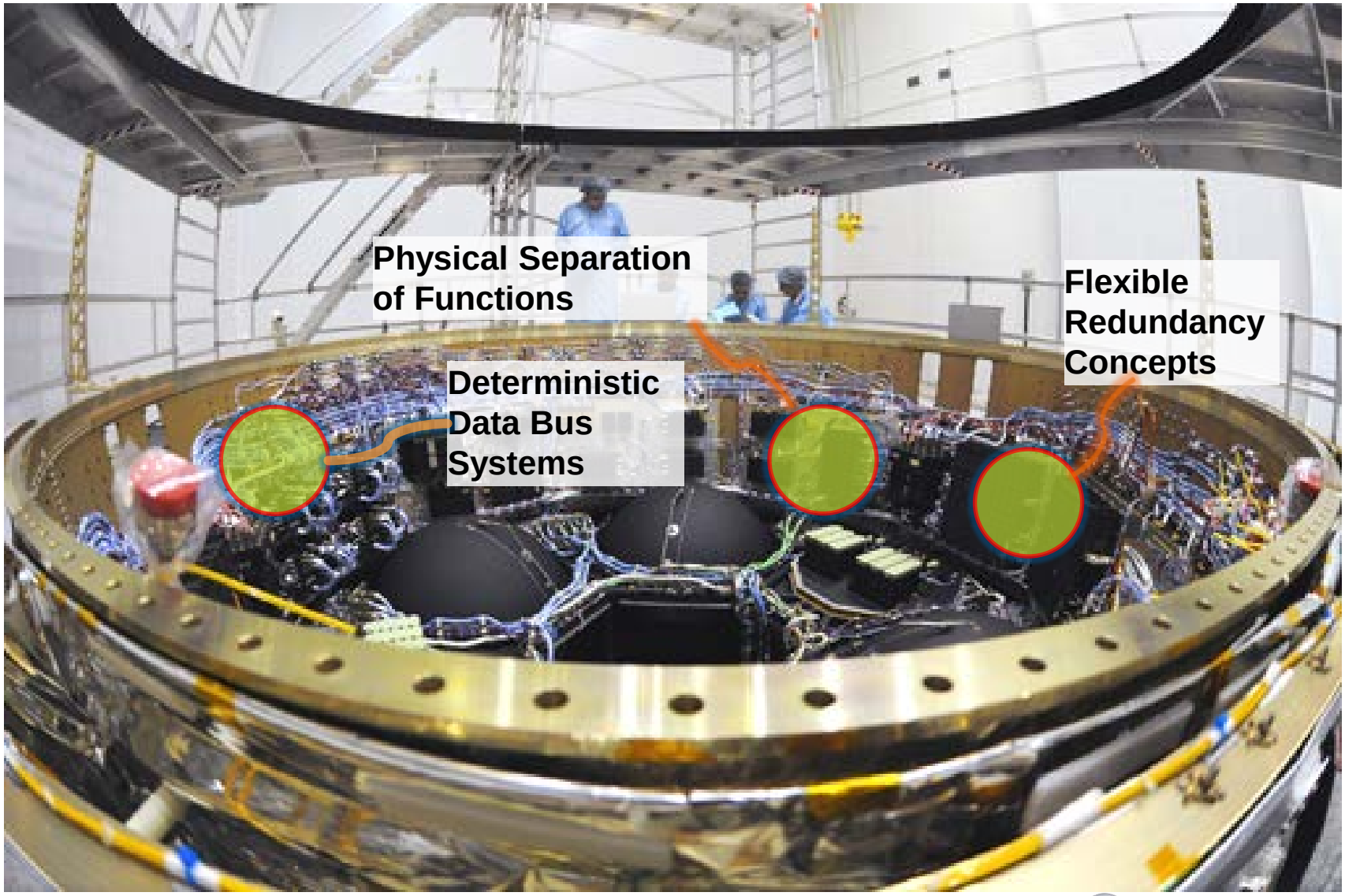
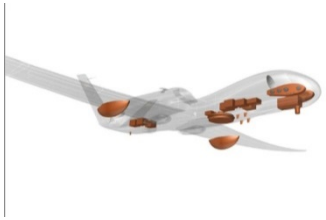
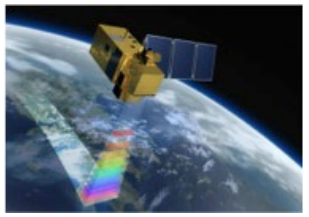
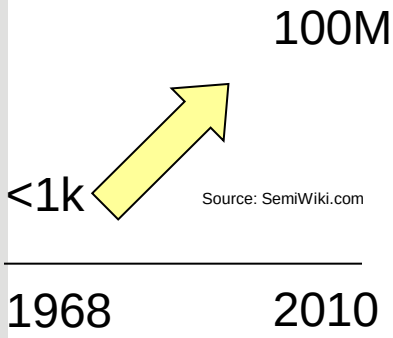
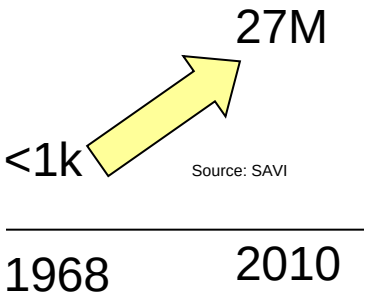
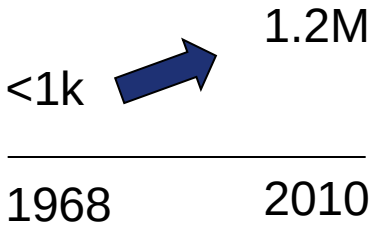
Avionics of today H/W



Avionics status of today for S/W

Domain	Automotive	Aeronautics	Space
			
Groth in SW Complexity			
Solution	AUTOSAR (2003) (AUTomotive Open System Architecture)	IMA (2000) (Integrated Modular Avionics)	SAVIOR (2007) (Space AVionics Open Interface aRchitecture)

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Situation of Avionics as of today

- Customers request more functionality
  - most of this functionality is implemented in software
  - provided CPU power needs to be much higher than today
- Many different avionic busses !
- Due to centralizes systems typically everything is Hi-REL !

- In summary we end up with systems which are :
- Highly complex
- Very expensive
  - Even in recurring mode
  - Due to obsolescence
- At the lower edge of today electronics performances !

Outline

Current avionic technologies

Avionic ingredients for new designs

Future consolidated system architectures

DLR Mission Statement for the On Board Computer System Architecture (OBC-SA) 2011

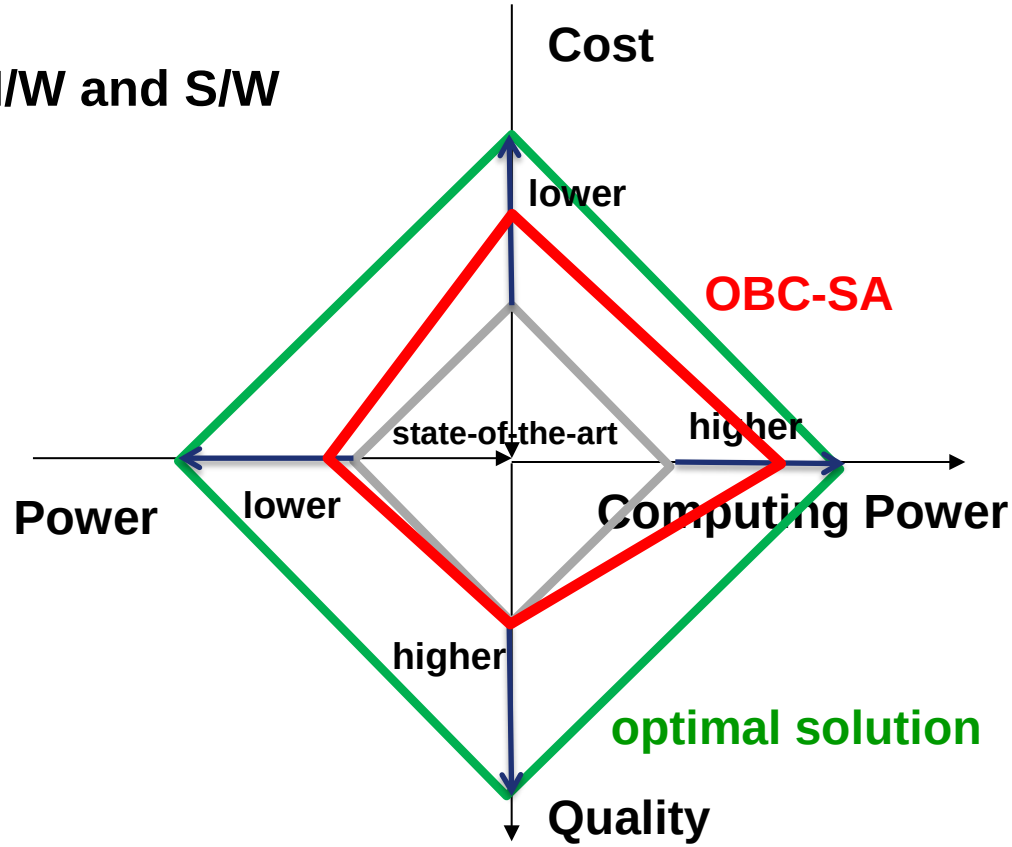
- **Motivation:**
  - The rapidly growing demand on computing power in most modern space missions can not be covered by todays On Board Computers (OBC)
- **Goal:**
  - Development of a high performance, high availability and scalable on-board-computer system architecture
- **Concept:**
  - Using a modular design of components by having standardized I/F

Gefördert durch:
Bundesministerium für Wirtschaft und Energie
aufgrund eines Beschlusses des Deutschen Bundestages

Motivation

New mission types having increased level of autonomy come up with new requirements.

Increased system complexity for H/W and S/W



OBC-SA:

- Lowers power consumption
- Reduces cost
- Enhances the computing power
- Keeps quality

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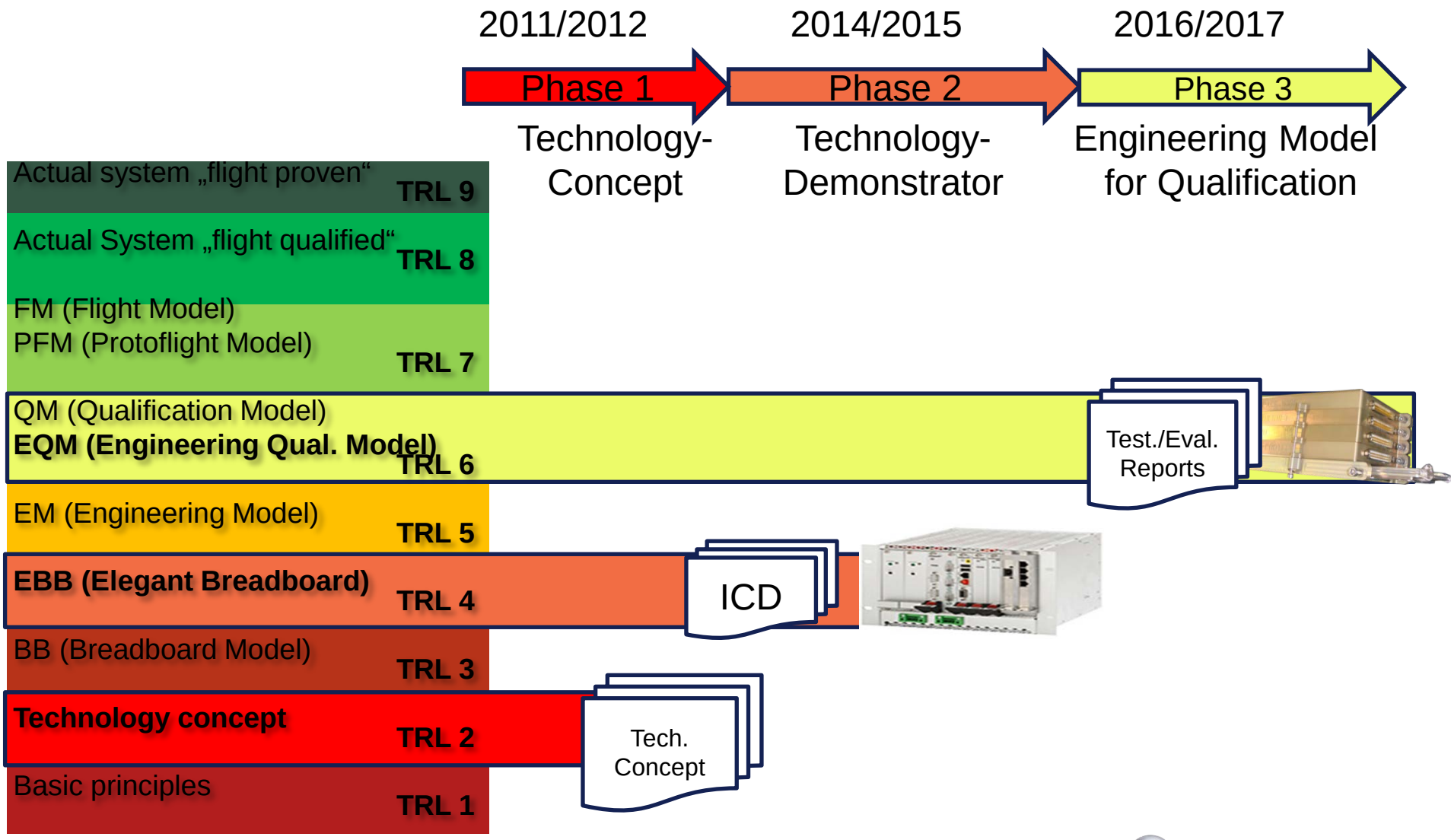
OBC-SA Phasen, TRL and Models



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How to do it ?

Savoir/Integrated Modular Avionics (IMA)
- De-centralized architecture

Different processor types
- Radiation Hard (HI-REL RH)
- Commercial Of The Shelf (COTS)

Time Space Partitioning (TSP)
- Hypervisor and Real Time-OS (PikeOS)

High performance deterministic bus
- Time Triggered Ethernet (TTE)

High Performance Backplane
- Compact PCI serial (cPCI)

DLR AIRBUS DEFENCE & SPACE STI SYSGO EMBEDDING INNOVATIONS TTTech Ensuring Reliable Networks Fraunhofer FOKUS essei

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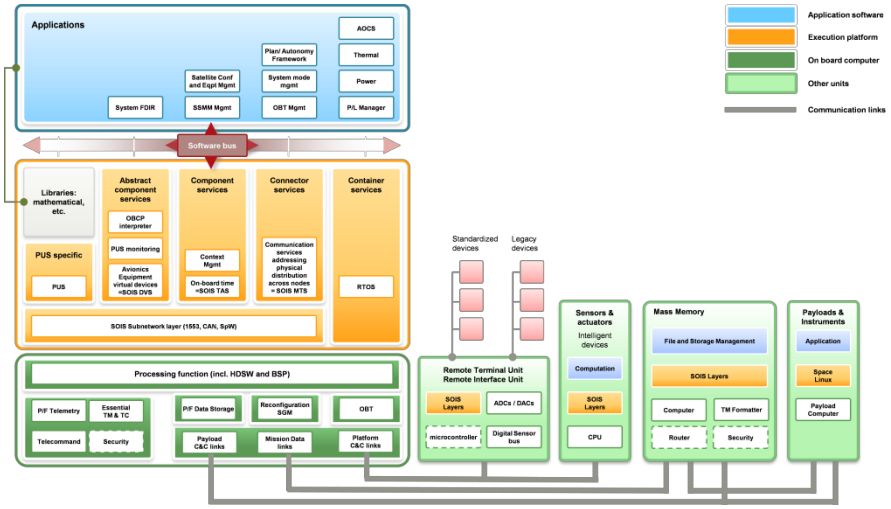
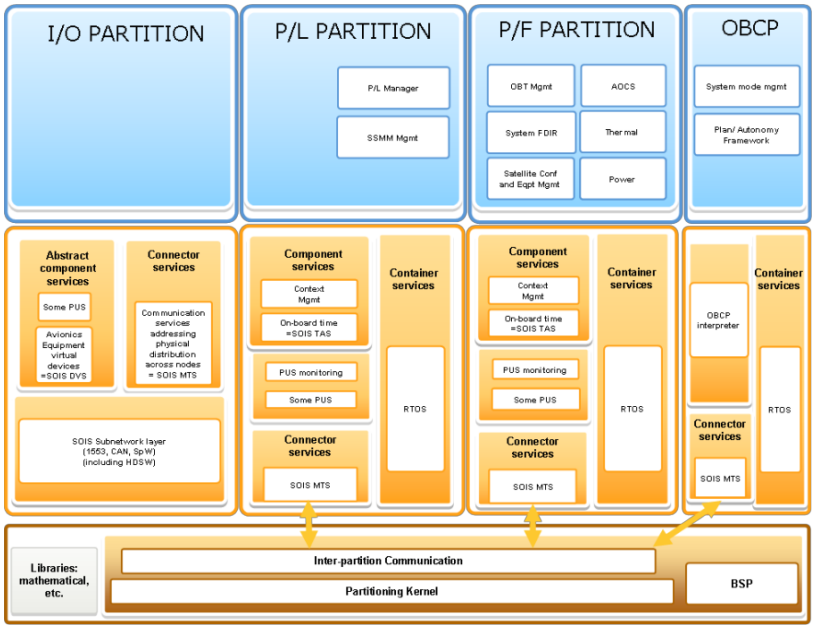
SAVOIR Approach (Full blown)



Reference Architecture



CorDet-IMA

http://savoir.estec.esa.int/

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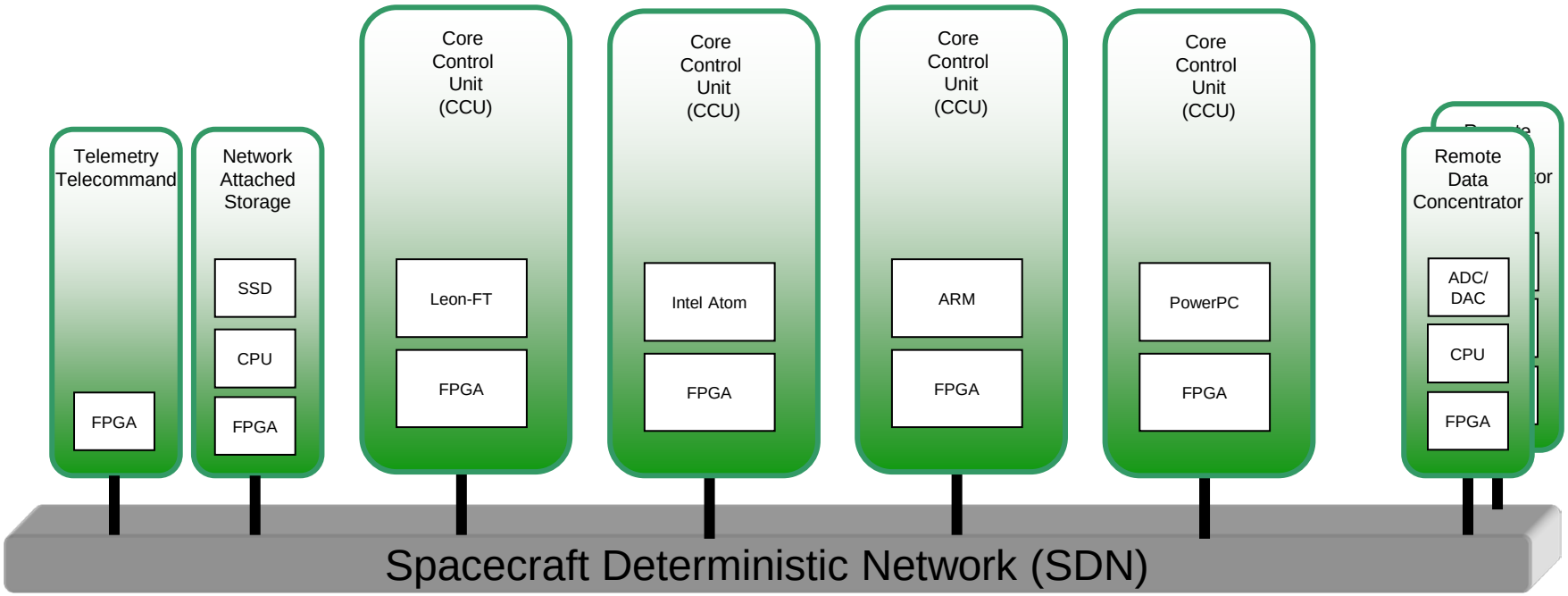
OBC-SA (SAVOIR tailored)



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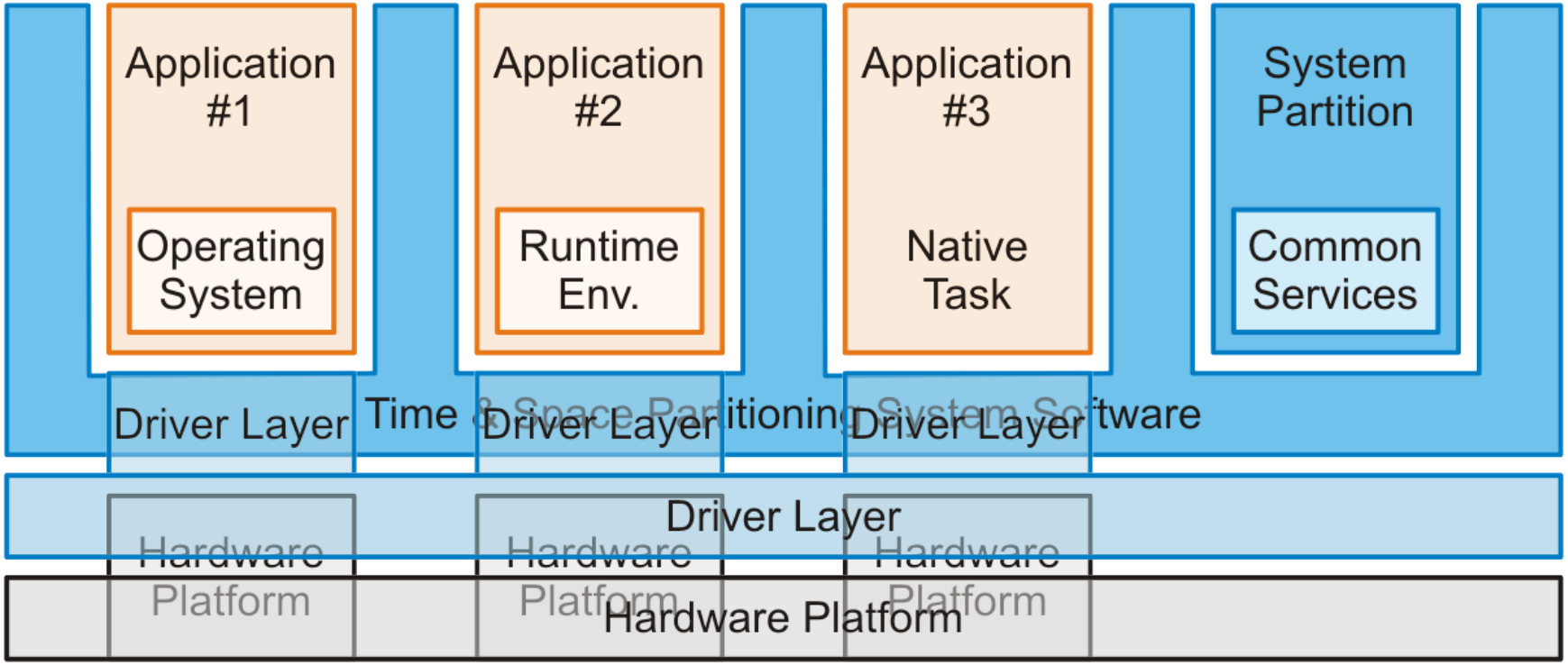
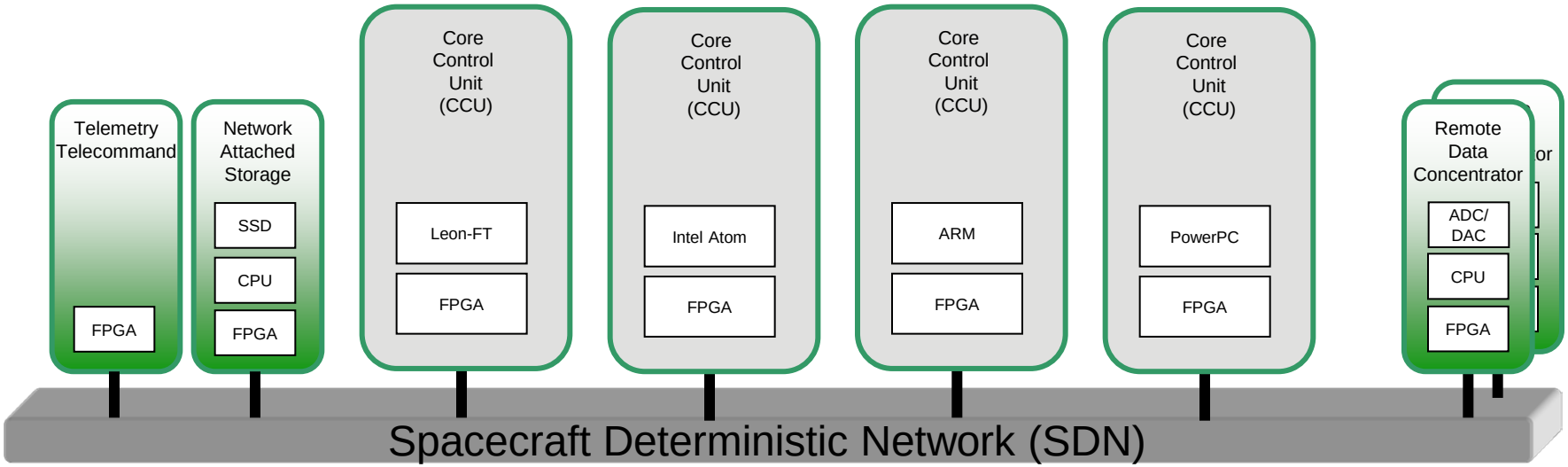
OBC-SA: Integrated Modular Avionics (IMA) Aproach



Which Processors fits best to this approach ?



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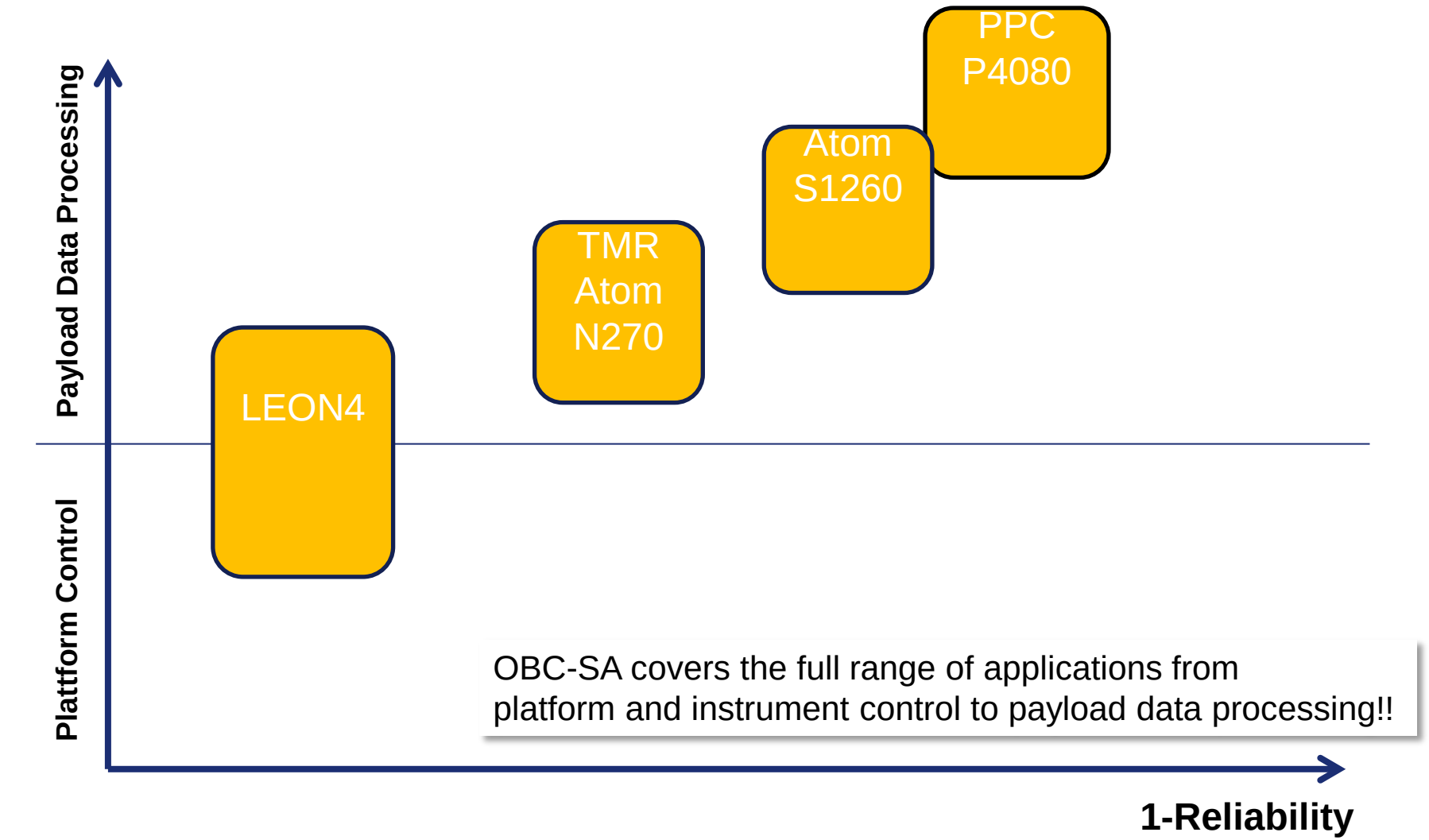
OBC-SA Coverage



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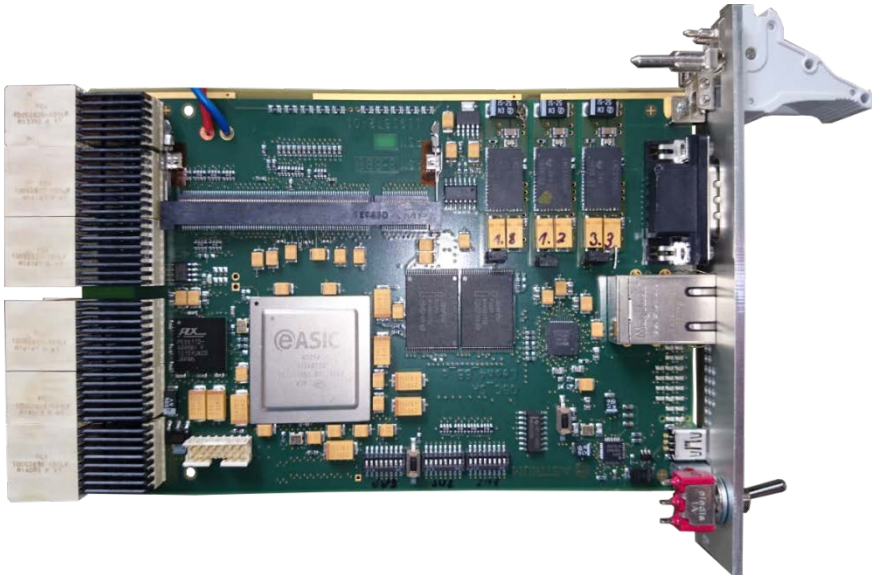
High Reliable Processing Node HRPN - SPARC V8 LEON

- **LEON4-N2X quadcore processor (NGMP)**
  - CompactPCI® Serial (PICMG® CPCI-S.0) interface
  - Clock speed: up to 150 MHz → 400MHz
  - Performance: WPDproximately 800 MIPS
  - RAM: 1GB DDR-2
  - FLASH: 64MB
  - Interfaces:
    - PCI serial
    - 1000Mbps Ethernet
    - Spacewire Router (optional)
    - MIL1553b (optional)
  - JTAG and DSU via USB debug interfaces
  - Flexible interface configuration through separate Xilinx Virtex-5-based I/O board
  - OS
    - SYSGO PikeOS real-time operating system
    - VXWorks 6.7



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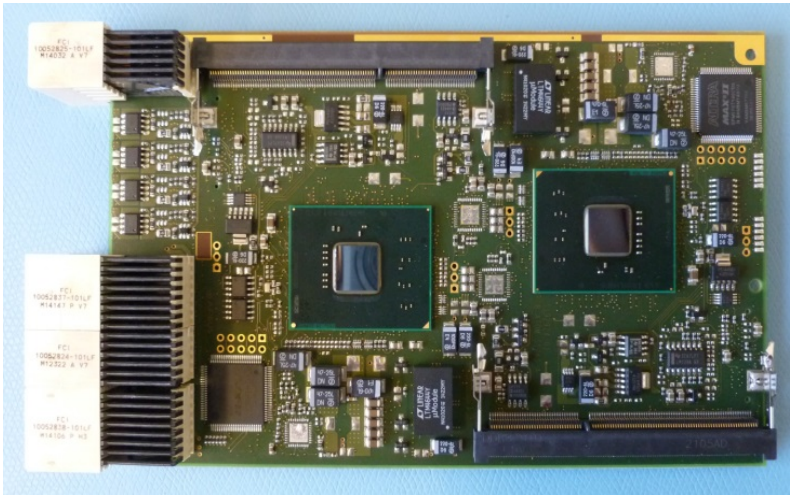
High Availability Processing Node HWPDN – x86-2

- **HWPDN – x86-2 (available)**
  - CompactPCI® Serial (PICMG® CPCI-S.0) interface
  - Intel Atom N270
  - Clock speed: up to 1,6 GHz
  - Performance: 3.300 MIPS / 2.100 MFLOPS
  - All power rails latchup protected
  - Flexible interface configuration through separate Xilinx Virtex-5-based I/O board

  - OS
  - SYSGO PikeOS real-time operating system
  - Linux SUSE 12.1
  - VxWorks 6.7
  - RTEMS



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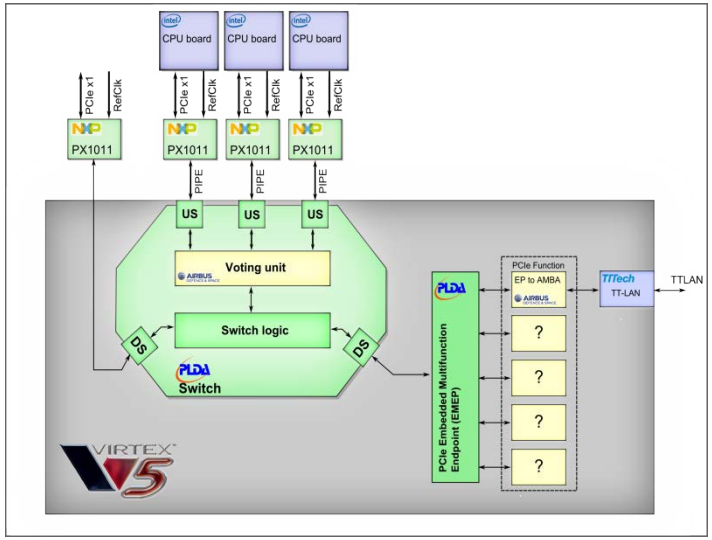
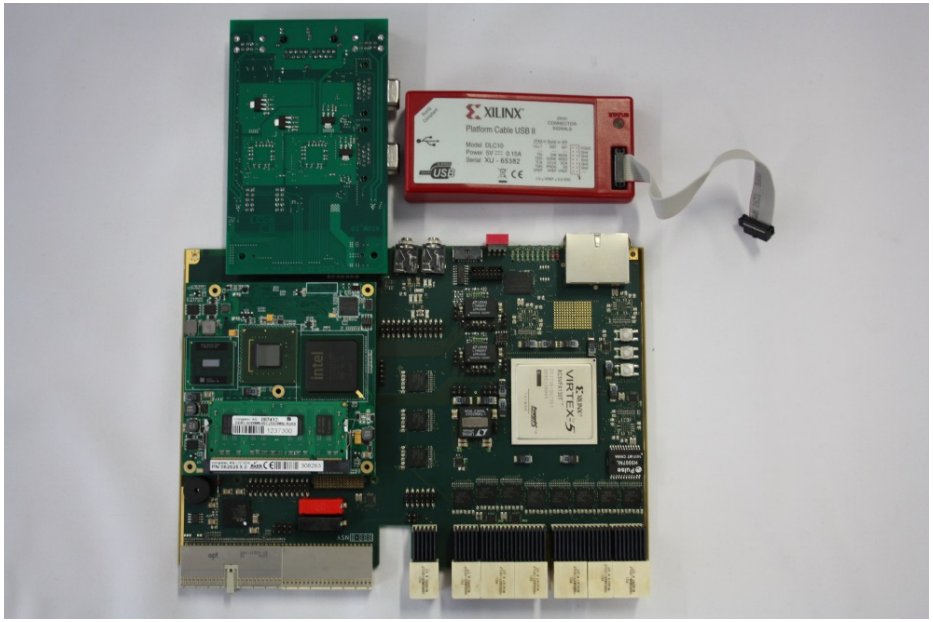
Voting and Interface Node VAIN-V5

VAIN-V5 (available)

- Synchronization and voting unit
- CompactPCI® Serial (PICMG® CPCI-S.0) interface
- Radiation-tolerant FPGA module with triple modularity redundancy (TMR) logic
- Flexible interface configuration via Xilinx Virtex-5
- Internode communication based on TTEthernet





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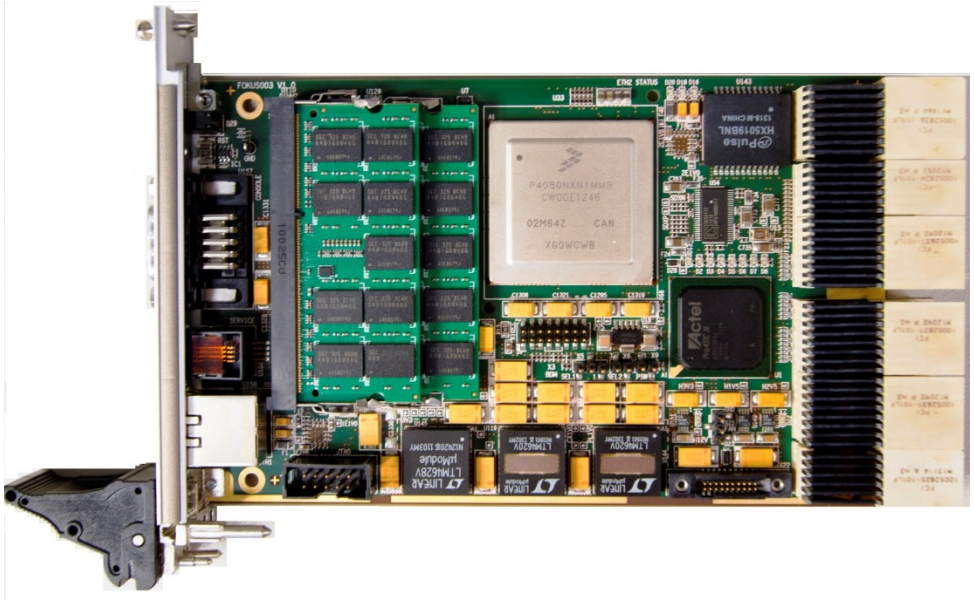
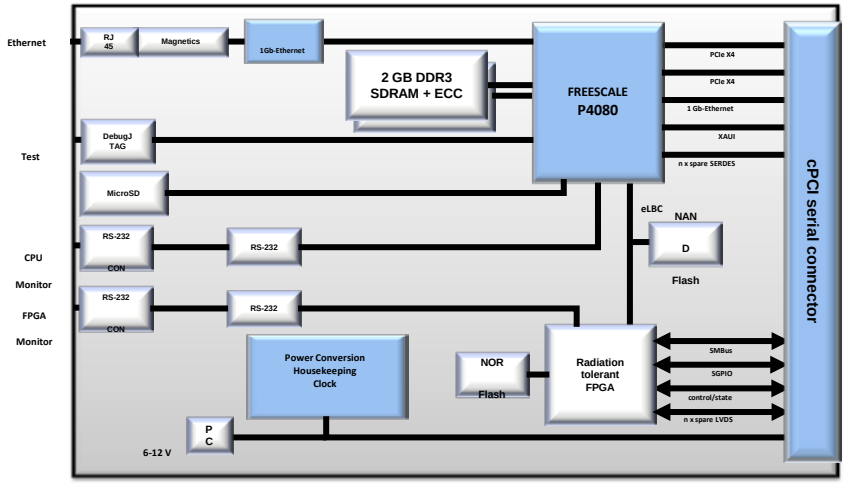
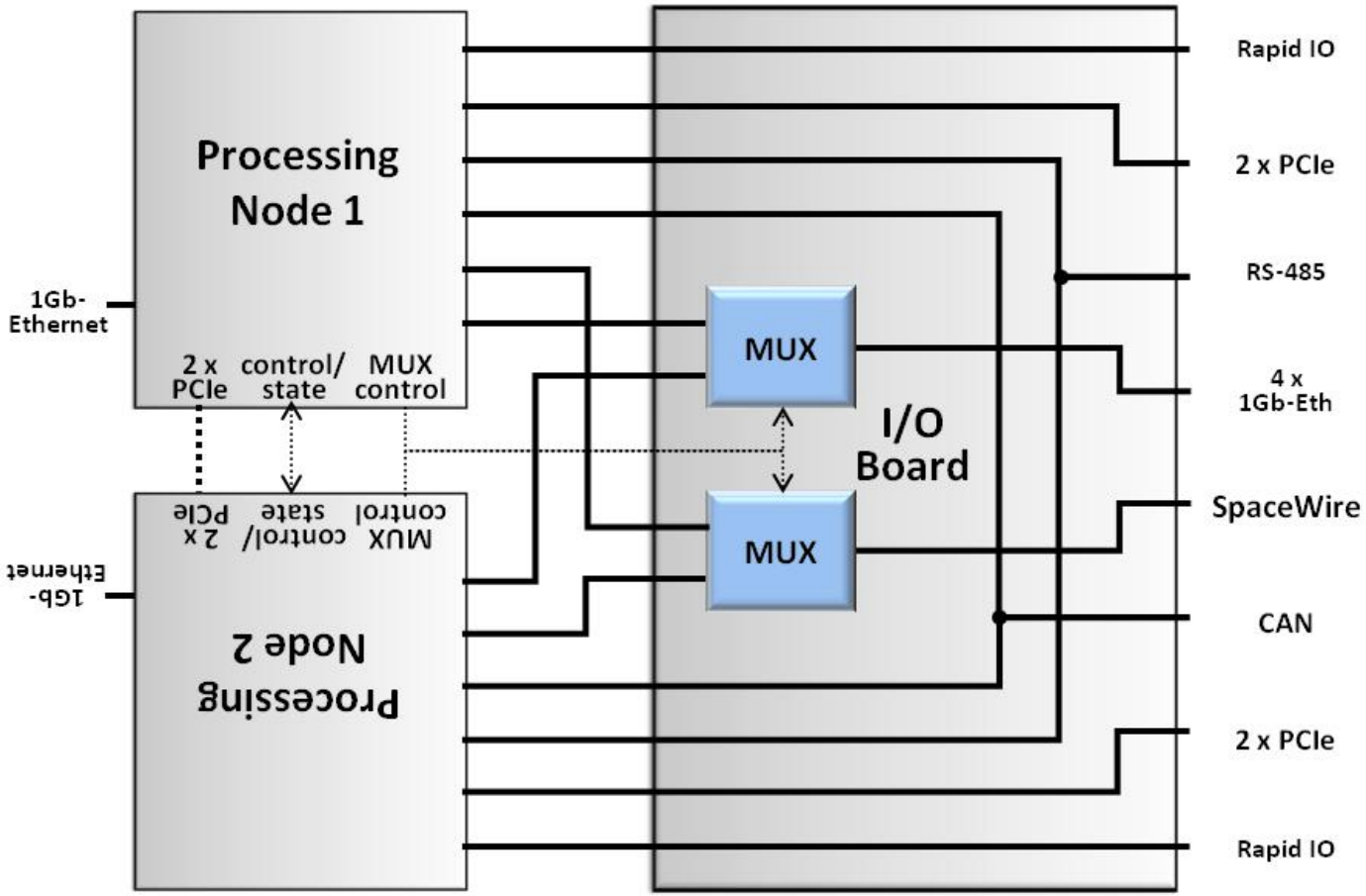
High Performance Processing Node HPPN – PPC-1



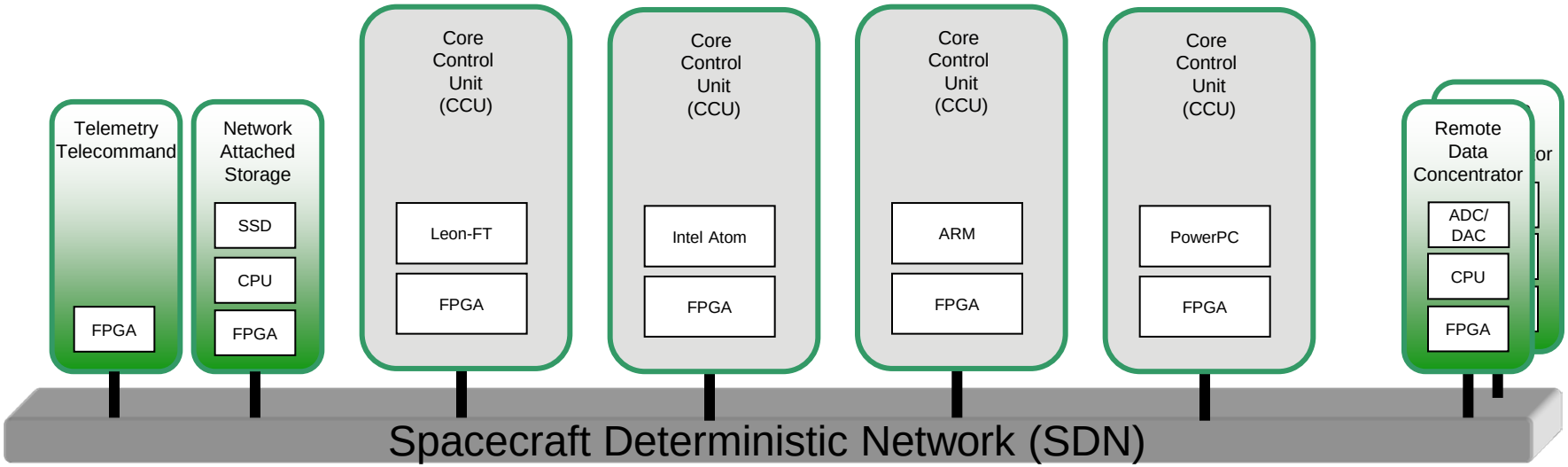


- **HPPN – PPC-1 (available)**
  - Freescale P4080, 1.2 GHz, 8-core 32 Bit processor
  - PICMG CPCI-S.O CompactPCI Serial compliant board
  - Up to 4 GB DDR3 DRAM, ECC
  - 32 Mbyte redundant NOR Flash
  - 4 GB NAND Flash + microSD card slot (Front)
  - Rear I/O: 3 x PCIe, 2 x Gb Ethernet
  - Front I/O: 1 x Gb Ethernet, 2 x RS 485
  - Effective SEU mitigation
  - Fully self-checking node design
  - Radiation tolerant system FPGA (TMR implementation)
  - Board Support Package (BSP) and PikeOS operating system
  - Support for SMP Linux

Architecture – Redundancy and I/O Structure



PikeOS fits best to this approach



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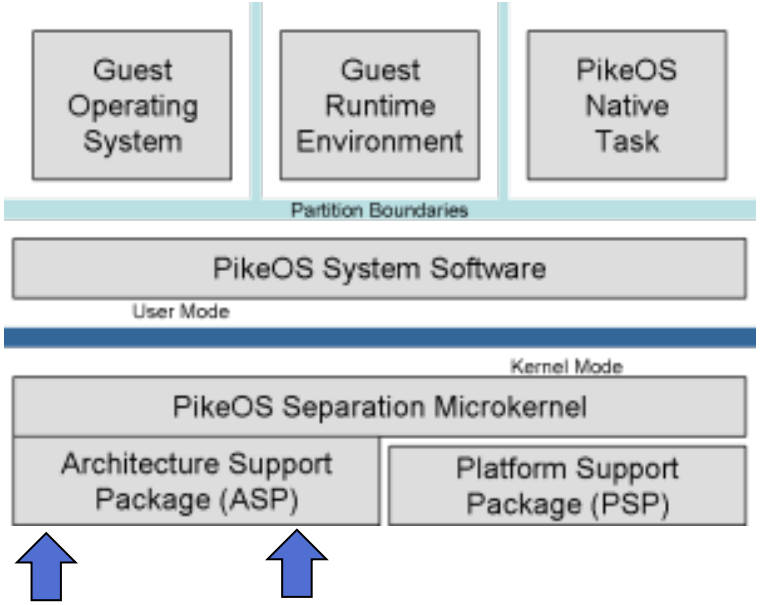
What is the net asset of a hypervisor driven system ?



Radiation Hard (Hi-Rel)

- **LEON4 SPARC V8/9**
  - Quad Core
  - 300 MHz

COTS (Single/Dual/Quad ..)

- **Intel x86 based (1-2 GHz)**
- ARM based (1 GHz)
- **PPC based (P4080)**

OBC-SA is based on a PikeOS Partitioning Kernel

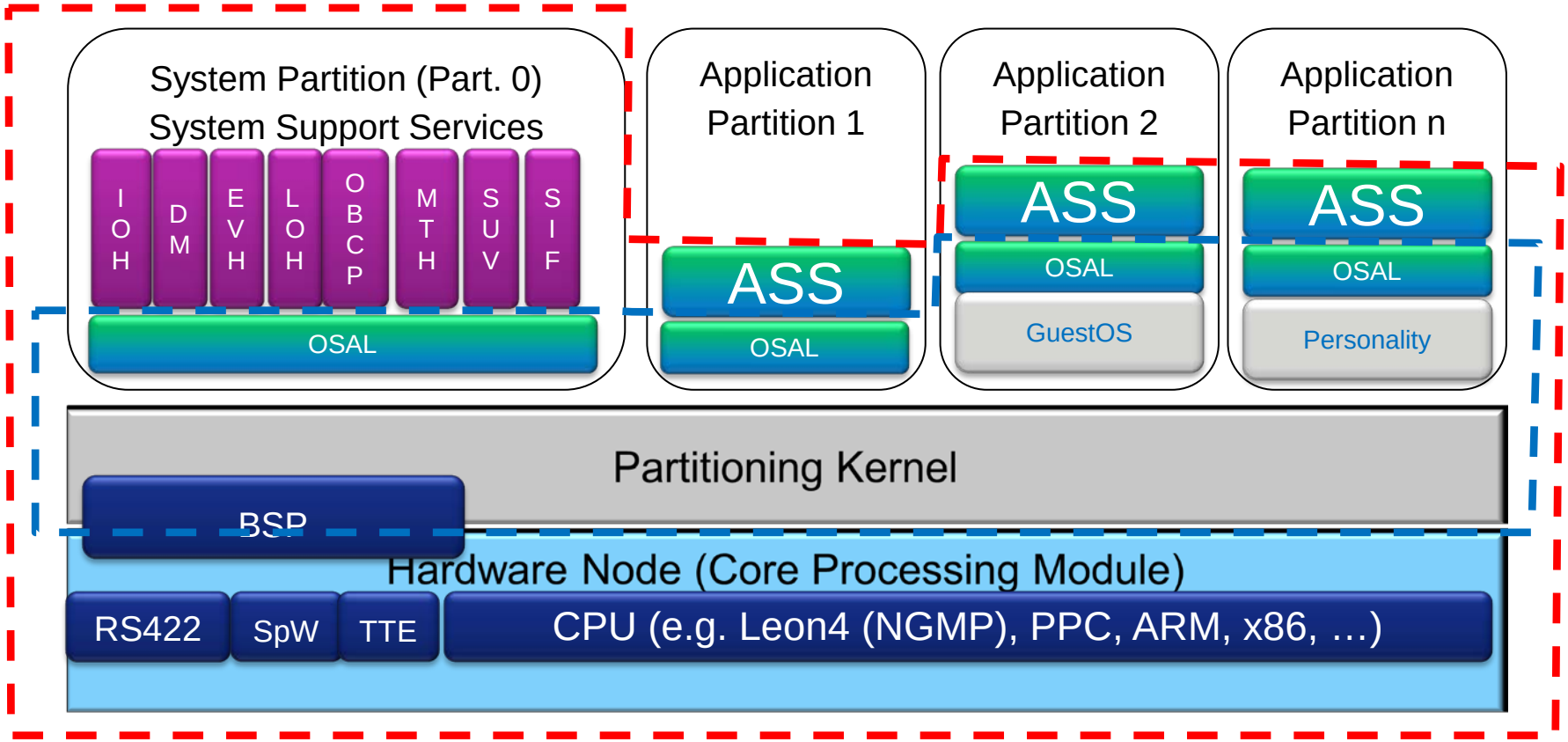
OBC-SA: Partitioning Kernel PikeOS allows:

- Abstraction of hardware
  - Hardware can be exchanged without the need to change application software
- Usage of standardised API
  - ARINC 653 APEX
  - POSIX
- Execution of guest operating systems in separated partitions
  - Linux
  - RTEMS 4.10
  - VxWorks
- Separation of heterogeneous networks
- **Results have been validated on three different platforms based on SPARC V8/9, PowerPC, x86**

OBC-SA: High-assurance certification on multicore hardware is possible

- PikeOS has been certified for EN 50128 SIL4 on a x86 multicore
  - EN 50128 SIL4 is comparable with ECSS-E-ST-40C / DO-178B Level A

OBC-SA Standardisation of S/W Interfaces and Services



ASS Application Support Service
OSAL Operating System Abstraction Layer

IMA SP Platform
System Exec.Platform

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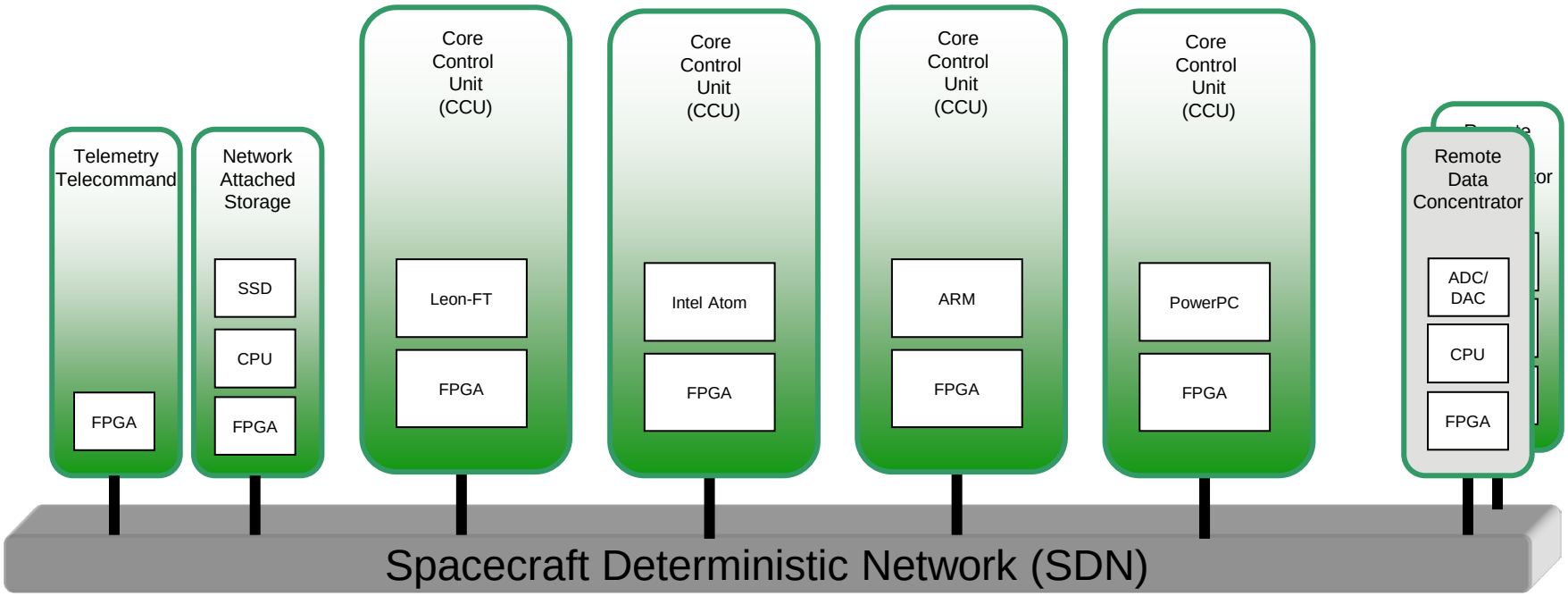
OBC-SA (SAVOIR tailored)



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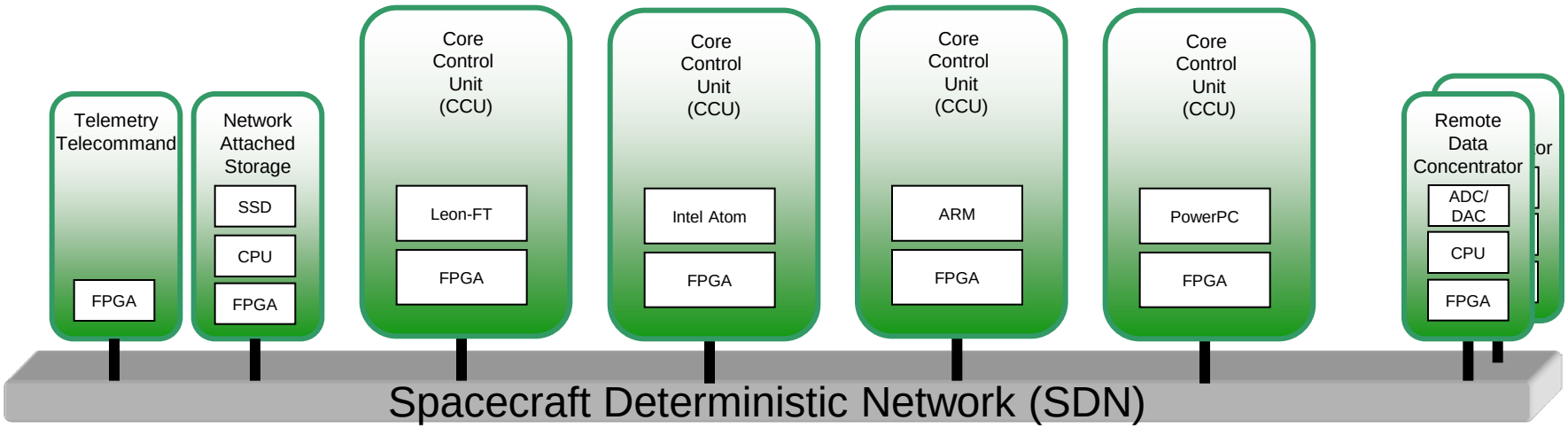
Remota Data Concentrator (RDC)

- **RDC interfaces (available)**
  - 1x TTEthernet
  - 7x analogue input
  - 2x analogue output (DAC)
  - 8x PWM output
  - redundant CAN
  - 2x pulse counter
  - 32x GPIO
  - 2x UART

  - power supply +5V
  - power consumption < 3W
  - dimensions 170mm x 100mm x 23mm
  - mass <110 g

Which Spacecraft Network fits best ?



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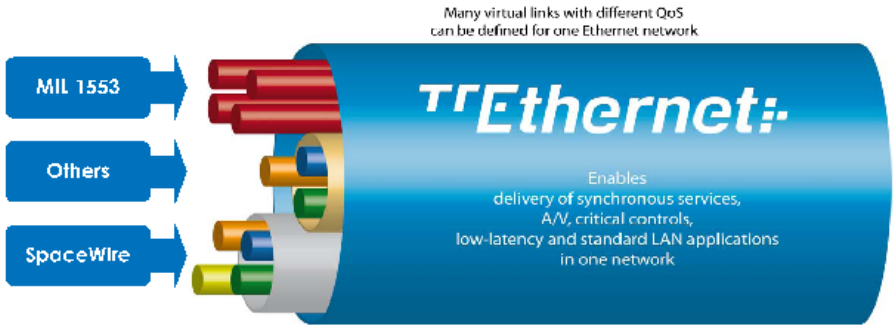
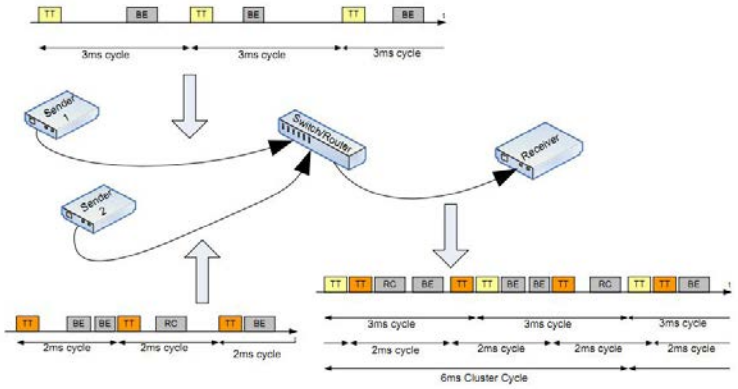
The Reliable Deterministic Network

- High data rate (>1 Gb/s)
- Different classes of communication protocols
  - Time-triggered (Mil-Bus)
  - Rate-constraint (ARINC)
  - Best effort (LAN/SpW)
- Time synchronization over network





Detailed Talk by Bülent Altan

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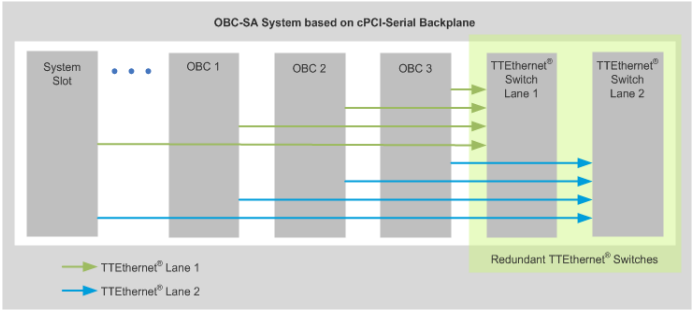
OBC-SA developed a TTEthernet Switch

- **TTE Switch (available)**
  - **12 x 1 Gbit/s full-duplex Ethernet via rear I/O (100Base-Tx/1000Base-T)**
  - 24 Gbit/s cross-sectional bandwidth (12 x full-duplex Ethernet links)
  - 1.5 Mbit on-chip memory
  - **TTEthernet implementation supports up to three redundant channel setups**
  - CompactPCI® Serial (PICMG® CPCI-S.0) peripheral slot
  - Size: 160 x 115 x 30 (in mm)
  - Weight: 500 g
  - Power consumption: <12 W typ.



SpaceWire and D-SpaceWire/Spacefiber

SpaceWire is part of OBC-SA phase 3

Advantage of SpaceWire

- Backward compatibility towards existing equipments / systems
- Do we always need 1 Gbit/s ?

Disadvantage of SpaceWire

- Not deterministic
- Up to now only 100 Mbit/s

Advantage of D-SpaceWire

- Determinism
- Second source compared to TTE
- Large amount of existing space qualified H/W
- ESA heritage

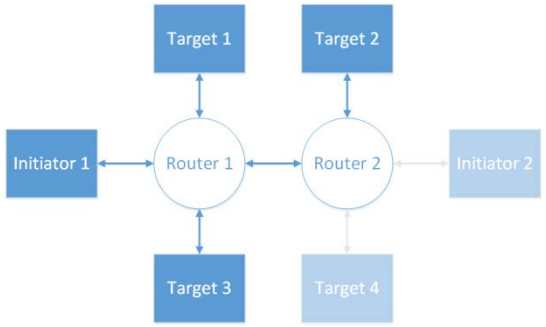
Disadvantage of D-SpaceWire

- Up to now only 100-200 Mbit/s

OBC-SA would need D-Spacefiber !

Example of a virtual bus with three targets and five links

Picture form 1)



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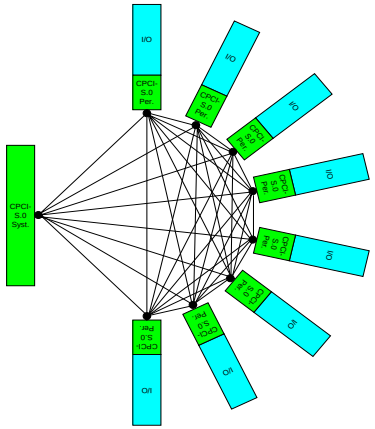
CompactPCI Serial as backplane standard

- **Standardized by PICMG (CPCI-S.0 R1.0)**
- Improve well-established industrial CompactPCI® specification with modern serial interfaces (PCI Express, SATA/SAS, USB and Ethernet) instead of parallel PCI bus.
- **Connector for high-speed serial interfaces (>10Gb/s)**
- The mechanical design is fully backward compatible to CompactPCI® and will interoperate with existing systems.
- **Hybrid backplanes with other CompactPCI® standards possible ➔easy migration**
- 3U and 6U boards are supported with focus on 3U ➔ less mass, volume
- CompactPCI® Serial does not need special infrastructure hardware ➔ less cost, effort, mass, etc.
- **Backplane is fully passive ➔reusable for different projects**



Space CompactPCI Serial standardization

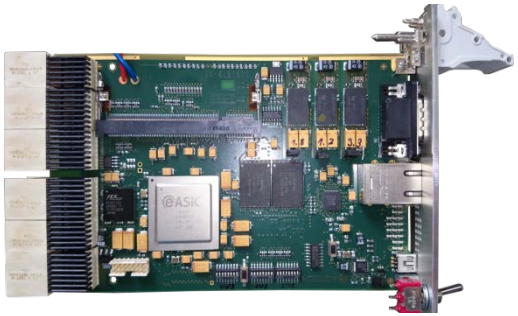
- **PIGMG working group established standardizing this new Space extension: Space CompactPCI® Serial**

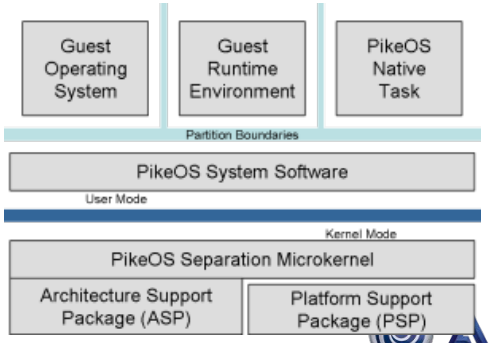
- **Features of Space extentsion**:
  - Fully backwards compatible to CompactPCI® Serial
  - **Improved by safety mechanisms like switched power, additional reset lines, space I/Fs, etc.**
  - Mechanical box and external connectors not covered to keep flexibility to different applications

- **Advantages to SpaceVPX:**
  - Backplane clearly defined (interfaces and functions of slots) ➔ reusable backplane projects
  - No utility module required ➔ less complexity, less costs
  - Pin assignment clearly defined ➔reuse of different modules
  - Connectors clearly defined (as not in SpaceVPX)
  - Connectors less complex and less expensive

Contact : friedrich.schoen@fokus.fraunhofer.de

Technology Demonstrator for OBC-SA Phase 2





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Outline

Current avionic technologies

Avionic ingredients for new designs (Phase 2)

Future consolidated system architectures (Phase3)

Gefördert durch:
Bundesministerium für Wirtschaft und Energie
aufgrund eines Beschlusses des Deutschen Bundestages

Deutsches Zentrum für Luft- und Raumfahrt

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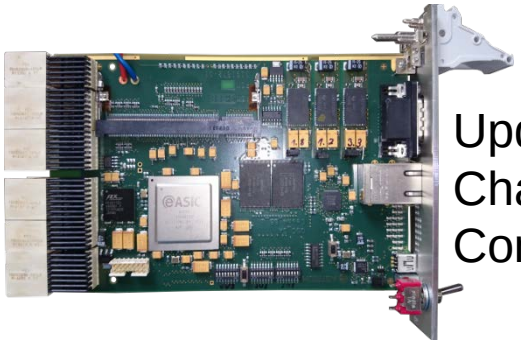
Consolidation of all existing technologies into OBC-SA Phase 3



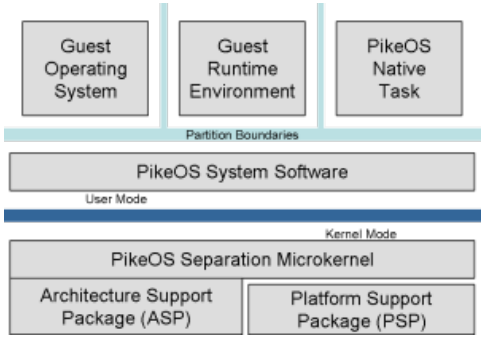
Update with GR740
Change to SRAM
Connect SpW

Adapt design to thermal requirement

Implement SpW
ProASIC4
S1260 voting

Full cPCIs comp.

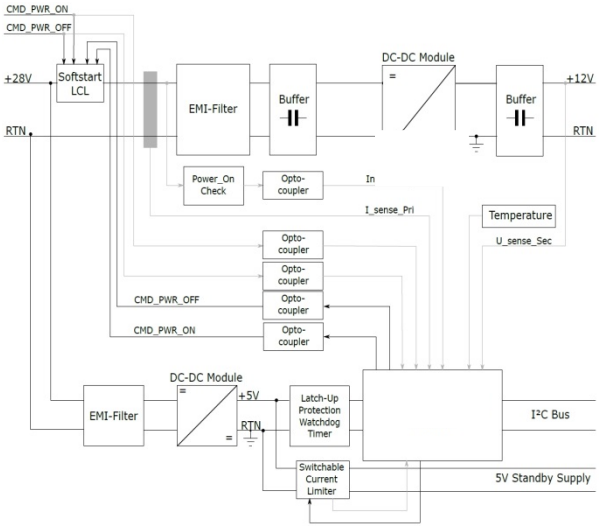
Use radhard FPGA



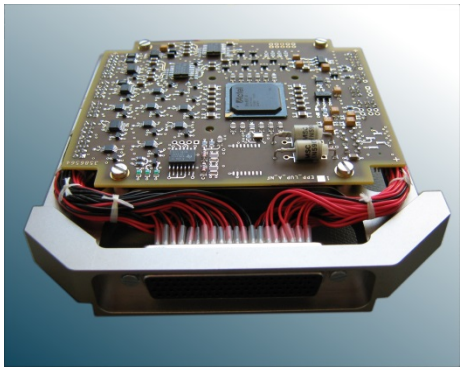
Implement SpW.

ÔBC-SA Phase 3 Box, Power and Latch up Protection Module

Preliminary mechanical housing



Preliminary PCDU design



Preliminary LuP Module

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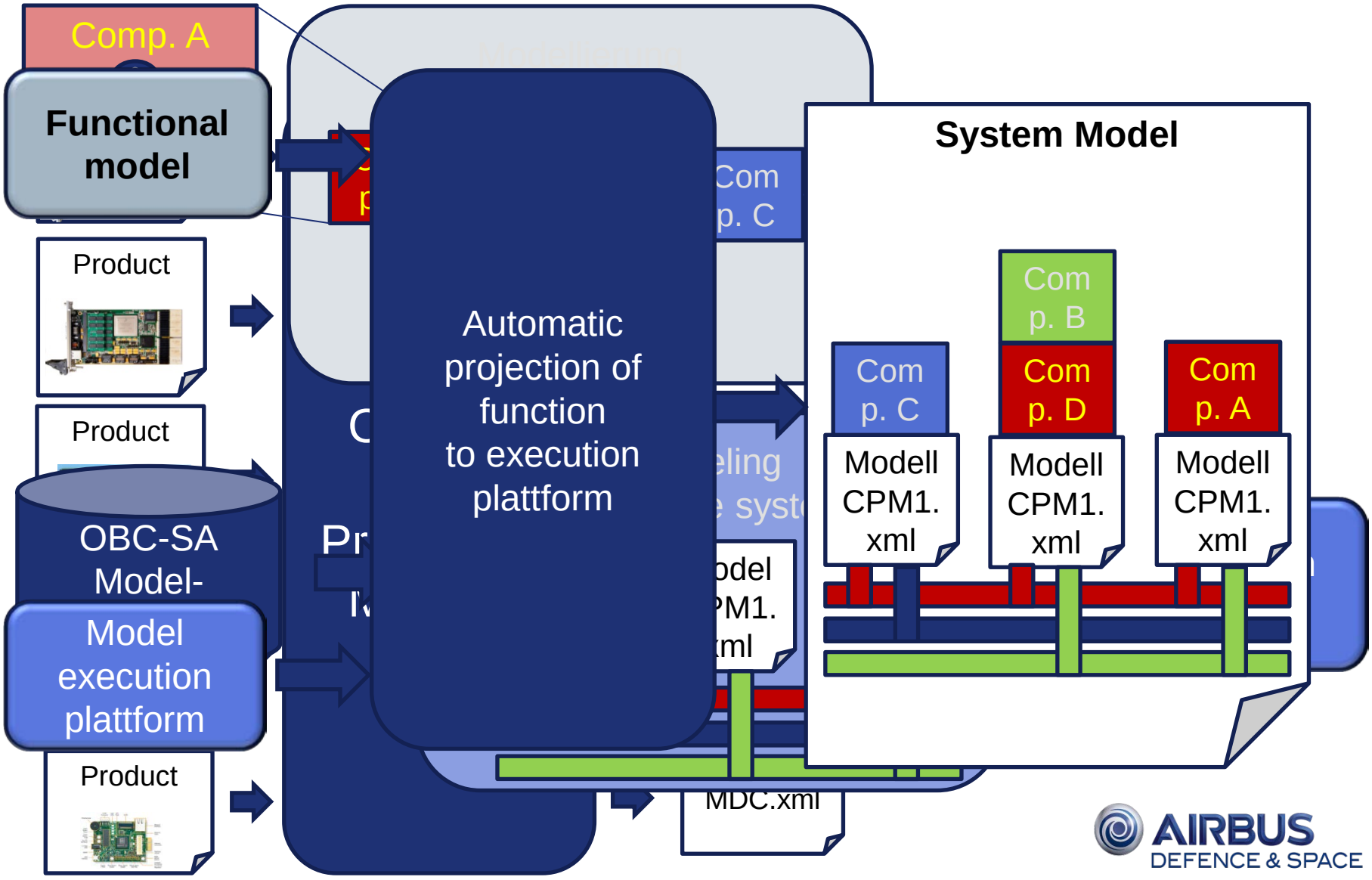
Modelling OBC-SA products for MBSE usage during phase 3



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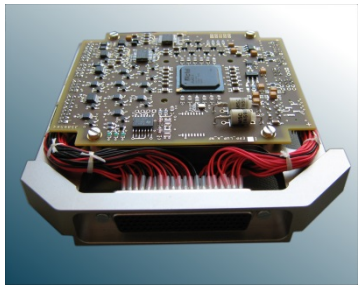
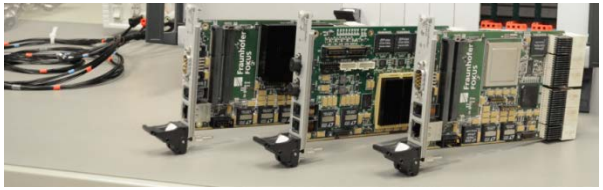
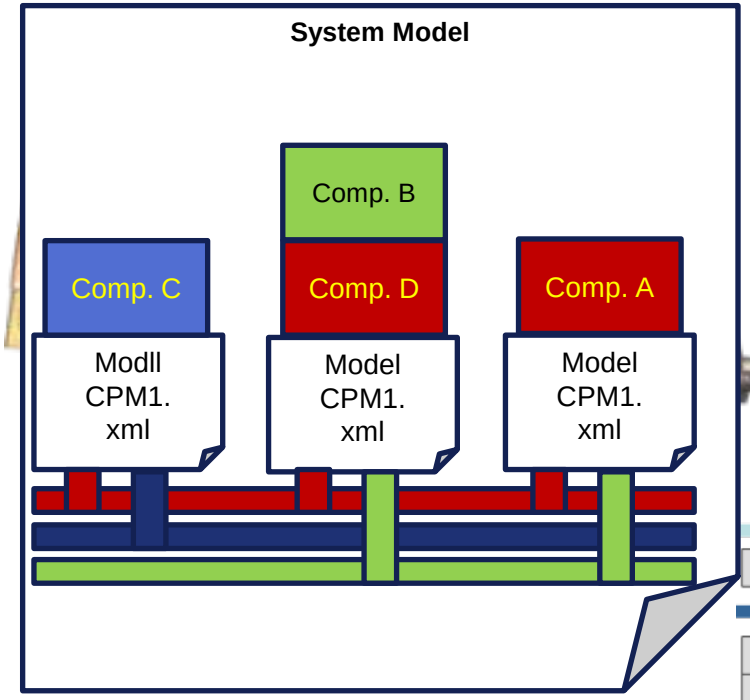
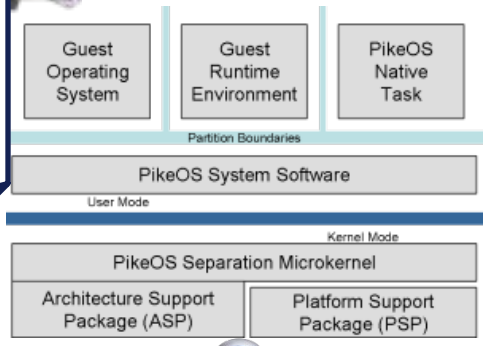
Consolidated technologies and new parts in OBC-SA Phase 3









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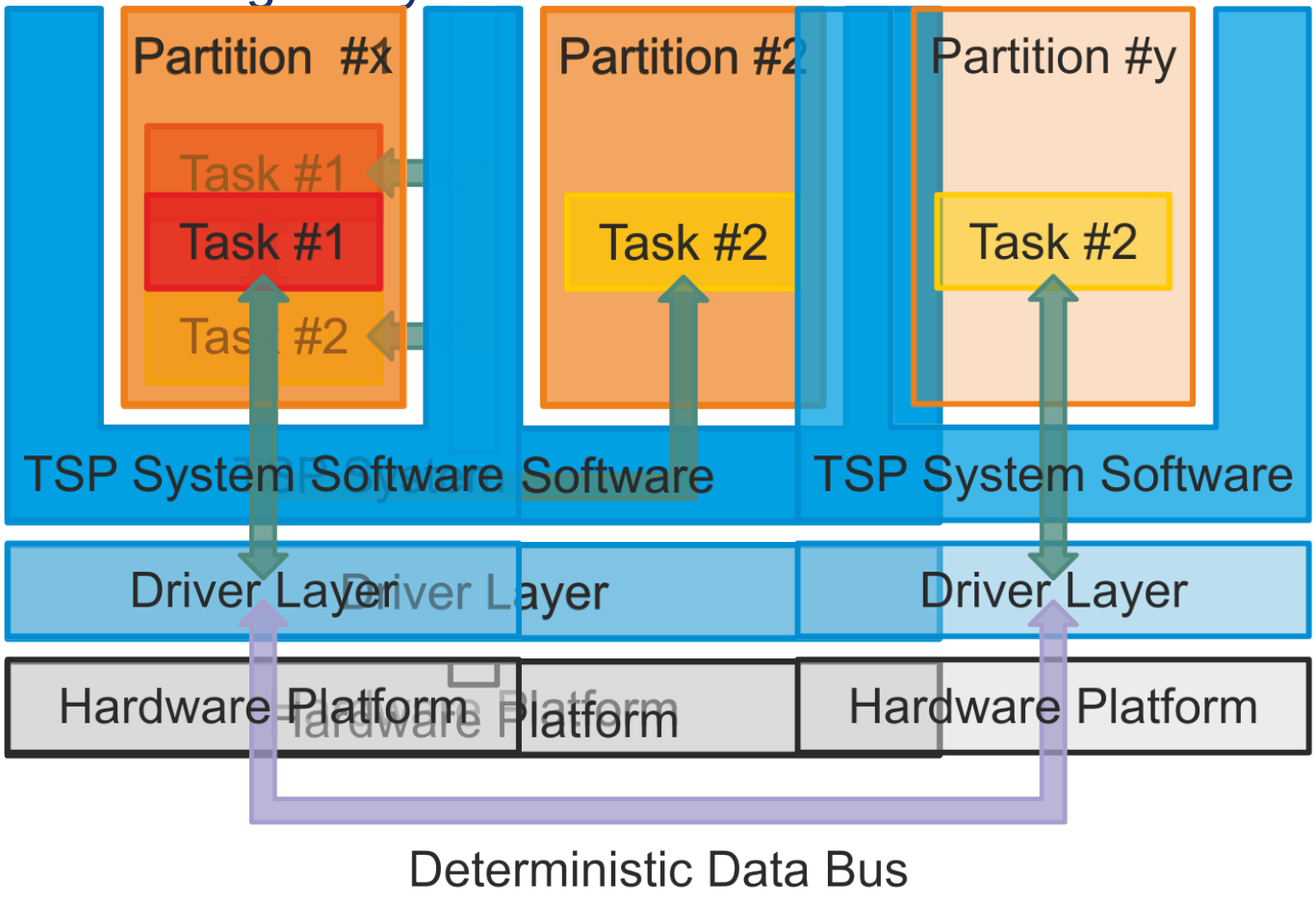
Distributed Integrated Modular Avionics (D-IMA)

The next step towards cooperation on complex and robust autonomous spacecraft's

Distributed IMA is Aiming on:
Autarkic intelligent systems



Conclusion

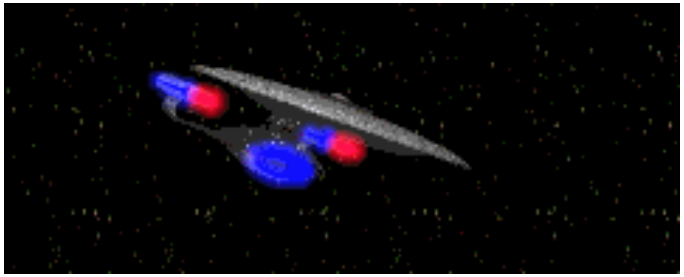
OBC-SA could be part of the **next logic** step towards a high performant and reliable space system

Factors for **our** success are:

- Standardised interfaces and open specifications
- Variety of hardware, software and tools
- Participation of a large user base, **like you**
- Space authorities **acceptance**

Gefördert durch:
Bundesministerium für Wirtschaft und Energie
aufgrund eines Beschlusses des Deutschen Bundestages

DLR



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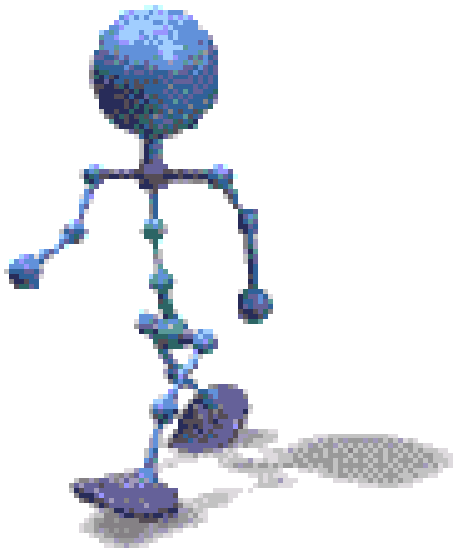
Thank You !



Questions

DLR AIRBUS DEFENCE & SPACE STI SYSGO EMBEDDING INNOVATIONS TTTech Ensuring Reliable Networks Fraunhofer FOKUS essei