Final Presentation

Single Board Computer Core Phase 2

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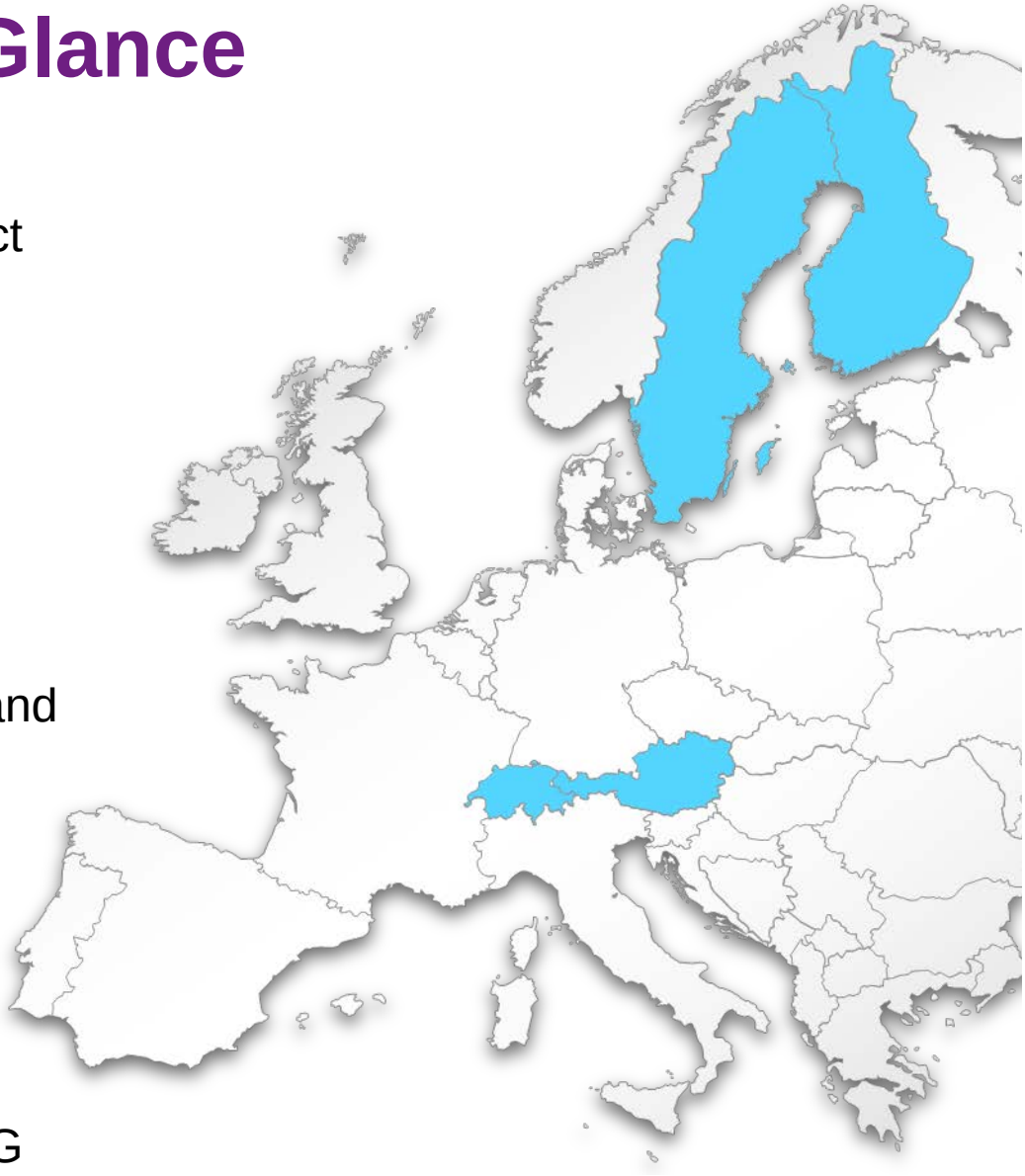
RUAG Space at a Glance

- Leading European space product supplier to the industry
- Acquisition of Saab Space and Austrian Aerospace (2008), Oerlikon Space (2009), Patria Space (2015)
- Eight sites in four countries (Switzerland, Sweden, Finland and Austria)
- US office in Denver, Colorado
- 1180 employees
- Total revenues (2014): 265 M€
- Headquarters: Zurich (CH)
- This activity carried out by RUAG Space AB in Gothenburg, Sweden



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RUAG Space AB, Sweden - RSE

Headquarters and center for Computer Systems, Antennas and Microwave Electronics: Göteborg, Sweden

Mechanical systems
Linköping operations, Sweden

2014:	
Sales:	785 MSEK, 86 MEuro, 115 MUSD
No of employees:	374

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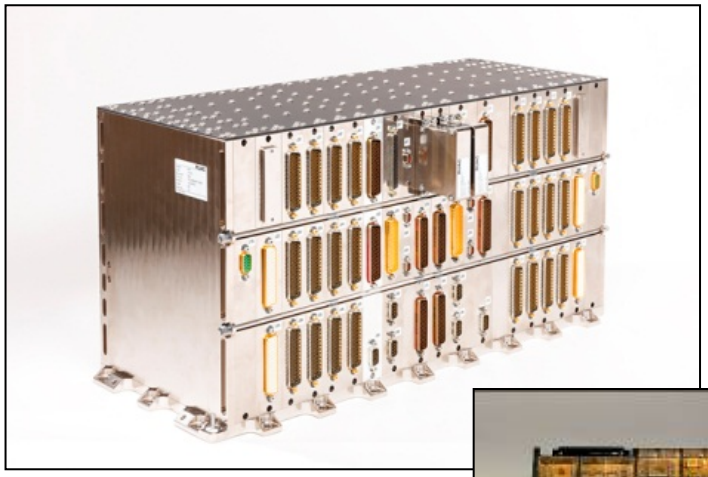
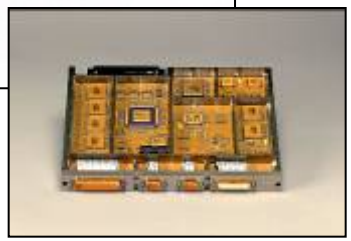
RSE Product Areas





Computer Systems

Adapters and separation systems

Satellite Structures

Antennas

Frequency Converters & Receivers

Single Board Computer Core Needs

- RUAG is a major European supplier of On-Board Computers (OBCs) and Spacecraft Management Units (SMUs)
- The next generation computers requires
  - new and updated functionality since standards and mission needs evolve with time
  - reduced weight & volume
  - reduced power consumption
  - reduced cost

Evolution of Standards

- New CCSDS recommendations on security, CCSDS 355.0-R-3
  - Includes Transfer Frame Header in the MAC computation
  - Separate security headers and security trailers
- Updated SpaceWire standard, ECSS-E-ST-50-12C Rev1
  - Changed definition of Time Codes
  - Introduction of Distributed Interrupts/Distributed Interrupt Acknowledge
- Upcoming SpaceWire standards
  - SpaceWire-D
  - SpaceWire Time Distribution

Evolution of Mission Needs

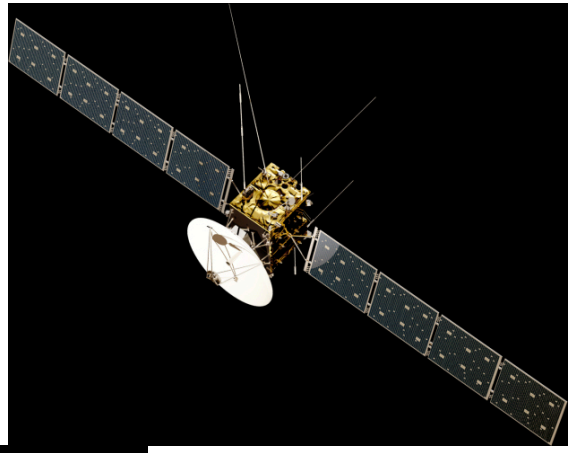
- More memory
  - Increased size of processor execution memory as well as software storage memory
  - Larger mass memory with non-volatile capability
- File based operation
  - Introduction of CCSDS File Delivery Protocol
- More SpaceWire links
  - SpaceWire used for both platform and payload
- Specific missions need more processing performance

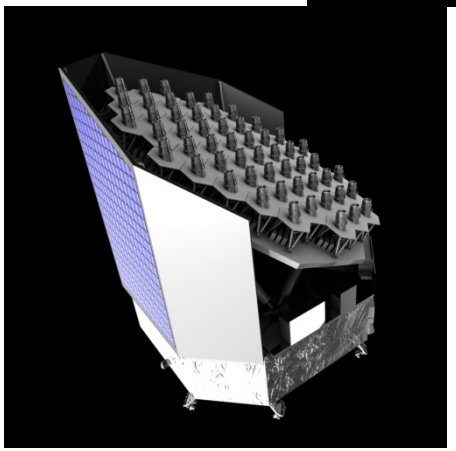
Single Board Computer Overview

- The Single Board Computer Core (SBCC) is a major evolution of the OBC and SMU
- The SBCC integrates all functions and interfaces needed for an OBC or an SMU core on a single board
- Large Instrument Control Units will also benefit from SBCC, allowing synergies between data handling and instrument control computers
- The SBCC improves the OBC and the SMU core (since an SMU is an OBC plus I/O modules in one unit)

SBCC Target Missions

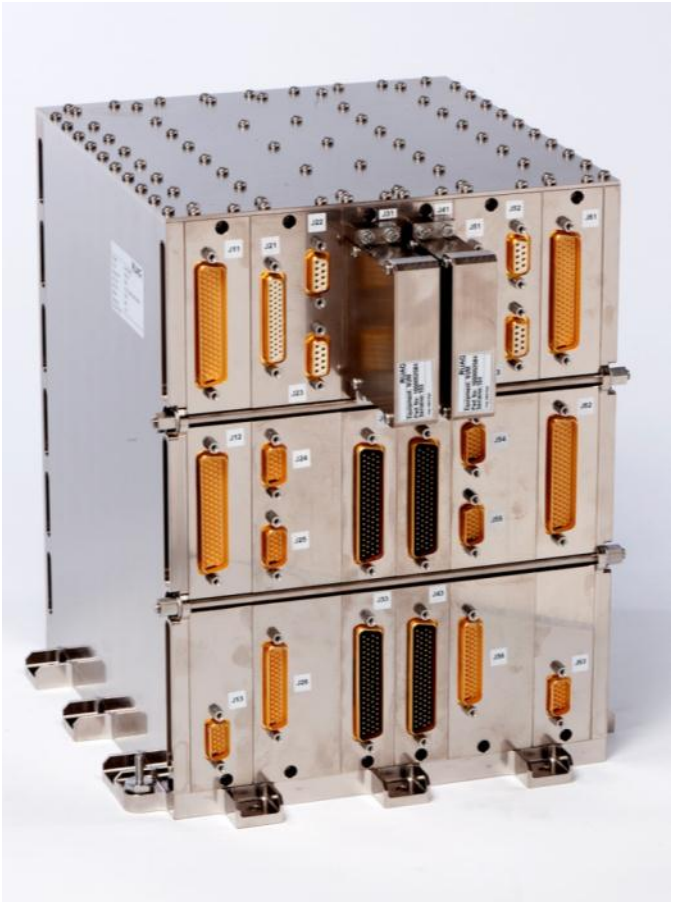
- Future ESA constellation, earth observation & science missions
  - Juice, Plato, Athena, FLEX/CarbonSat, upcoming Mars and Planetary Exploration missions, Galileo Next, future Instrument Control Units …
- Future commercial telecom and earth observation satellites
- Emerging markets
  - Non-European Programmes
  - Integrated Avionics
- Synergies with launcher computers





Current OBC Concept

- Two digital boards per redundant OBC half; TTRM & PM
- TTRM = TM, TC, RM & MM:
  - Telecommand (TC)
  - Telemetry (TM)
  - Reconfiguration
  - Small Mass Memory
  - Two ASICs: CROME and HAMSTER
- PM = Processing Module:
  - LEON Processor
  - Control interfaces: MIL-STD-1553, SpaceWire, UART…
  - One ASIC: COLE
- Power board with High Priority Commands



SBCC OBC Concept

- One digital board per redundant half
  - Combines and extends the functionality of the previous TTRM and PM boards
    - One System-on-a-Chip ASIC: CREOLE
  - Single board benefits
    - Reduced cost due to fewer components and lower manufacturing cost
    - Less weight & volume
    - Lower Power Consumption due to higher integration
- One power board per redundant half
  - Includes interfaces for High Priority Commands and Synchronisation signals

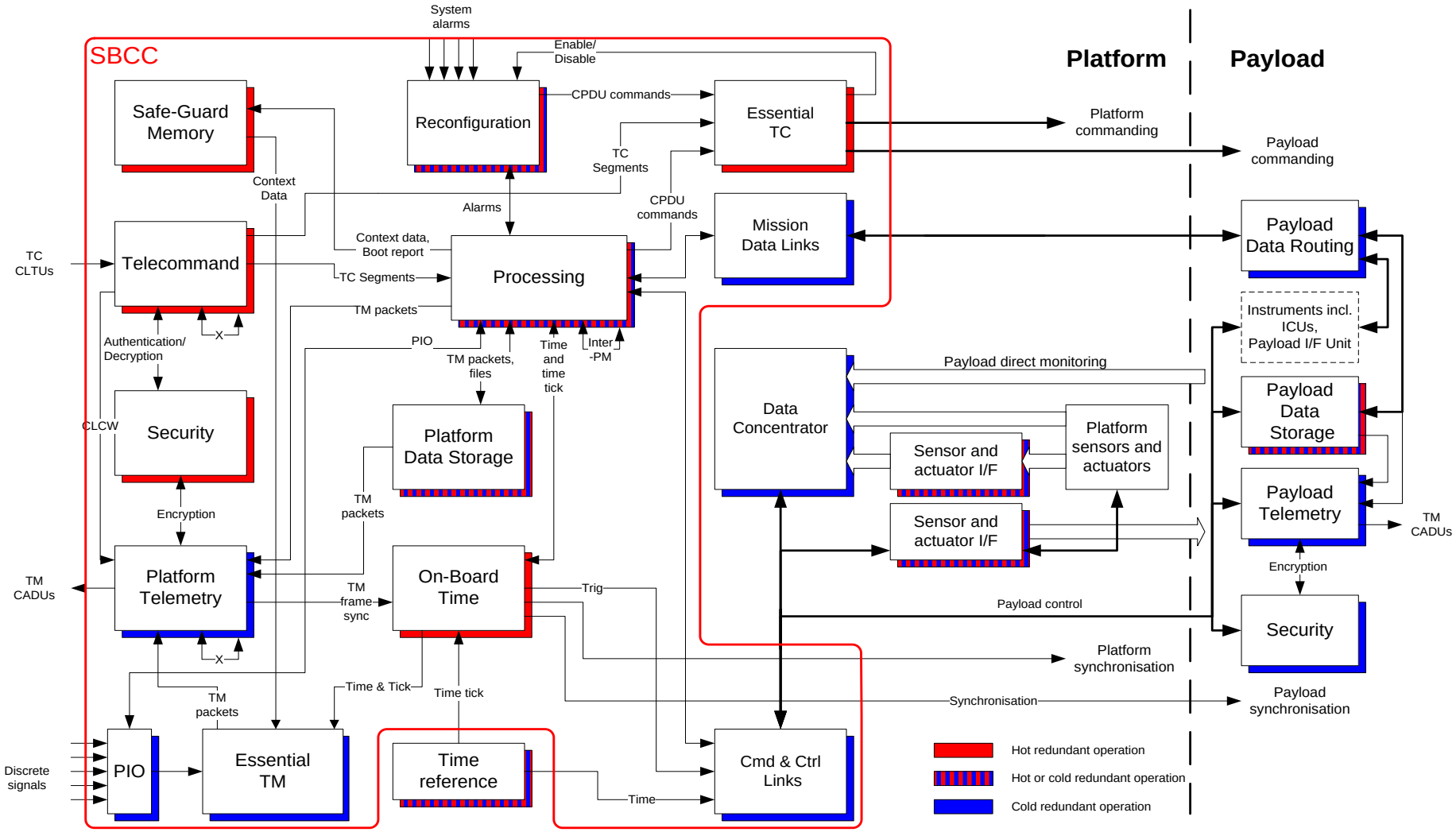
SBCC OBC Concept, cont'd

- Compliant with SAVOIR Avionics System Reference Architecture (ASRA) Generic OBC Specification
- Support for On-board Software Reference Architecture (OSRA) and IMA/TSP
- Support for non-volatile Data Storage and prepared for CCSDS File Delivery Protocol (CFDP)
- Software interface has been kept as intact and compatible as possible
- Prepared for increasing performance significantly through additional add-on processor connected through high-speed serial link, such as the next generation Micro-Processor (NGMP), or Field Programmable Gate Array (FPGA) for hardware acceleration

Results at end of SBCC Phase 2

- SBCC development has been divided into three separate phases
- Results at end of Phase 2:
  - Consolidated SBCC system concept and architecture
  - Single Board Computer Core development board with standard OBC interfaces and CREOLE baseline design implemented in an FPGA
  - New and enhanced functionality, with corresponding driver software
  - CREOLE flight design ready for ASIC implementation
  - Verification through simulation at module and chip level
  - Validation at System-on-Chip level in FPGA
- Final Phase 3 result is validated CREOLE ASIC on SBCC board

SBCC Functionality



SBCC Functionality, cont'd

- Standard Interfaces:
  - CCSDS Packet Telecommand and Packet Telemetry
    - Includes both Essential TC and Essential TM
  - Legacy MIL-STD-1553 and CAN
  - A large number of Deterministic SpaceWire interfaces with Time Codes
  - Synchronisation signals with programmable output frequencies

- Core functionality
  - Processing with FDIR support by a Reconfiguration Unit
  - Flexible Encryption and Authentication implementation, also supporting external Encryption/Authentication units
  - On-Board Time handling and Synchronization
  - Non-volatile Mass Memory
  - Merging of memory buses, oscillators & reset management reduces external component count

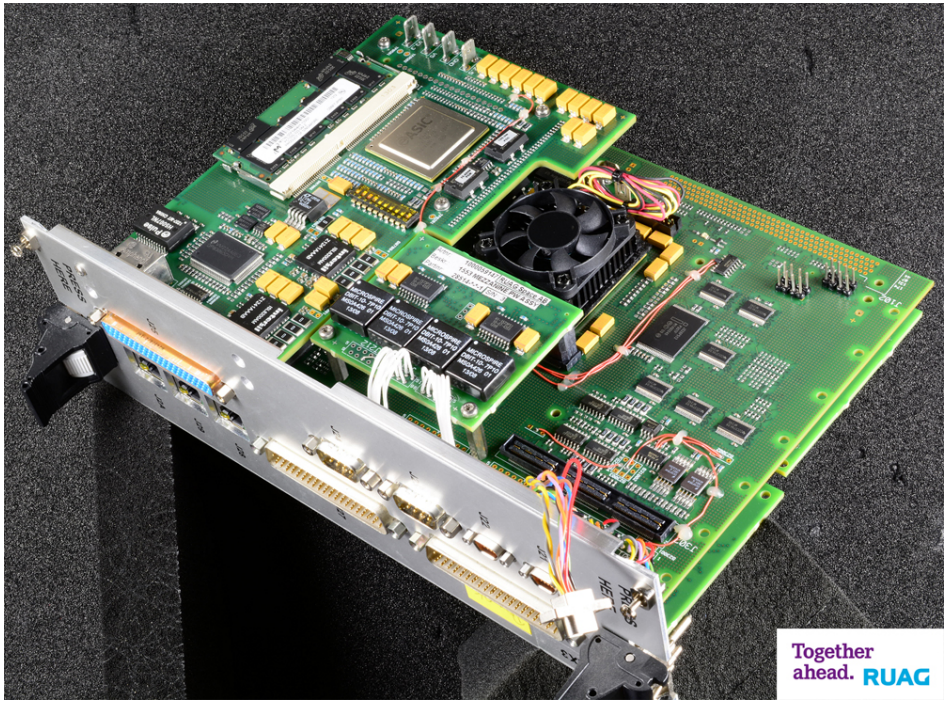
SBCC Functionality, cont'd

- Software aspects:
  - LEON processing
  - Large memory sizes can be accommodated
  - Hardware support reducing processor response times for interfaces
  - Ethernet-based Enhanced Debug Support Unit with real-time tracing capability, with corresponding LEON Tools suite for efficient software development
  - Maintaining SW as compatible as possible reduces cost for software redevelopment by customers

- Flexibility and Scalability
  - Network on Chip for extendibility and flexibility
  - Add-on powerful processor or FPGA

Multi Functional Core (MFC) Breadboard

- Prototype development FPGA board used for SBCC validation
- Standard OBC interfaces
  - TM, TC, Alarms, some IO
  - MIL-STD-1553, CAN
  - SpaceWire
- NGFP Add-on Processor Mezzanine
- Mezzanine connectors for functional growth & expansion
- Enhanced debug support unit with Ethernet connection
- Used by a large number of projects



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Summary

- RUAG Space is on track for the next generation single board computer incorporating the functionality of current OBCs
- New and extended functionality in line with the needs of future SAVOIR, OSRA, CFDP based missions; including extensive modern SpaceWire connectivity with flexibility and extendibility, non-volatile Data Storage, scalability through add-on processing
- Maintaining the software interface and enhanced debug support facilitates software adaptation

- Integration driven approach and large team for record-breaking short development: 12 months instead of contractual 18 months
- Phase 3 work such as extra tests started while waiting for kick-off
- OBC-NG EQM foreseen early 2018, in line with schedule for next Science and Earth Observation missions

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Thank you for your attention!