

Single Board Computer Core

Prime contractor: RUAG Space AB ~ Presenters: Peter Sinander

ESA TO: Kostas Marinis

Abstract:

RUAG Space is the major independent European supplier of Data Handling Systems (DHS) and On-Board Computers (OBC) for launchers, satellite platforms, payload control and similar equipment based on advanced computer technology. In order to remain competitive and to be able to provide the European space community with a highly integrated computer core, the processor, telemetry, telecommand and reconfiguration functions needs to be integrated on a single board.

The main enabler for the SBCC is the next generation system-on-chip. In the second phase of the activity an FPGA (Field Programmable Gate Array) prototype of this chip, called CREOLE (derived from the current generation chips CROME combined with the COLE) has been further developed and consolidated into a design ready for ASIC implementation.

The development has been divided into three separate phases, where the end result will be the CREOLE ASIC (Application Specific Integrated Circuit) and corresponding software drivers that will be used for the next generation of highly integrated DHS and OBCs, targeting missions such as Juice, Plato, Galileo Next, etc.

The CREOLE integrates all major functions that form the basis of the novel generation of RUAG Space computers. Functions include a LEON fault tolerant processor, I/O controllers, on-board time, telecommand decoder, telemetry encoder and reconfiguration controller needed to support many different applications. It is foreseen to add a Flash Mass memory controller developed under a separate contract.

The CREOLE design has been validated using a flexible multi-functional FPGA breadboard called MFC (Multi-Functional Core) which includes all required interfaces and memory types supported by the CREOLE.