MINIATURISED DIGITAL HEATER CONTROLLER

G.Capuano

TEC-ED & TEC-SW

Final Presentation Days

ESA-ESTEC June 2015

Via Provinciale Pianura 2, Zona Industriale San Martino int 23 – 80078 Pozzuoli (Naples) ITALY
Tel. +39 0815263475 Fax +39 0815262701 - e.mail : info@tsd-space.it - web page : www.tsd-space.it

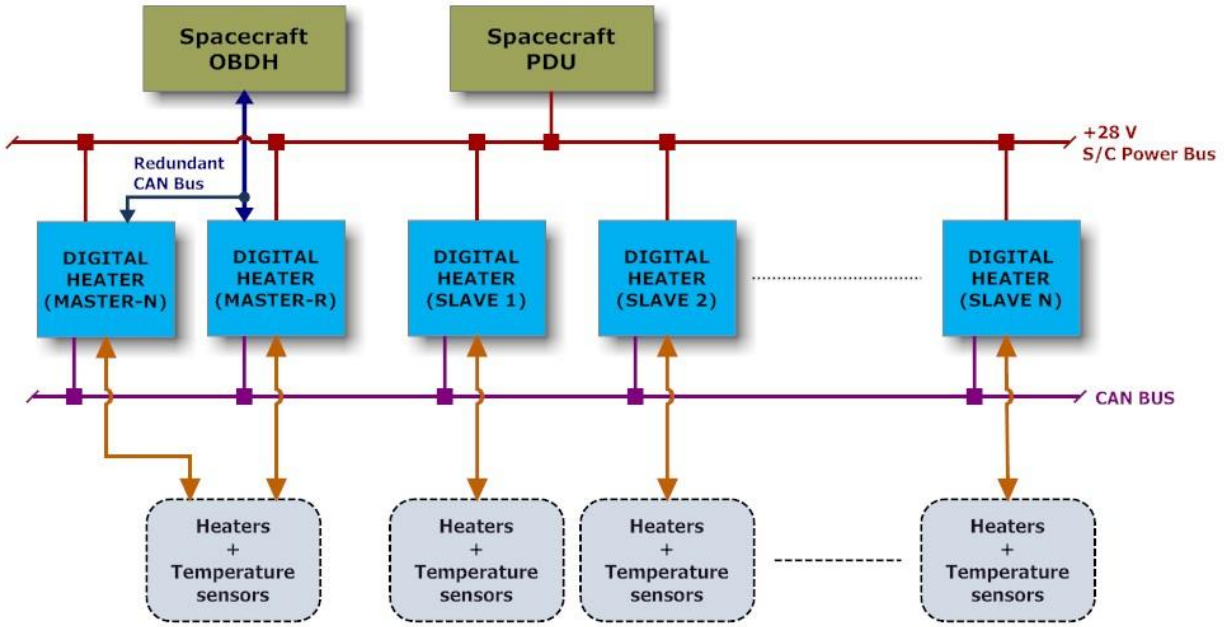
Introduction

- The digital heater controller is a module dedicated to the closed loop control of heaters for thermal Control on board Spacecraft. The module receives the desired temperature set-point from spacecraft OBDH and drives the heater so to reach an to maintain the desired temperature

- The scope of the activity is the development of a very compact electronic module to be used close to the heater and able to drive the heater in a temperature controlled way. Thanks to this electronic module, the heater can be seen externally as a digital devices and in particular as a “Digital Heater”

- The module allows the implementation of a “distributed” thermal control system and it is aimed at reducing the mass and volume of the harness that characterize traditional centralized thermal control systems on board Spacecraft

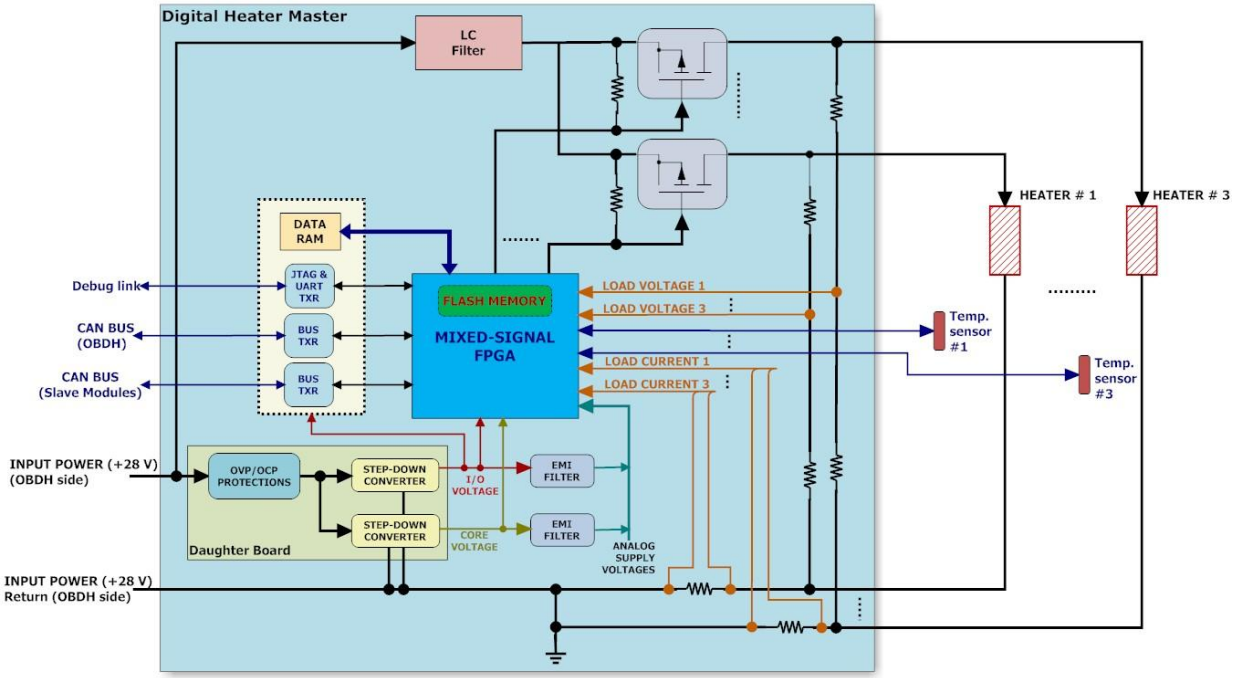
Overall Architecture



- The network consists of two master nodes (nominal & redundant) and a certain number of slave nodes
- The use of two masters is adopted to enhance the system reliability considering the case of a fault within the master node.

- Each master node performs following tasks:
  - Bus bridging and protocol conversion
  - Monitoring of the status of all the slave nodes
  - Decoding and distribution of commands issued by OBDH
  - Transmission to the OBDH of a significant subset of data produced by network nodes

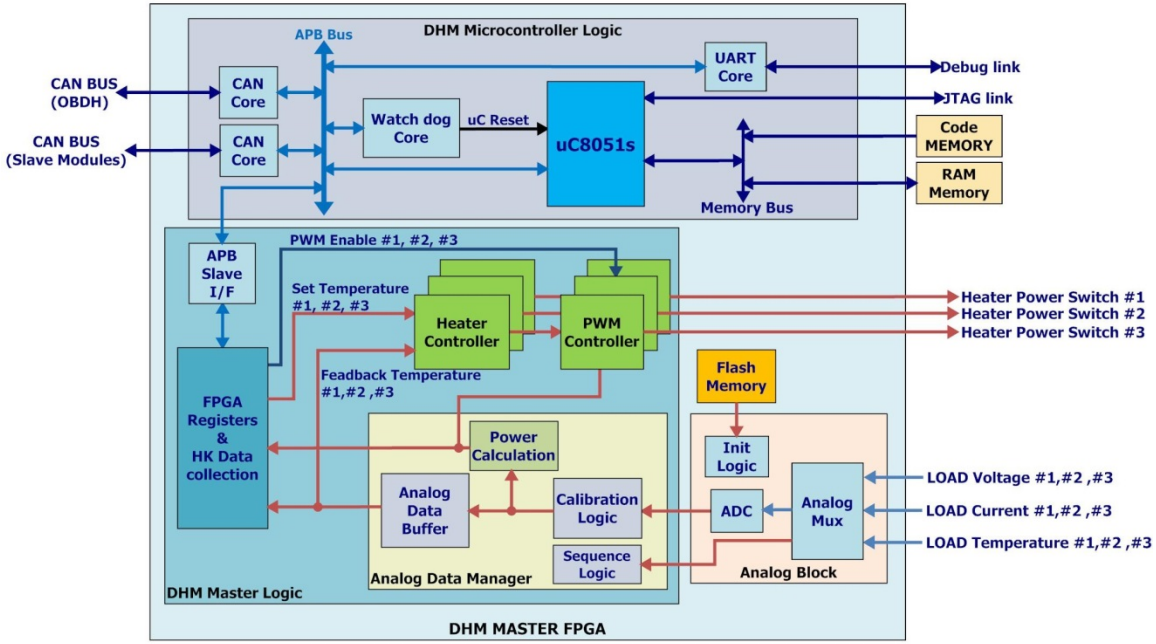
Digital Heater Master Architecture



- The master module and the slave module as well are based on a "mixed signal" FPGA belonging to FUSION family by ACTEL-MICROSEMI (AFS1500 for the master and AFS 600 for the slave)
- The adoption of a "mixed signal" FPGA is aimed at minimizing the number of components needed to implement the analog signal conditioning

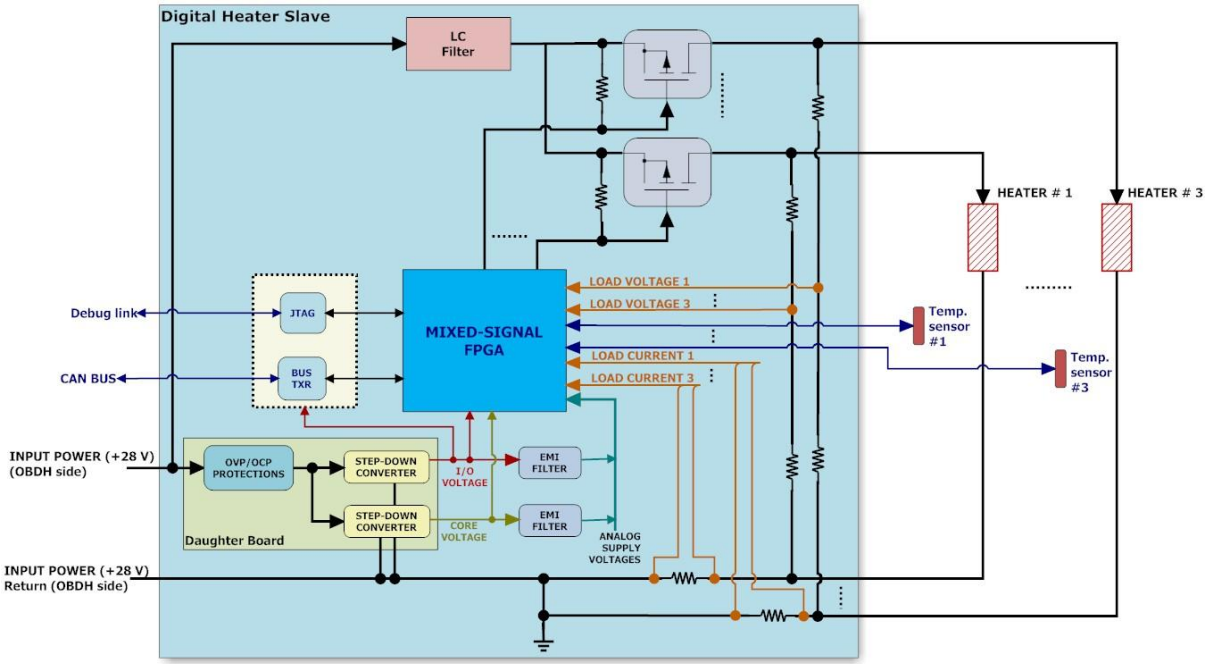
- The module consists of the following sections:
  - Power conditioning and distribution, including OVP/OCP protections and step-down regulator
  - Redounded CAN bus interface to/from OBDH
  - Redounded CAN bus interface to/from slave modules
  - Conditioning of Analog Signals (temperatures, currents and voltages
  - Power driving up to 3 Heaters based on P-channel MOSFET up to 2A (at least)
  - Temperature Control & Data acquisition

Digital Heater Master FPGA Functionalities



- The FPGA of the Master Module implements the following functionalities:
  - 8051 Soft IP core Micro-controller
  - Analog signal conditioning & 12 bit A/D converter
  - Data acquisition module
  - PI digital controller for closed loop temperature control
  - PWM signal generation for the Power MOSFET driving
  - CAN bus node controller
  - CAN to CAN Bridge
  - Storage of operational parameters into a non volatile FLASH memory

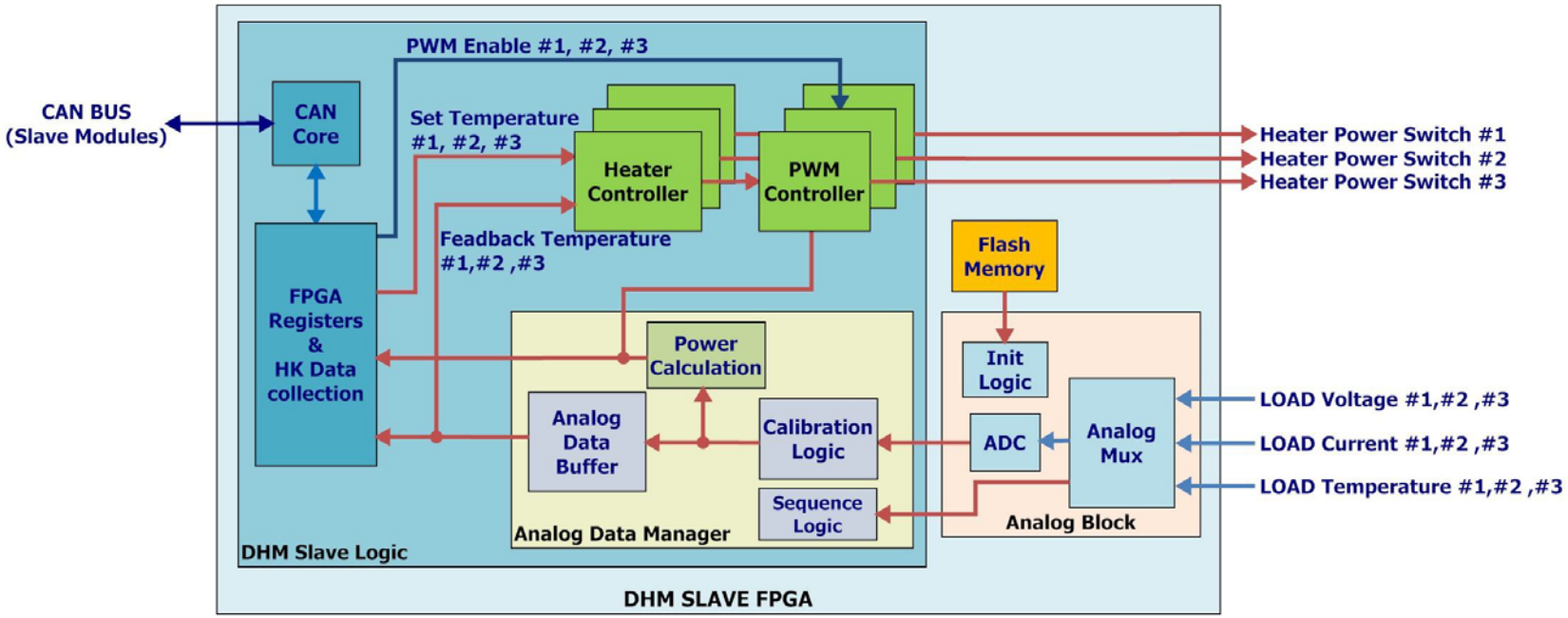
Digital Heater Slave Architecture



- With respect to the master module, the slave module is characterized by a simplified architecture
- In particular, with respect to master type, this module exhibits reduced functionalities. It is only in charge to receive configuration command via CAN bus, to transmit HK & status data and to perform heater driving in thermally controlled way

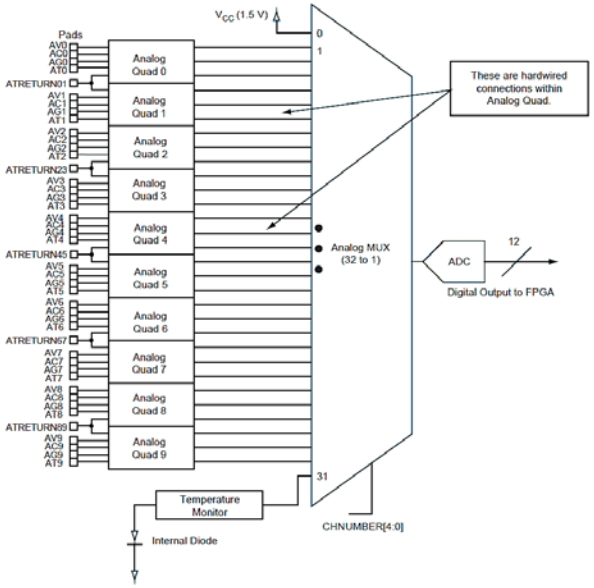
- The thermal controller is hard-wired implemented in the FPGA by means of specifically designed IP core operating with data represented in single precision; no soft IP core microcontroller is used

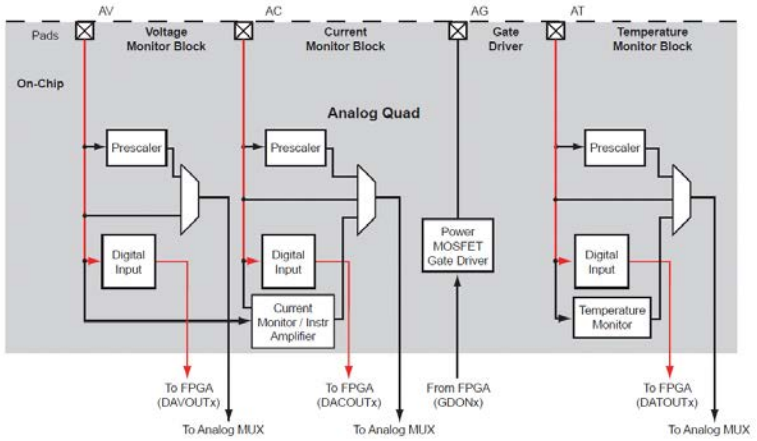
Digital Heater Slave FPGA Functionalities



- The FPGA of the Slave Module implements the following functionalities:
  - Analog signal conditioning & 12 bit A/D converter
  - Data acquisition module
  - PI digital controller for closed loop temperature control
  - PWM signal generation for the Power MOSFET driving
  - CAN bus I/F
  - Storage of operational parameters into a non volatile FLASH memory

ACTEL FUSION FPGA Analog Resources





- The FUSION FPGA is provided with a set of 10 analog signal conditioning blocks, named Quad block, that are connected to the A/D converter via a analog multiplexer

- Each analog Quad block supports the following analog interfaces:
  - Voltage monitor with dedicated configurable voltage prescaler
  - Current monitor based on instrumentation amplifier
  - Temperature monitor
  - Power MOSFET gate driver

Performances of FPGA Analog Resources

	Digital Filtered	Raw data
Accuracy	3mV (0.12%FSO)	2mV (0.078% FSO)
Mean square error	1.11mV (0.043%FSO)	6.23mV (0.24% FSO)
Linearity FSO	0.05%	0.09%

Accuracy of ADC direct signal acquisition

	Digital Filtered	Raw data
Accuracy	16mV (0.16%FSO)	17mV (0.17%FSO)
Mean square error	1.04mV (0.01% FSO)	5.51mV (0.054% FSO)
Linearity FSO	0.05%	0.08%

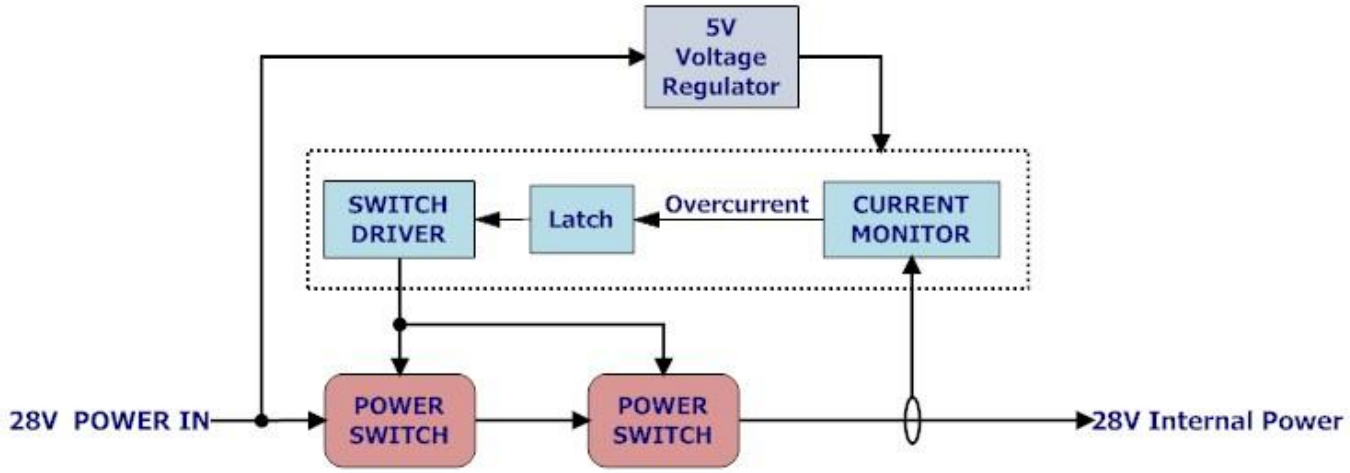
Accuracy of voltage monitoring stage

	Digital Filtered	Raw data
Accuracy	16mV (0.62%FSO)	41mV (1.6%FSO)
Mean square error	7.73 mV (0.3%FSO)	46.55mV (3.1%FSO)
Linearity FSO	0.34%	0.5%

Accuracy of current monitoring stage

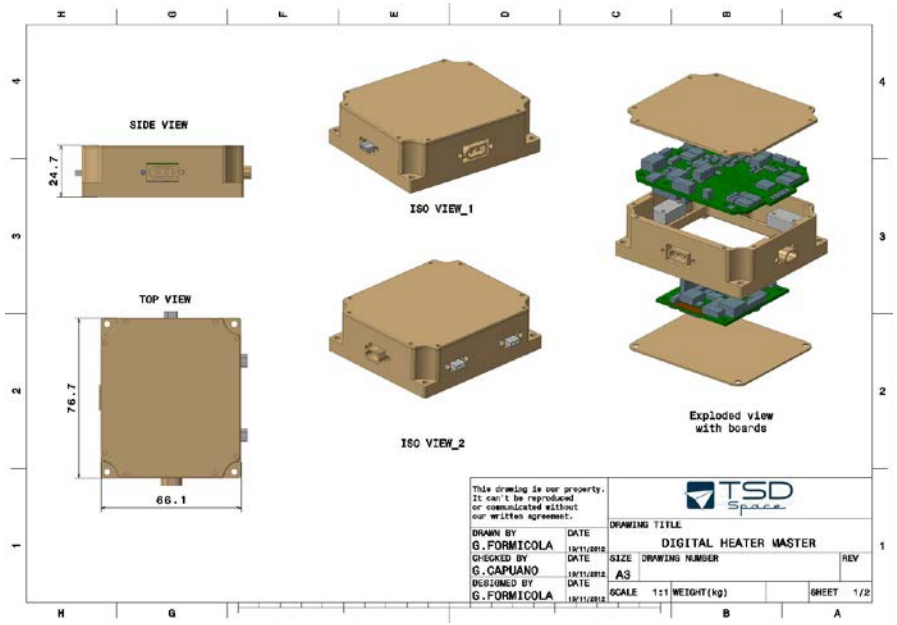
- During the component selection phase, the analog capabilities of the FUSION FPGA have been verified by running a laboratory test campaign, aimed at assessing in particular:
  - Accuracy
  - Repeatability
  - Linearity
- Reference voltages coming from a very accurate generator have been applied to the three different analog input channels:
  - ADC direct connection with a 0÷2.56V range
  - Bipolar Input with a ±5.12V range
  - Current monitoring input with a 0÷51.2mV range (gain equal to 50)
- The laboratory test results, here summarized in the tables, showed performances suitable for the specific application:
  - The ADC direct connection channel was used to acquire the temperature
  - The lower accuracy of the current monitoring channel, due to the high internal gain, results however enough for the monitoring of the current injected into the heaters

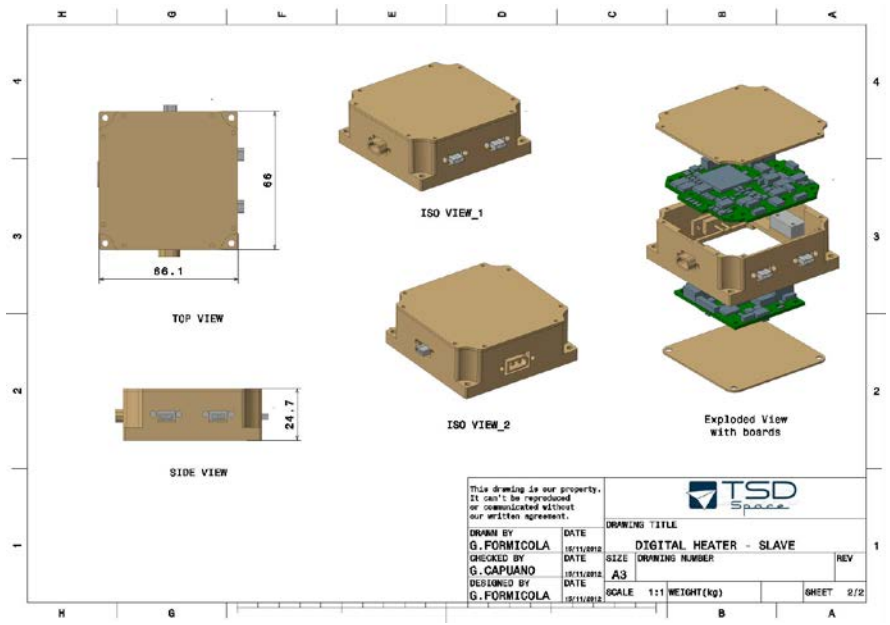
Over Current Protection



- A multi-drop topology has been adopted for the 28V power bus that supplies all the DHM present in the network
- Each DHM (master or slave) is provided with an Over Current Protection (OCP) that very quickly disconnects it from the power bus in case of overload or short circuit
- The OCP intervention is latched and the module remains powered off stays until a power cycle is performed
- The OCP is based on a hard-wired stage and it adopts a redundant power switch based on 2 P-MOSFET power switches arranged in series configuration

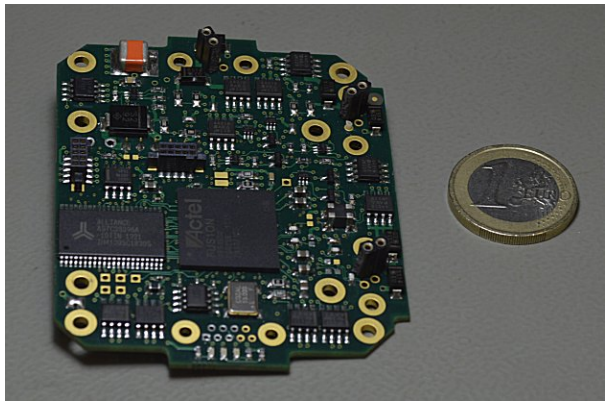
Mater and Slave – CAD Models



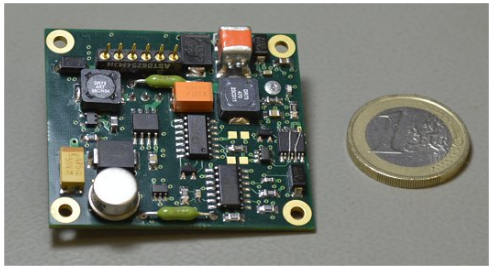


- Highly compact mechanical and electronic configuration
- Electronics distributed on a main board plus a piggyback board
- Mounting holes embedded in the main body thus avoiding mounting feet
- All the connectors (with the exception of the power one) are right angle PCB mounted connectors encapsulated into the unit structure, so to avoid internal cabling and at the same time to ensure that mechanical stresses are not transferred to the PCB

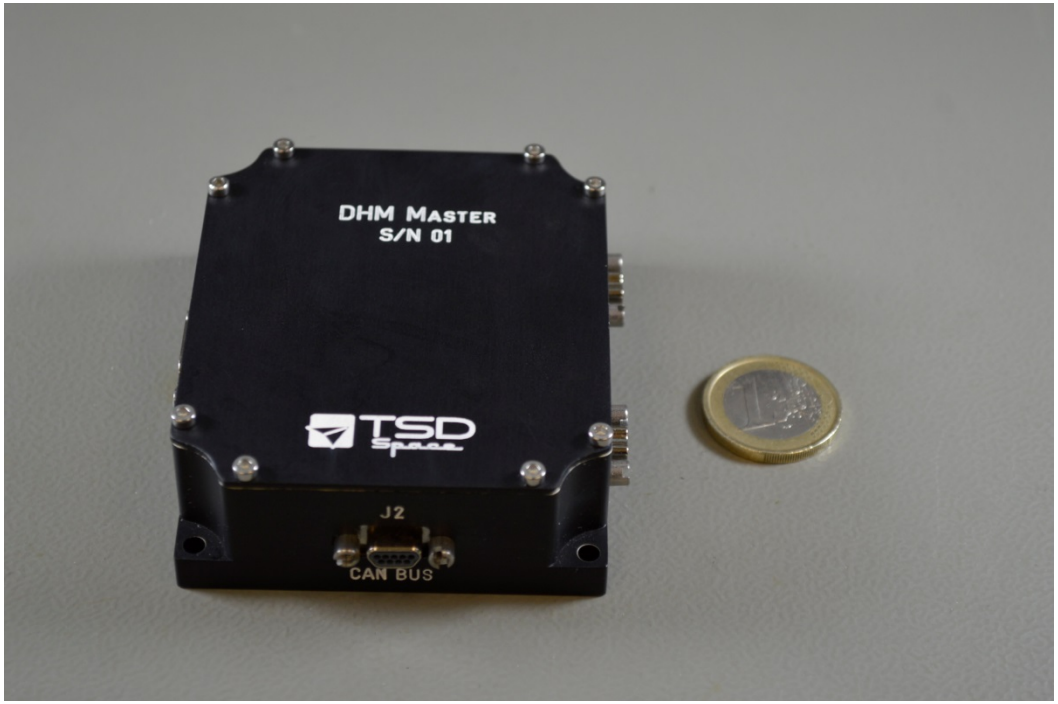
DHM Master Electronics and Enclosure



DHM Master Main Board



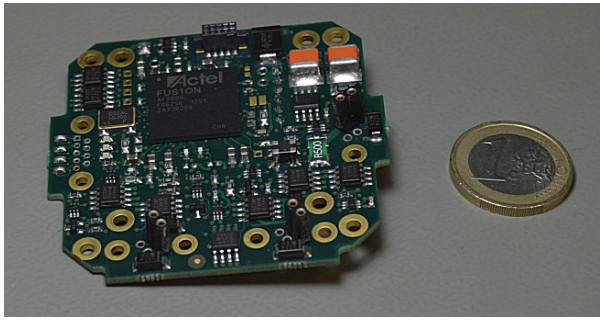
DHM Piggyback Board



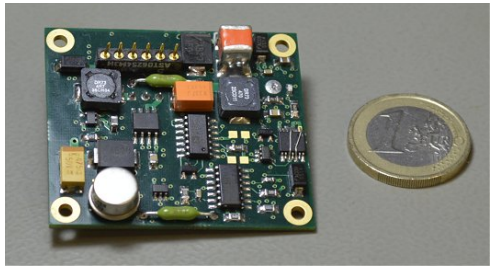
Total Mass	**169[g]**
Power	1.5[W]

- The piggyback board is the same for both the master and the slave modules
- It is placed in a free volume that arises due to the presence of the right angle PCB connectors located on the main PCB.

DHM Slave Electronics and Enclosure



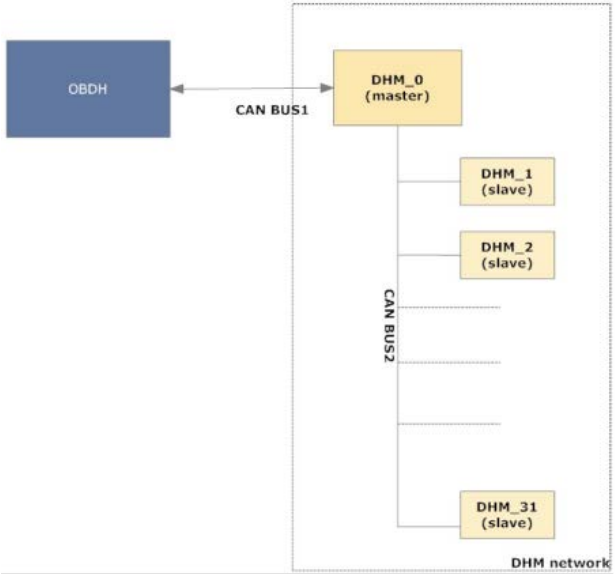
DHM Slave Main Board



DHM Piggyback Board

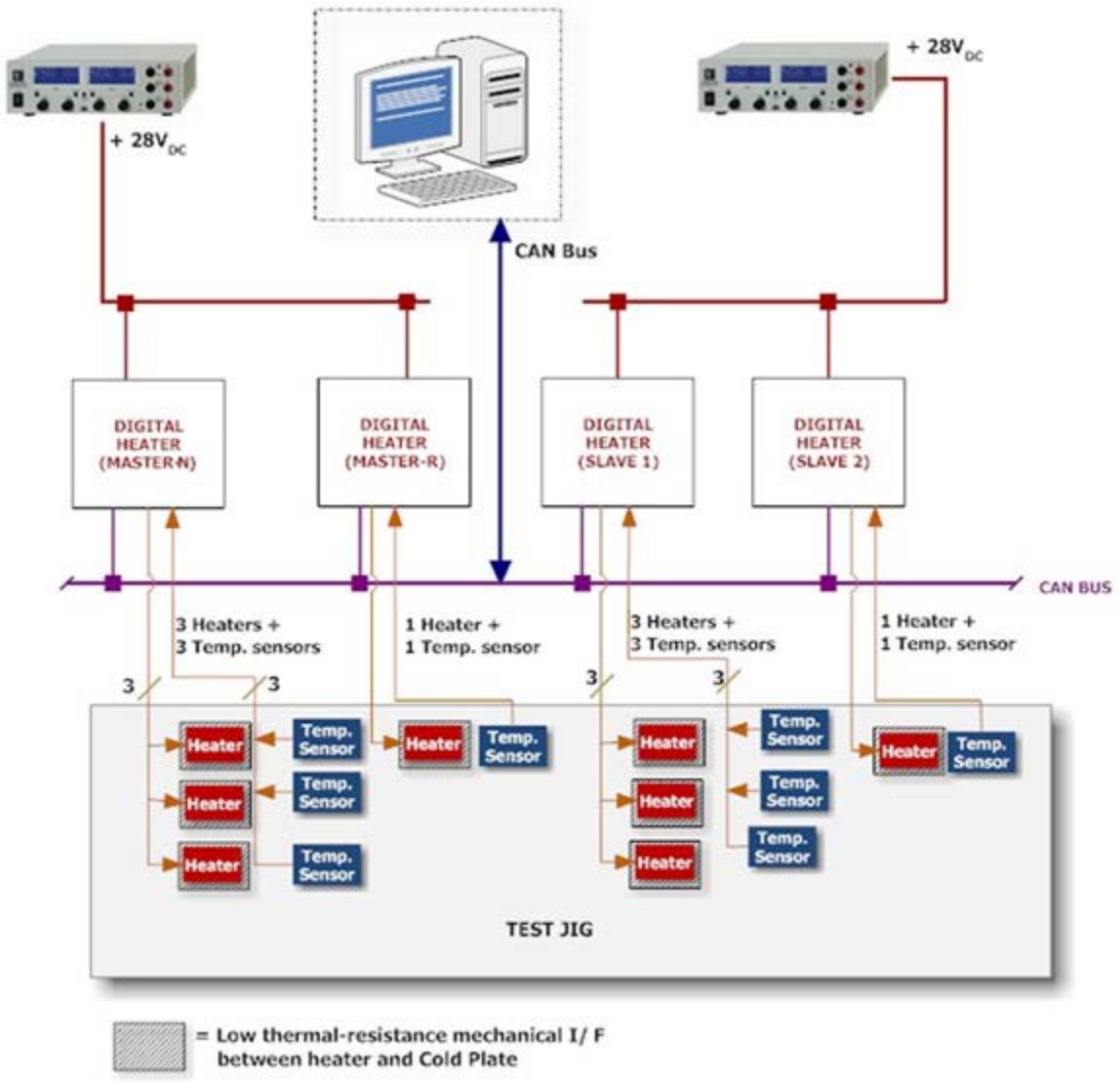
Total Mass	**158[g]**
Power	1[W]

Communication Buses and protocols



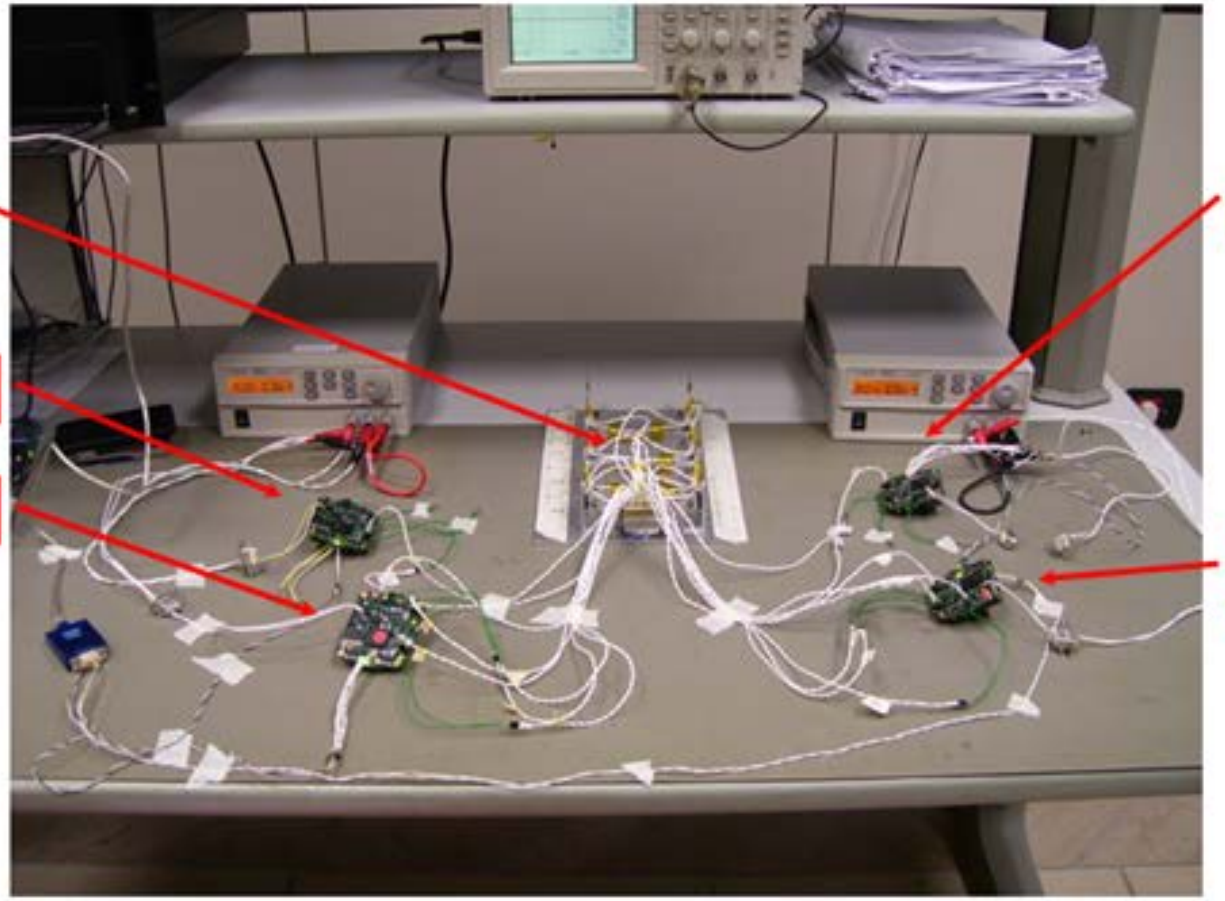
- The DHM master communicates with the OBDH over CAN BUS1 (external CAN bus) and with up to 31 DHM slaves over CAN BUS2 (internal CAN bus)
- The communication over the internal CAN bus (CAN2) is usually performed at higher rate w.r.t. the communication over the external CAN bus (CAN1). The master DHM requests HK data at 10Hz to all the connected digital heaters.
- The OBDH typically can request the master DHM to:
  - Enable/Disable the temperature control
  - Set the temperature set point
  - Receive digital and analog telemetry (status, temperature, power, …)
  - Upload/Retrieve the current DHM configuration
- The master DHM in turns requests the slaves DHMs to:
  - Give evidence of their availability (heartbeat)
  - Enable/Disable the temperature control
  - Set the temperature set point
  - Receive digital and analog HK data (status, temperature, voltage, current, …)
  - Upload/Retrieve the DHM configuration
- The request can be addressed to a single slave digital heater or a set of them
- For sake of commonality the high level message protocol is the same for the two buses.

Test Set-up



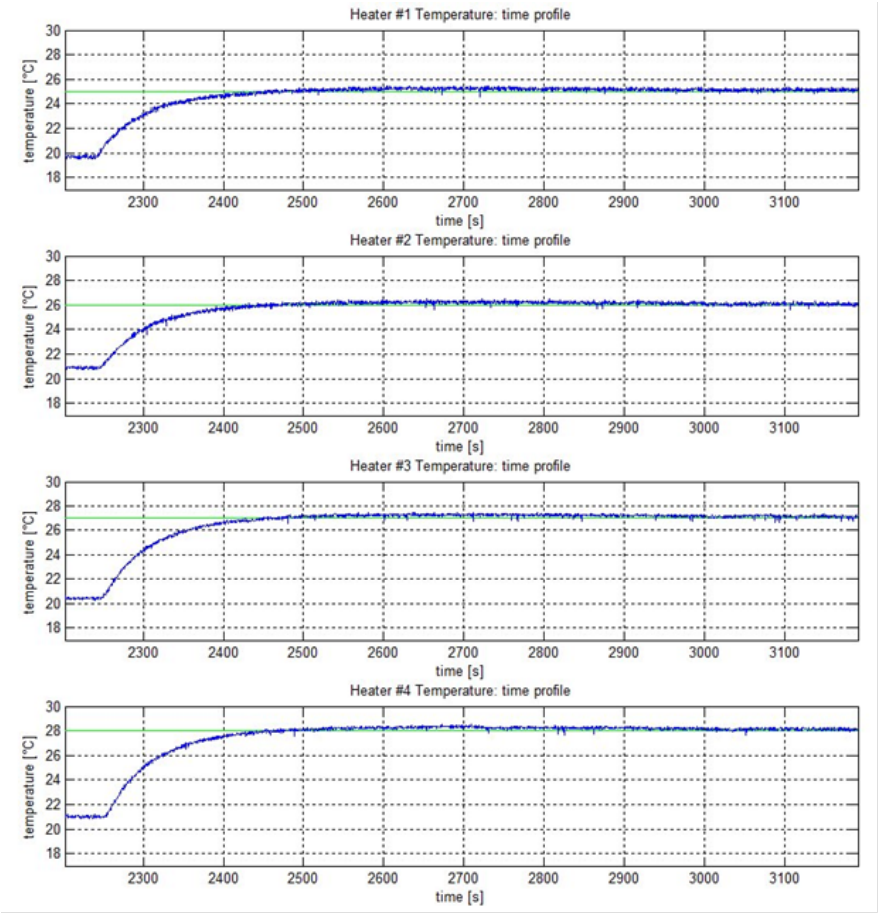
- The test set-up has included the following items:
  - One PC workstation simulating the OBDH
  - One 28V power supply simulating the Spacecraft EPS
  - Two (nominal and redundant) master modules
  - Two (nominal and redundant) slave modules
  - Set of heaters and temperature sensors properly interfaced to independent thermal loads
  - One Temperature data acquisition system with independent temperature sensors

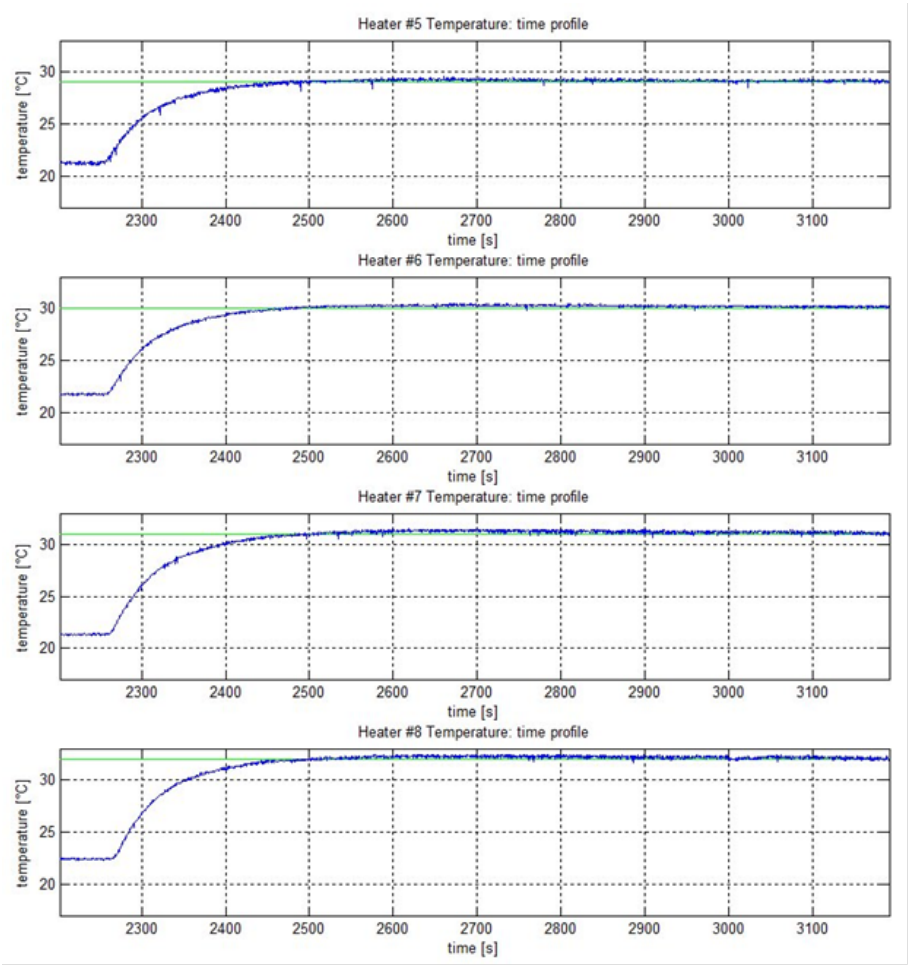
Test Set-up



Test Results

All heaters reach the temperature set points with a precision of about ±0.2°C





DHM Master Data Sheet

Digital Heater Module - Master	
Summary	■ Highly integrated distributed thermal control system icluding both the heater driving and the data acquisition capability ■ High level of integration achieved by using a mixed-signal FPGA as module controller ■ Driving of heater elements in temperature controlled way by means of digital PID controllers and PWM drivers
Configuration	■ Mixed-signal Flash FPGA with integrated "Soft" IP core micro-controller Core80C51S ■ Redundant CAN Bus network for low-speed communication to/from OBDH ■ Redundant CAN Bus network for low-speed communication to/from Slave modules ■ PWM based heater drivers ■ Conditioning for external temperature sensors ■ Hardware digital PID Controller implemented in the FPGA
FPGA	■ Mixed-signal Actel Fusion FPGA family ■ Integrated 12-bit Analog to Digital Converter ■ Integrated Analog front end ■ Embedded Flash Memory
Processor	■ Core80C51S IP core running at 20MHz ■ 64Kbyte SRAM memory ■ 64Kbyte code implemented with the flash memory embedded into the FPGA ■ Debug: ■ RS422 UART I/F running at 115kbit/s ■ JTAG port
CAN Bus	■ Core provided by ESA (ver. 5.2.4) ■ Bit rate: 500kbit/s ■ Redounded CAN bus to/from OBDH for: • Decoding of configuration commands • Transmission of HK and status ■ Redounded CAN bus to/from DHM slaves for: • Commands from OBDH to slave modules transmission • Slave modules status reading
Heater Drivers	■ Number of drivers: 3 ■ Power delivered with a PWM Voltage driver ■ Nominal voltage : 28V ■ Driving current: 2A (at least)
Temperature sensor I/F	Support for two different types of temperature sensors: ■ Diode Connected Transistor ■ AD590 Active temperature sensor
PID Controller	■ Three Hardware cores included into the FPGA ■ "Velocity form - type C" implementation ■ PID or PI configurable ■ 100Hz sampling rate
Setting	■ PID controller parameters ■ Temperature set-point ■ Maximum power delivered to the heater ■ Temperature sampling frequency
Housekeeping	■ Temperature set point ■ Acquired Temperatures ■ Modules status update rate:10Hz
Power Supply	28V nominal
Power Consumption	1.5W @ 28V
Mechanical Specs	■ Size: 76.7mm x 66.1mm x 24.7mm ■ Mass: 169 g

Digital Heater Module - Slave	
Summary	■ Highly integrated distributed thermal control system including both the heater driving and the data acquisition capability. ■ High level of integration achieved by using a mixed-signal FPGA as module controller ■ Driving of heater elements in temperature controlled way by means of digital PID controllers and PWM drivers
Configuration	■ Mixed-signal Flash FPGA ■ Redundant CAN Bus network for low-speed communication to/from Master module ■ PWM based heater drivers ■ Conditioning for external temperature sensors ■ Hardware digital PID Controller implemented in the FPGA
FPGA	■ Mixed-signal Actel Fusion FPGA family ■ Integrated 12-bit Analog to Digital Converter ■ Integrated Analog front end ■ Embedded Flash Memory
CAN Bus	■ Core provided by ESA (ver. 5.2.4) ■ Bit rate: 500kbit/s ■ Redundant bus ■ Communication to/from DHM Master for: • Command reception • Module status transmission
Heater Drivers	■ Number of drivers: 3 ■ Power delivered with a PWM Voltage driver ■ Nominal voltage : 28V ■ Driving current: 2A (at least)
Temperature sensor I/F	Support for two different types of temperature sensors: ■ Diode Connected Transistor ■ AD590 Active temperature sensor
PID Controller	■ Three Hardware cores included into the FPGA ■ "Velocity form - type C" implementation ■ PID or PI configurable ■ 100Hz sampling rate
Setting	■ PID controller parameters ■ Temperature set-point ■ Maximum power delivered to the heater ■ Temperature sampling frequency
Housekeeping	■ Temperature set point ■ Acquired Temperatures ■ Modules status update rate:10Hz
Power Supply	28V nominal
Power Consumption	1W @ 28V
Mechanical Specs	■ Size: 66mm x 66.1mm x 24.7mm ■ Mass: 158g

DHM Slave Data Sheet

Possible Follow-on

- Flight Application for a Satellite Thermal Control employing the actual configuration and size
  - The DHM has been already designed by selecting technologies and components also available in radiation tolerant version
  - One or more (in some cases) solutions of radiation tolerant components (ITAR or ITAR free and with different tolerance levels) are available for each specific function
  - The application would require only a proper modification of the PCB to take into account the package of the specific selected radiation tolerant devices

- Development of a dedicated mixed signal ASIC
  - The development of an ASIC would allow to drastically reduce the number of components and consequently the size and mass of the device thus increasing significantly the number of potential space applications

Possible Applications in other Fields

- The architecture and the technology solutions for the Digital Heater Module could be fruitfully employed in Health Monitoring Applications that could take benefits from a distributed network of sensors and actuators and a capability of local signal processing

- An interesting application could be the Health Monitoring of aeronautical structures aimed at implementing an early detection of structural degradation/damages

- A network of miniaturized devices could be used for a distributed acquisition of signals generated by accelerometers, strain gage, etc. distributed on the structure and also, in case of adoption of active techniques, for the distributed driving of piezoelectric actuators