SATA CONTROLLER
INTO A
SPACE CPU

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TEC-ED & TEC-SW

Final Presentation Days

ESA-ESTEC June 2015

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ntroduction

- The SATA specifications define a flexible and reliable communication protocol between host and mass storage devices like the HDDs (Hard Disk Drives), based on magnetic rotating disks and the latest SSDs (Solid State Disks), based on Flash memory devices

- Adoption of SATA provides a low cost solution, high data rates, easy integration due to the compact cabling and greater flexibility with respect to system configuration

- In the last years the SSDs are substituting the HDDs for applications requiring higher transfer rate, lower power consumption and better reliability

- The SATA SSD storage technology has gained a good penetration also in the military and defense segments thanks to its relevant benefits over competitive solutions and to the technological trend in the industry and consumer markets

ntroduction

The technology can be considered mature and the industry road-map is well established and the support in the long-term is ensured. Ruggedized SATA SSDs are currently available with storage capacity up to 128 GByte and read/write rate up to 210 MByte/s

The non volatile NAND-based flash memory, on which the SATA SSDs are based, is raising an increasing interest for space applications too

A number of radiation tests performed for Ground and Flight Missions have demonstrated a radiation tolerance in the order of tens of Krads that can results enough for LEO Missions also with significant duration

R&D activities are on-going to define powerful error-correction system to mitigate the possible failure of those memories and allow them to be reliable over a long period of time

ntroduction

This presentation describes the activities performed within an ESA project , named "*SATA Controller into a Space CPU*" aimed at starting a development activity to spin-in the SATA technology to the space market

Space applications could benefit from the adoption of the SATA protocol as interface layer between the host controller and the mass memory module. Currently no space-proven implementation of the SATA specification exists

As first step, TSD has proposed the development of a LEON based CPU implementing the SATA controller in the same FPGA that hosts the LEON Soft IP core; such CPU board can initially be used, in combination with ruggedized COTS SATA SSDs, for short missions and in general for missions with low radiation tolerance requirements

In a subsequent step, in order to provide a complete radiation tolerant SATA storage solution, a solid state qualified storage device with SATA interface could be designed as a follow-up R&D activity

SATA Controller – CCSM Architecture

The integration of a SATA Controller into a Space CPU is achieved with a module named CCSM (*Control, Communication and Storage Module*)

The module consists of a CCSM Motherboard and a CCSM Daughterboard which physically hosts the SATA SSD

The CCSM has been designed by adopting components already available in radiation tolerant version, like the Xilink Virtex-5 FPGA for which it is available the Virtex-5QV version that represents the industry's first high performance rad-hard reprogrammable FPGA for processing-intensive space systems

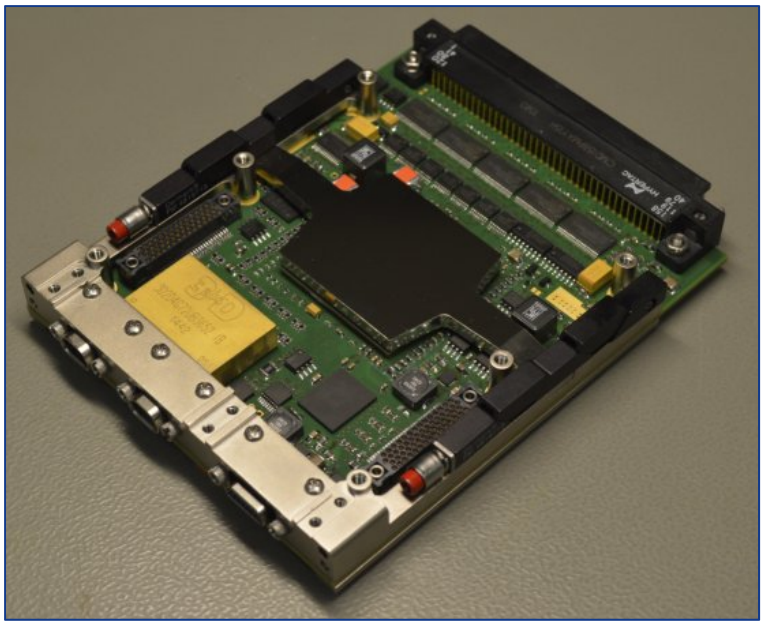
Thanks to its very high density and performances, the Virtex-5 FPGA is employed as a complex SoC (System-on-Chip), hosting the LEON3 CPU and all the foreseen peripherals

SATA Controller – CCSM Architecture

The selected architecture provides the following advantages:

- by integrating the CPU and all the peripherals in only one devices, better performances and higher integration level can be guaranteed
- by adopting a reprogrammable FPGA, different architectural solutions for the SoC can be evaluated
- the high density FPGA allows to have free available resources to implement hardware accelerators for intensive computational tasks, so to achieve high performance for data processing applications
- different available IP cores can be evaluated including third-part available IP core (for example for SATA I/F) and relevant ESA IP cores (for example SpaceWire and CAN IP cores)

SATA Controller – CCSM Configuration



CCSM Motherboard

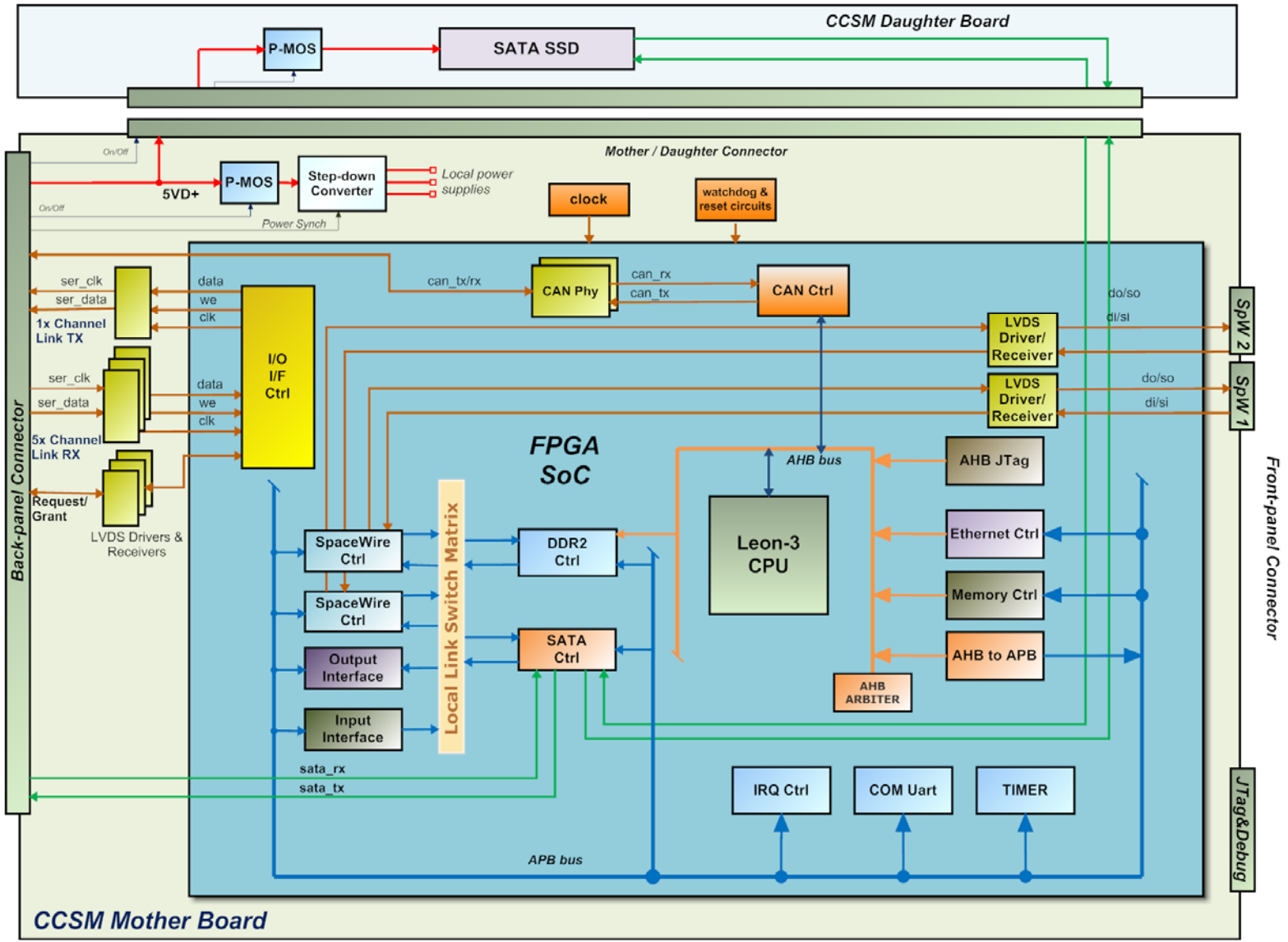
The CCSM consists of a Motherboard hosting the FPGA implementing the LEON3 CPU and the SATA controller and a Daughterboard which physically hosts one SATA SSD

An additional SATA SSD can be connected to the module through the backplane connector

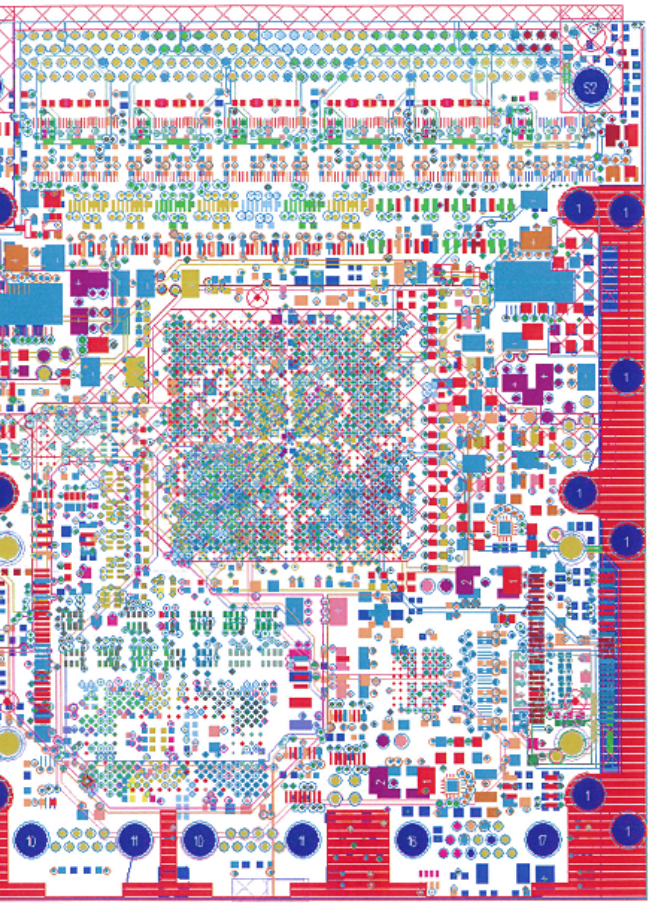
In addition to the Virtex-5 FPGA SoC, external data and program memories (DDR2) are employed for the operating system and the application software

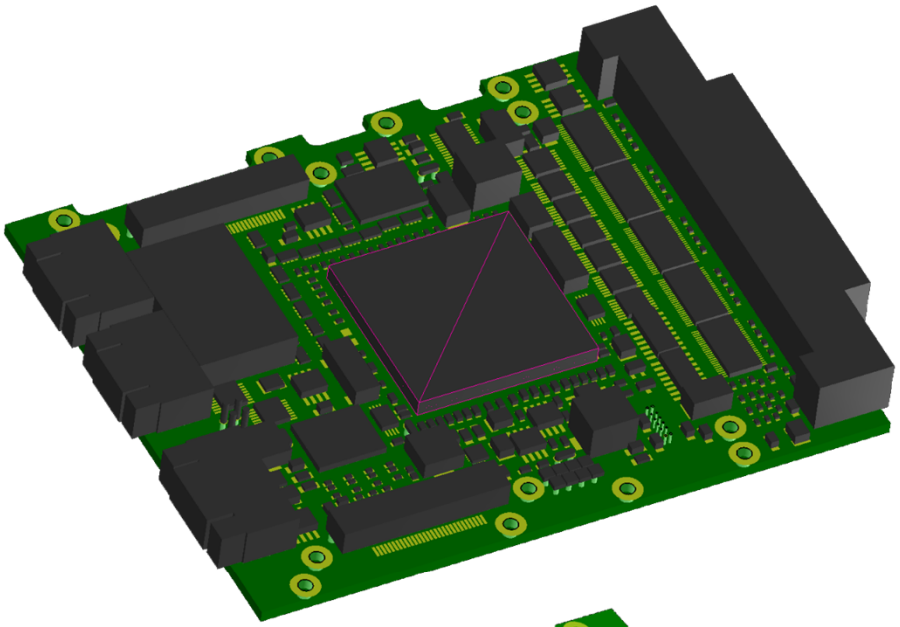
The unit is powered by a 5V input line; high-efficiency switching point-of-load converters are used to provide the low voltage lines needed by the local electronics

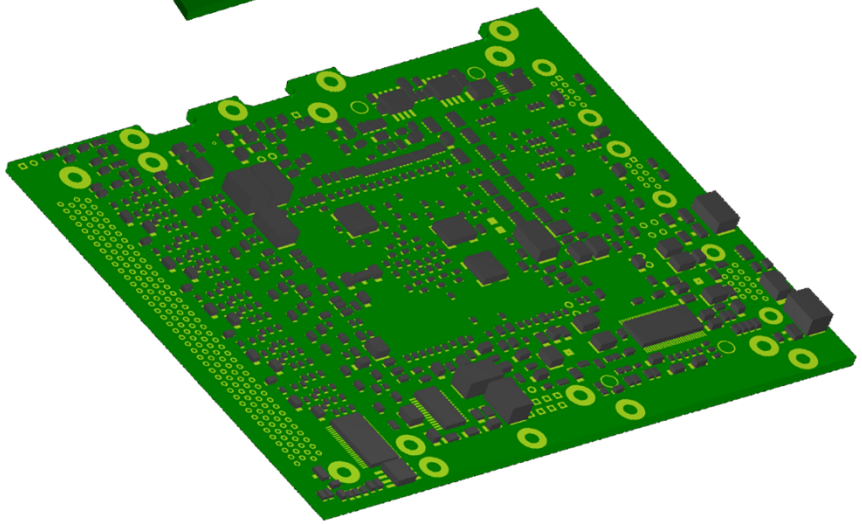
SATA Controller – CCSM overall block diagram



SATA Controller – CAD Models







SATA Controller – CCSM Architecture

e CCSM offers the following basic functionalities:

- LEON-3 CPU
- SATA controller for two Solid-State Storage Devices
- 2 x SpaceWire I/Fs
- CameraLink video image acquisition
- 4 x Channel Link Deserializer inputs @ ~1.5Gb/s
- 1 x Channel Link Serializer output @ ~ 1.5 Gb/s
- Redundant CAN I/F
- 256MB DDR2 as high speed volatile memory for acquired data buffering and for LEON-3 CPU
- FLASH memory as non- volatile memory for FPGA bitstream and LEON-3 CPU SW storage
- 1 x Ethernet I/F
- 1 x RS422 Debug I/F

SATA IP core - selection criteria

- A market survey has been carried out to identify and select the core that implements the SATA controller in FPGA

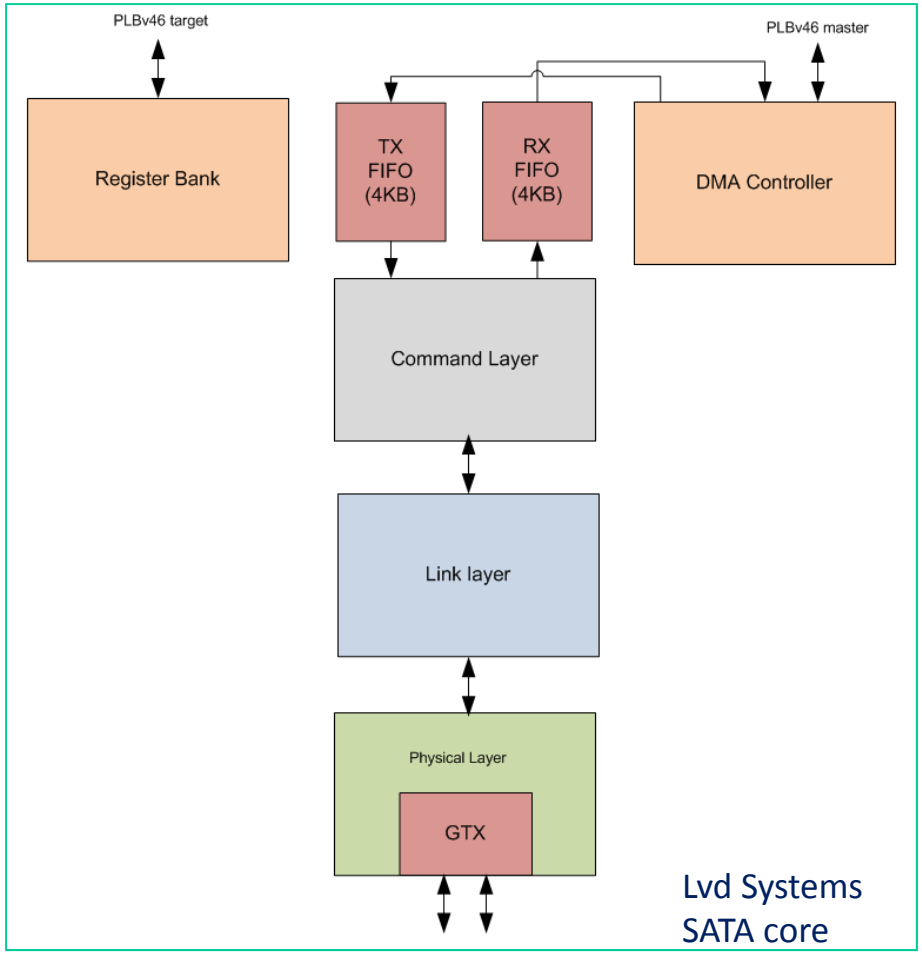
- The following criteria have been considered to select the candidate:
  - direct support for Virtex-5 FPGA integration and embedded GTX/GTP transceiver usage for SATA Phy
  - maximum operating frequency
  - availability of demo version or a hardware evaluation license
  - core deliverable (documentation, source code and/or netlist)
  - long term support
  - supplier location
  - cost

- The core selected is the one provided by *LVD Systems*. The main reasons for the choice are:
  - performances equivalent to other evaluated products
  - availability of source code
  - single site license, multiple projects
  - tight connection with IP core developer (LVD is an Italian firm)

SATA IP core – selected solution

P core has three main interfaces:
target interface: low speed
rface used for configuration, status
nitoring and for command issuing
master interface: used by the core
ransmit and receive data to/from the
tem memory using an embedded
A controller
h Speed differential signals (using
X) to communicate with the SATA disk

P core architecture has three main
ules:
sical Layer: implements low level
A interfacing and negotiation
k Layer: implements SATA scrambling
descrambling, flow control and FIS
apsulation
mmand Layer: generates SATA FISes
ording to user commands and
eives and decodes SATA FISes from
disk



SATA Disk

SATA SSD SELECTION

In the last years some “embedded” and in particular “board level” variants of the traditional 1.8” form factor SATA SSD disks have gained market positions for applications where reduced mass and envelope dimensions represent critical factors

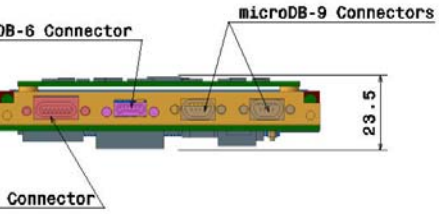
A board level SSD has been considered very interesting for the CCSM and the Slim-SATA (MO-297), a registered standard, by JEDEC Solid State Technology Association, has been selected because it is very suitable to be hosted and fixed on the PCB of the CCSM daughter board.

The MO-297 standard defines the layout, connector positions and physical dimensions for a 54mm x 39mm solid state drive, thus allowing interchangeability among products coming from a number of different suppliers

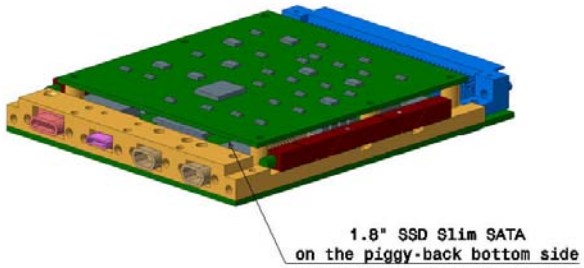
Proteus Plus SSD, 64GB

- Selected Slim-SATA embedded module by TCS
- TCS offers solutions which are specifically designed for the military market and special assembly options are available for space applications

CSM Mechanical layout

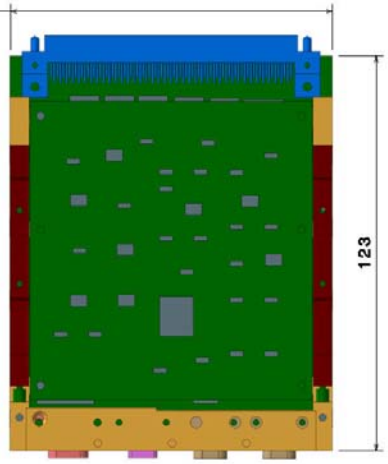


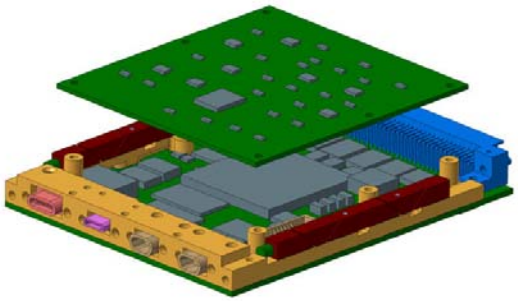
FRONT VIEW



ISO VIEW

TOP VIEW

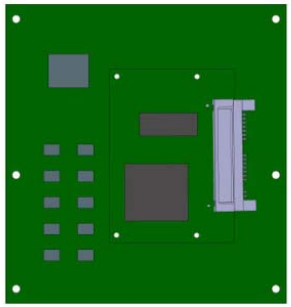




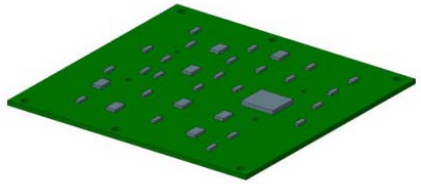
EXPLODED VIEW

- From mechanical point of view, the CCSM has been designed so as to minimize the overall dimensions, allowing to have all functionalities in a very compact volume.
- As shown in the picture, the CCSM mother and daughter boards are mechanically linked to an aluminum frame. This frame has a double purpose: it increases boards' stiffness and dissipates heat produced by electronic components. Moreover, the frame allows that stresses incoming from harness are not transferred to the PCB via the connectors.
- The weight of the CCSM motherboard is 243[g]

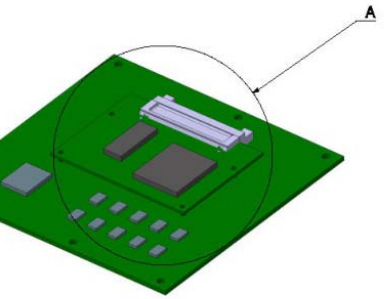
CSM – Slim SATA SSD mechanical detail



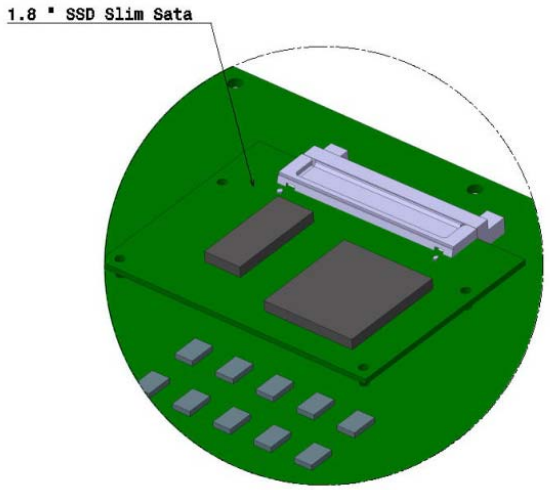
BOTTOM VIEW



ISO VIEW (top)



ISO VIEW (bottom) with SSD detail (A)



SSD Detail (A)

- The SSD PCB is mounted on the daughter board bottom side, thus reducing the overall dimensions
- The electrical connection is ensured through a slim SATA standard connector

CCSM SW Architecture

The CCSM Software foresees a layered architecture that comprises four main components:

- The Board Support Package (BSP)
- The Real Time Operating System (RTOS)
- The SATA driver and the Application Software (ASW)

SATA Controller SW Driver

The SATA controller is provided with a custom developed SATA SW driver that allows an easy integration with the selected operating system (currently WindRiver VxWorks 6.7)

The SATA driver provides the basic functionalities to initialize and control the SATA disk. In particular three main services are offered by the driver:

- **Initialization Service**: this service is called at the start-up and performs the SATA controller configuration and the attached device identification
- **Block Write Service**: this service allows to write a variable number of blocks (512-byte array) starting from a selected address. In this respect the disk is seen as a contiguous memory with flat addressing
- **Block Read Service**: this service allows to read a variable number of blocks (512-byte array) starting from a selected address

On top of the SATA driver it is possible to add a Block Device I/F SW library and a File System library which are usually provided by the operating system

SATA Controller SW Driver

e **Initialization Service** is provided by calling the ***sataInit*** function. The function rforms the following operations in sequence:

- Creates a VxWorks binary semaphore; this semaphore is given into the interrupt service routine (ISR) that is called when a SATA transaction is terminated. It is the method to signal to the SW the completion of the transaction
- Initializes the FPGA DMA engine that is used to transfer the data blocks to/from the SATA controller and the LEON-3 memory
- Initializes the interrupt controller by connecting the IRQ 7 to the ISR and unmasking (enabling) the corresponding bit in the IRQ mask
- Resets the SATA controller and then removes the reset
- Performs disk identification

ould any of the above operations fail, a corresponding error code is returned by e function

SATA Controller SW Driver

Block Write/Read Service is provided by calling the ***sataWrite/sataRead*** function. function requires the following input parameters:

pointer to the buffer containing the data to be written/read to/from the disk

he destination address of the disk expressed as the initial sector to be written/read

he total number of sectors to be written/read. The selected disk allows up to 512 ectors (256KB) to be transferred within a single write/read transaction

he function initiates the SATA transaction and waits until it is completed by pending n the reception of the above mentioned semaphore. The wait has a timeout urrently set to 5s. Should the timeout expire, the function returns an error code

SATA Controller – Validation tests

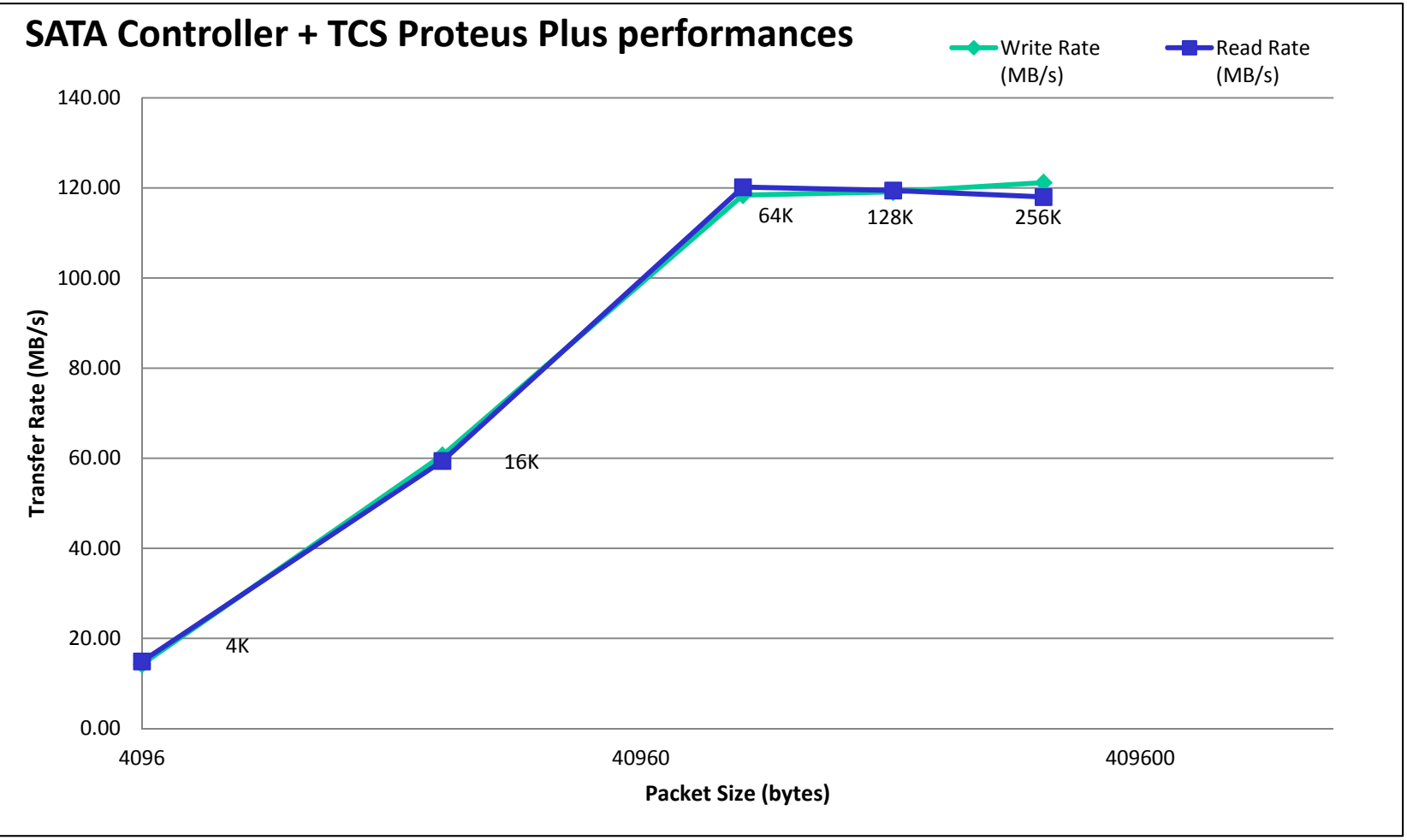
A number of tests have been carried out in order to verify the proper functioning and performances of the SATA controller. A host PC is used to control and command the CCSM, to download the SSD content and debug the CCSM application software (by UART and Ethernet links)

The Application SW (ASW) used for the validation tests is a benchmark of the SSD that makes use only of the SATA driver, i.e. without a file system, in order to achieve the maximum performances

The ASW allows to configure several parameters:

- Type of test: *WRITE* test, *READ* test, *WRITE/READ* test, *WRITE/READ/CHECK* test
- Size of data block to transfer with a single operation, range 512÷262144 bytes (256KB)
- Total amount of data to transfer, the entire capacity of the disk can be selected
- Sector of the disk where to start the operation

SATA Controller – Results



SATA Controller – Results

- The write and read performances are almost identical, as is typical of the solid state disks
- The peak of performances is achieved by utilizing large packet as is also typical of all types of disks, both mechanical and solid state, because the larger the packet the lower the number of SATA transactions
- Maximum performances are achieved already with 64K-packets and are in the order of 120MB/s that is close to the maximum throughput also declared by the disk manufacturer (~130 MB/s)
- The maximum power consumption of the CCSM during the sustained read/write operation is about 11[W]
- In the current configuration the FPGA is occupied at about 35% of the available resources

CCSM & SATA Controller - Planned Applications

The CCSM will be used by TSD as standard Control, Communication and Storage Module for Payloads especially those very demanding in terms of data handling that require acquisition, real time processing and storage at very high data rate

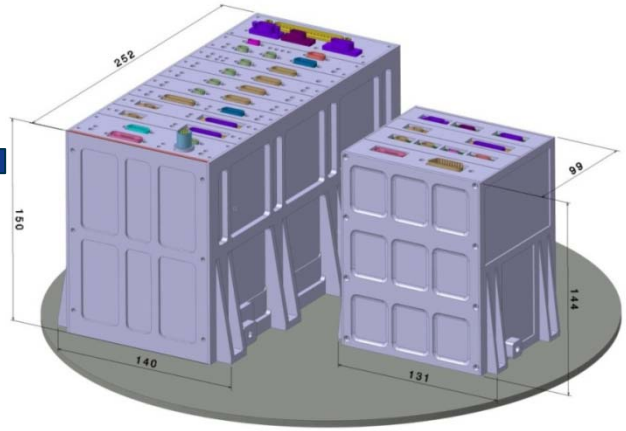
In perspective a radiation tolerant version of the CCSM could be used as core of a compact Compression & Storage Unit for Earth Observation Payloads on board Small Space Platforms

An already planned application for the CCSM low cost version is in the frame of ESA programme for Sounding Rockets where the CCSM will be employed as the controller of the Digital Video System on board MASER rockets

The adoption of the CCSM for the Digital Video System on board MASER rockets will allow a very significant reduction in terms of SWaP w.r.t. the existing video system. Next picture shows a comparison between the old and new system

ng System
Channel Version)

4.6[Kg]
e: 5.3[l]
32.8[W]@28[V]



New System based on CCSM

Mass: 1.8[Kg]
Volume: 1.9[l]
Power: 16[W] @ 28[V]