History of ESA Microprocessor Developments

MA 31750 (Dynex Semiconductor)

- MIL-STD-1750A architecture
- GEC-Plessey 1.5 µm

SPARC V7 ERC32 3-chipset

- IU, FPU, MEC: “TSC691 , 692, 693”
- Temic 0.8 µm

SPARC V7 ERC32 single chip

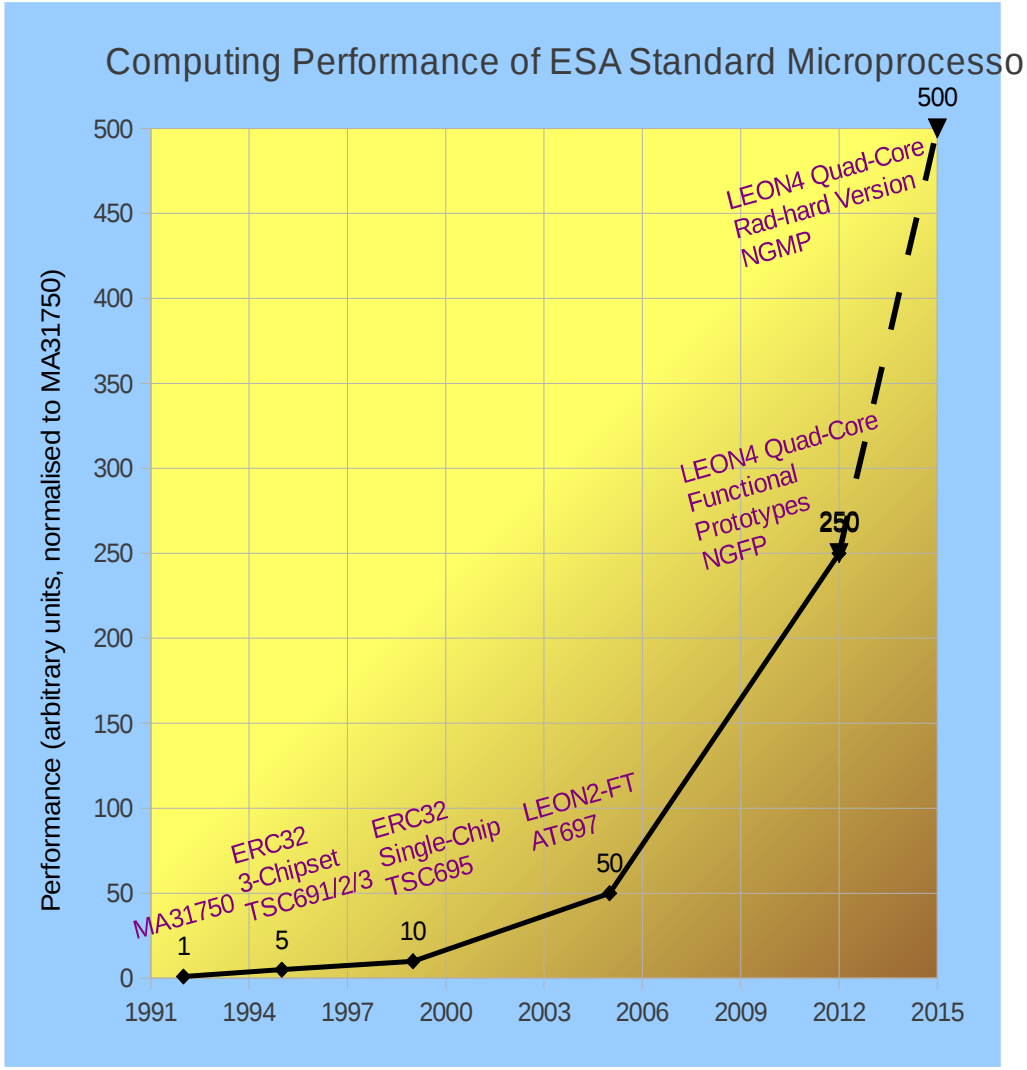
- Temic 0.5 µm – “TSC695”

SPARC V8 LEON2 – “AT697”

- Atmel 0.18 µm, 100 MHz single-core

SPARC V8 LEON4/NGMP – “GR740”

- ST Microelectronics 65 nm
- **Goal: 10x AT697 performance**



NGMP – How (and when) it all started …

Statement of Work for the GINA study

esa

Ref: TEC-EDD/2004.21/ALRP
Issue: 1, Rev.: 3
Date: 19 August 2004
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- To design, to model, to verify, and to validate the next generation of SPARC based architecture processor for space applications (LEON3) with a highly improved performances (250 MHz) and improved functionality as it is strongly required for future ESA space missions.

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The "real" NGMP contract was started in 2009 and it was on hold for some time, waiting for a suitable ASIC technology