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GR740 - Next Generation Microprocessor (NGMP)

Cobham Gaisler
2015-06-01

Presenter: Jan Andersson

Final Presentation Days 2015
ESA/ESTEC

Introduction

What is NGMP?

- NGMP: Next Generation Microprocessor
  - (Next Generation Multi Purpose Microprocessor)
- NGMP is an ESA activity developing a multi-processor system with higher performance than earlier generations of European space-microprocessors
- The NGMP is part of the ESA roadmap for standard microprocessor components
- The goal of this contract was specification of the architecture, architectural (VHDL) design, and verification by simulation and on FPGA. The goal of this work was to produce a verified gate-level netlist for a suitable technology. Contract was then extended to also include (almost all) work up to mask production.

Introduction

Team

- Team (tech):
  - Cobham Gaisler (SE): Requirements, verification, synthesis, (FPGA) validation
    - M. Hjorth, M. Själander, N-J. Wessman, J. Gaisler, D. Hellström, M. Åberg, A. Larsson, D. Cederman, A. Gianarro, M. Isomäki, K. Glembo
  - EADS Astrium, now AD&S (FR, D): Requirements, specification
    - V. Lefftz, JF. Coldefy, H. Fischer, O. Notebaert
  - STMicroelectronics (FR, UK): Tech provider, Layout
    - R. Chevallier, R. Forsyth
  - ESA: Roland Weigand (TO), Luca Fossati
- Functional prototype development team: Cobham Gaisler (SE), Pender Electronic Design (CH), eASIC (US, RO)
- Input received from several parallel activities at ESA and CNES. As well as from internal R&D efforts at several companies

Objectives

Next Generation Multi Purpose Microprocessor

- To develop a microprocessor (NGMP) with higher performance than earlier European space-microprocessors
  - Establish NGMP specification, selection of suitable IP cores, design feasibility assessment, SEE mitigation assessment, considering also SW induced requirements to facilitate reuse of existing SW
  - Establish requirements for OS and SW development tools
  - NGMP design implementation in HDL and verification by simulation
  - Adaption of compilers, BSP for OS and development of drivers for the on-chip peripherals
  - NGMP verification and co-verification with OS and drivers on FPGA platform
  - Advanced synthesis on the target technology, baseline ST Space-DSM
  - Preliminary validation of the applied SEE mitigation by analysis simulation and fault injection

Objectives

NGMP CCN: Feature extensions, detailed design and layout

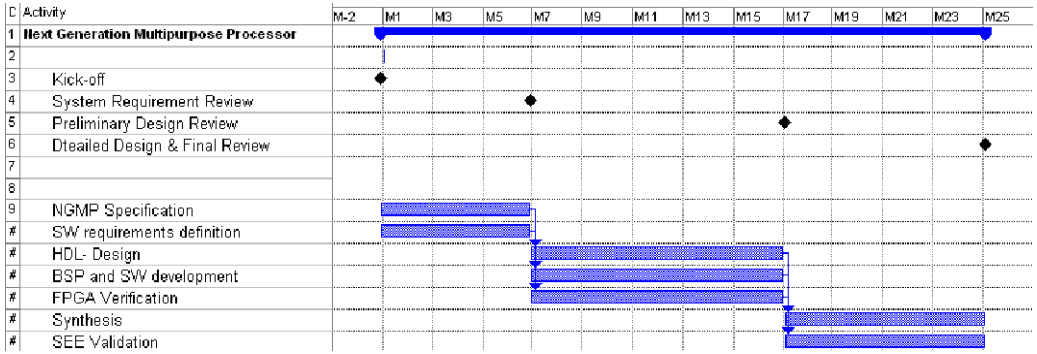
- Extension of phase 1 to also include layout work
  - Extend Level-2 cache to allow handling cache hits while performing miss processing
  - Final synthesis, gate-level simulations, layout verification
  - Back-end work

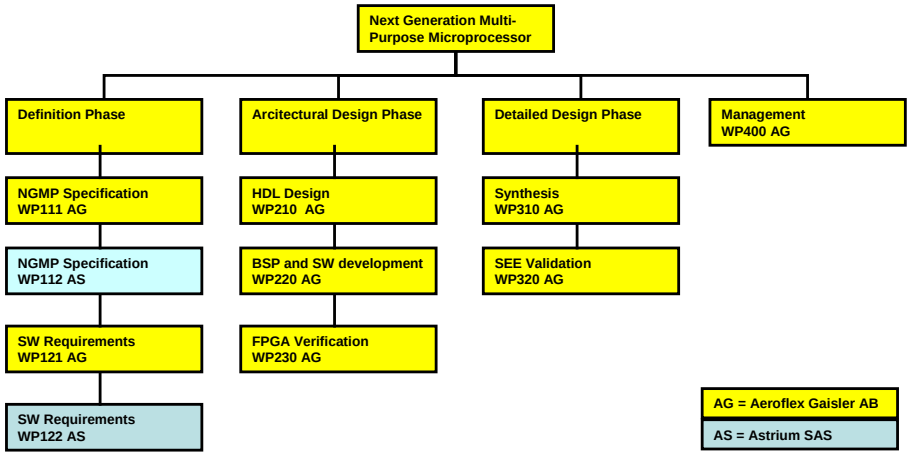
Description of work performed

- Specification
- Architectural design
  - Software/tool support (debugger, simulator, toolchains)
  - Benchmarks / trade-offs
  - Evaluation boards (functional prototype, FPGA prototypes)
- Detailed design, verification
- Layout and layout verification
- (Package design)

Schedule and work packages

Phase 1 + 0.5



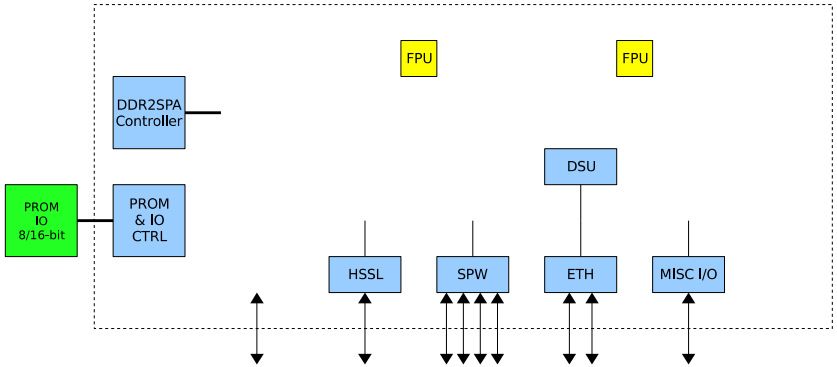


- Milestone completion:
  - T0: 1st of Aug 2009
  - SRR: Feb 2010
  - PDR: Dec 2010
  - (FP development)
  - pDDR: June 2014
    - Planned: Aug 2011
  - $T0_{CCN}$ 15th July 2014
  - DDR/pCDR: Dec 2014
    - Planned: Oct 2014
  - pCDR/FR: April 2015
    - Planned: Nov 2014

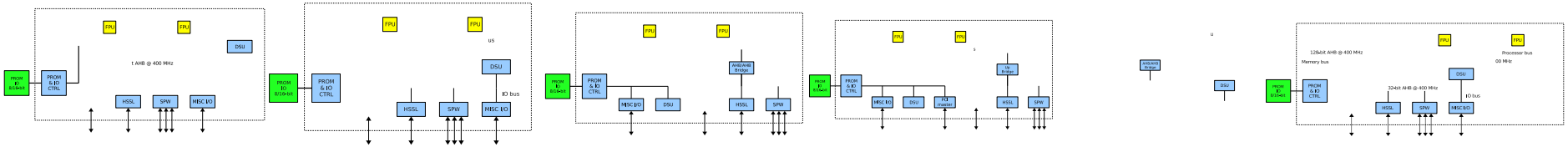
- CCN WP510: Feature extension
- CCN WP610: Detailed design and pre-layout verification
- CCN WP710: Layout generation and verification

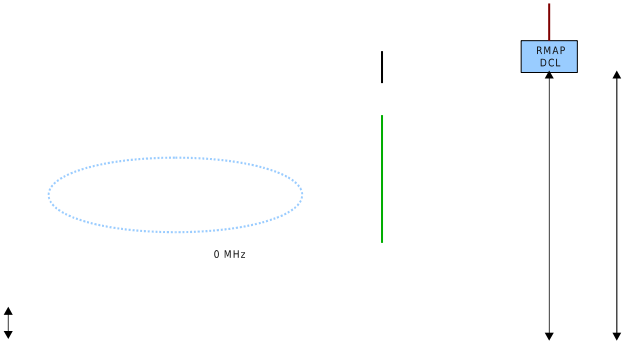
Evolution of design

Proposal -> Specification, SRR



- Proposal, December 2008

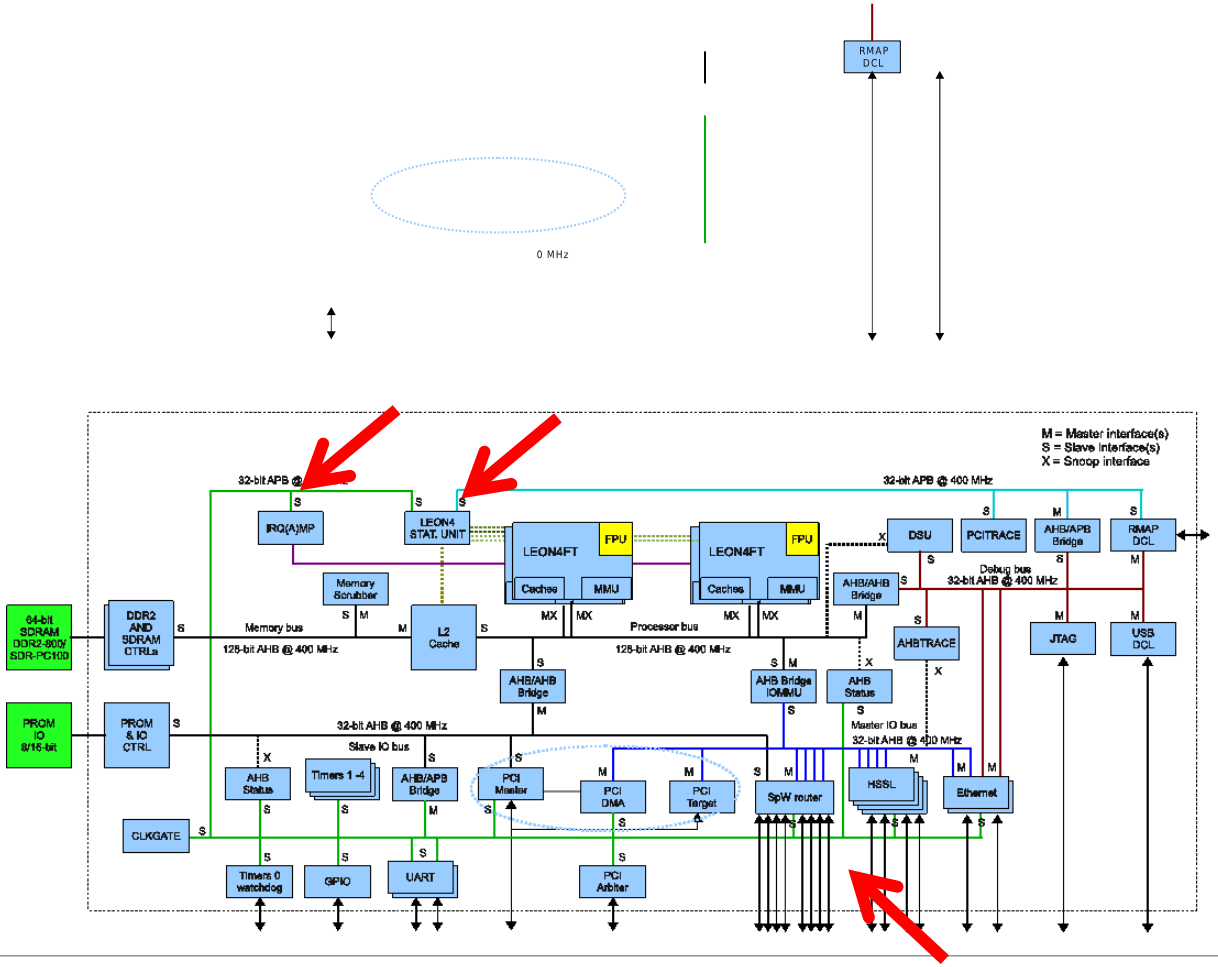




- Specification, February 2010

Evolution of design

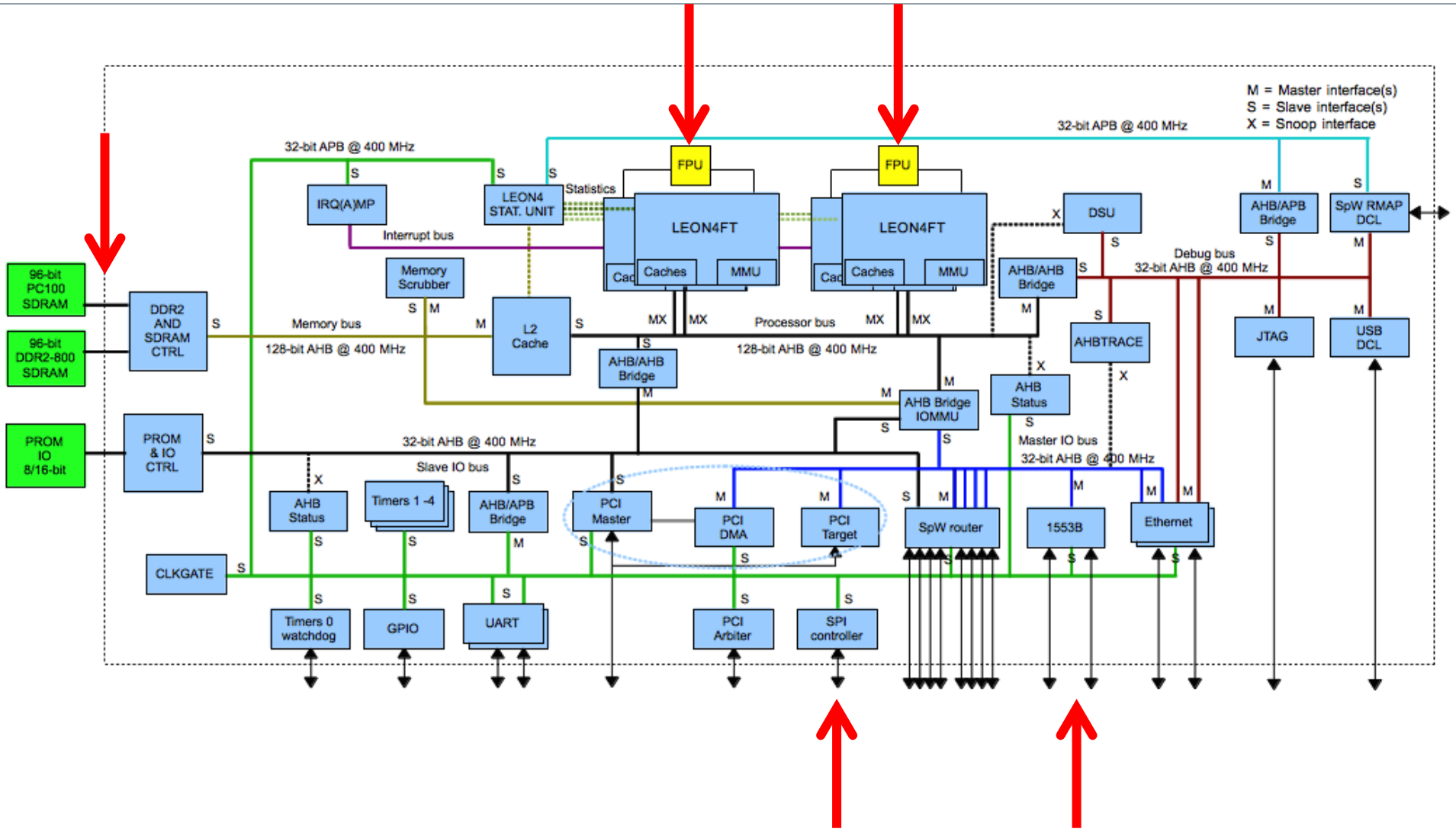
SRR to PDR



- SRR, February 2010
- PDR, December 2010

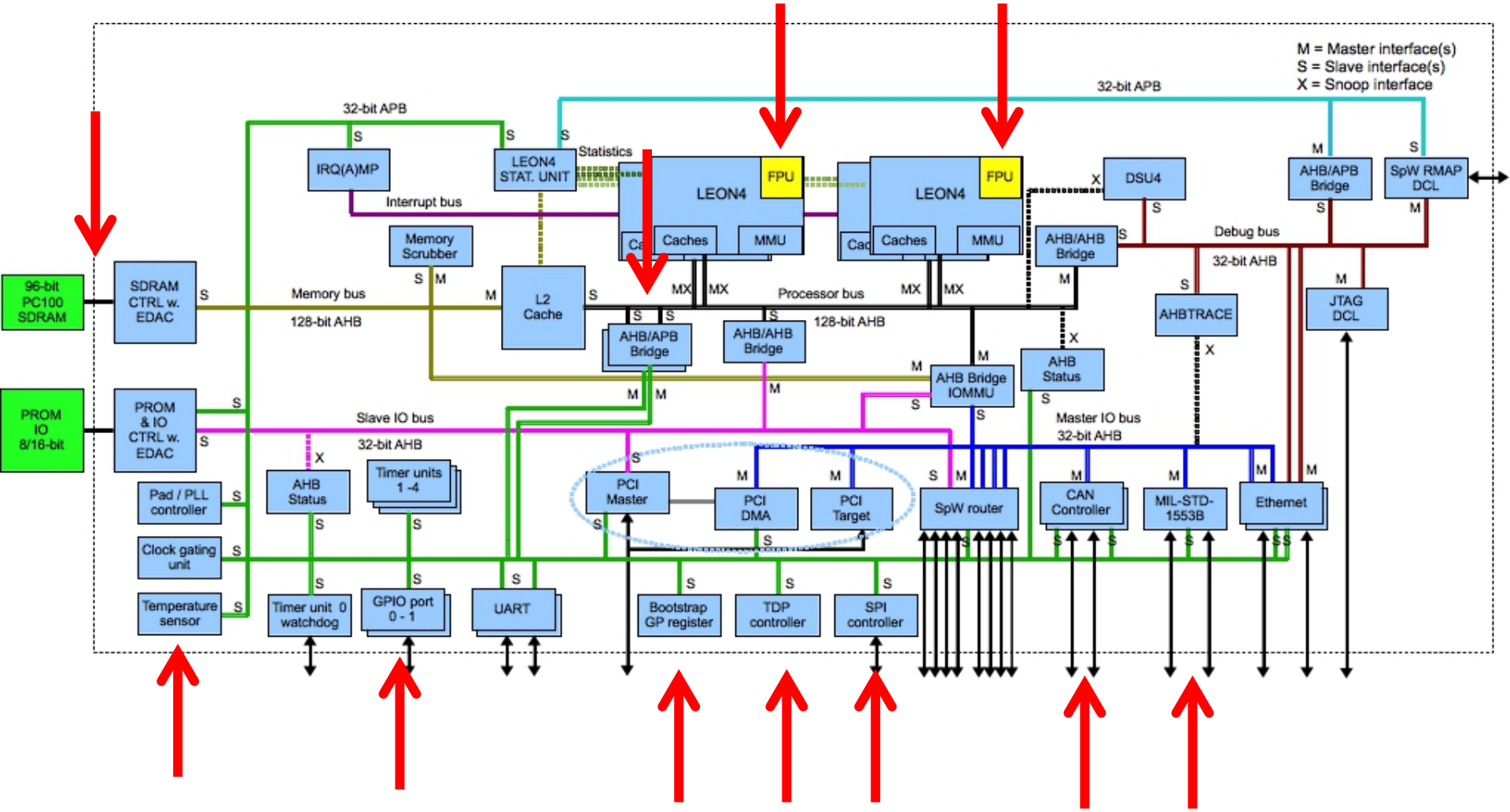
Evolution of Design

Functional prototype implementation



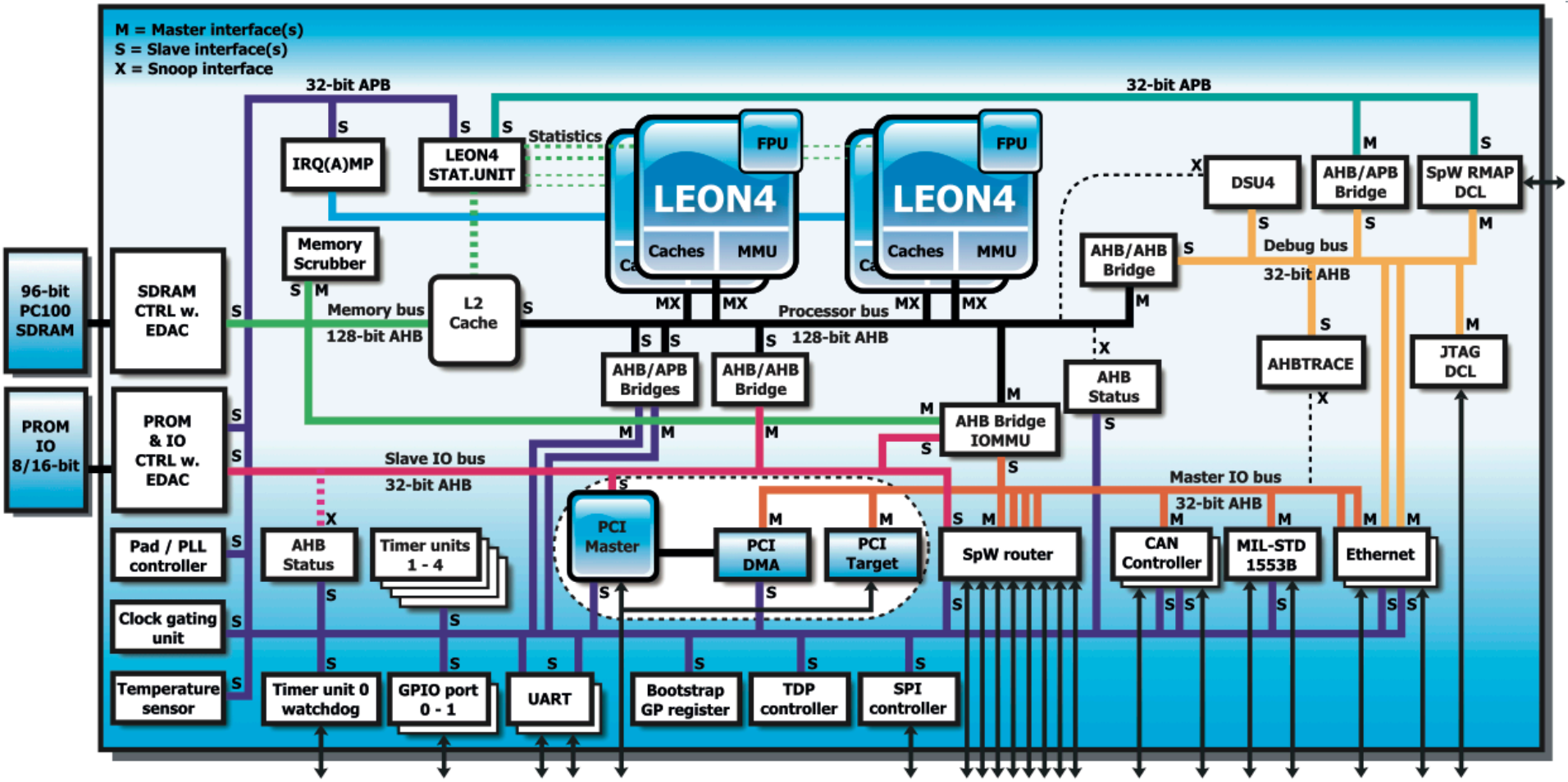
Evolution of Design

NGMP EM – GR740



Description of design

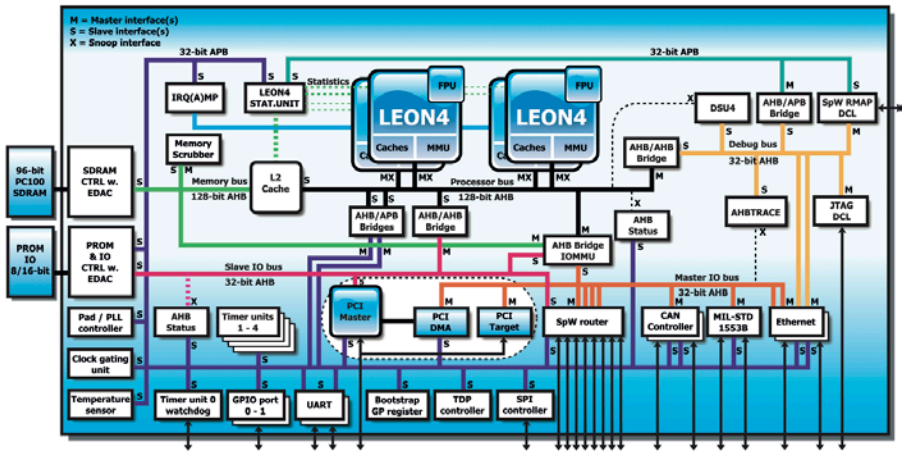
GR740



NGMP Design Overview

Features – for GR740

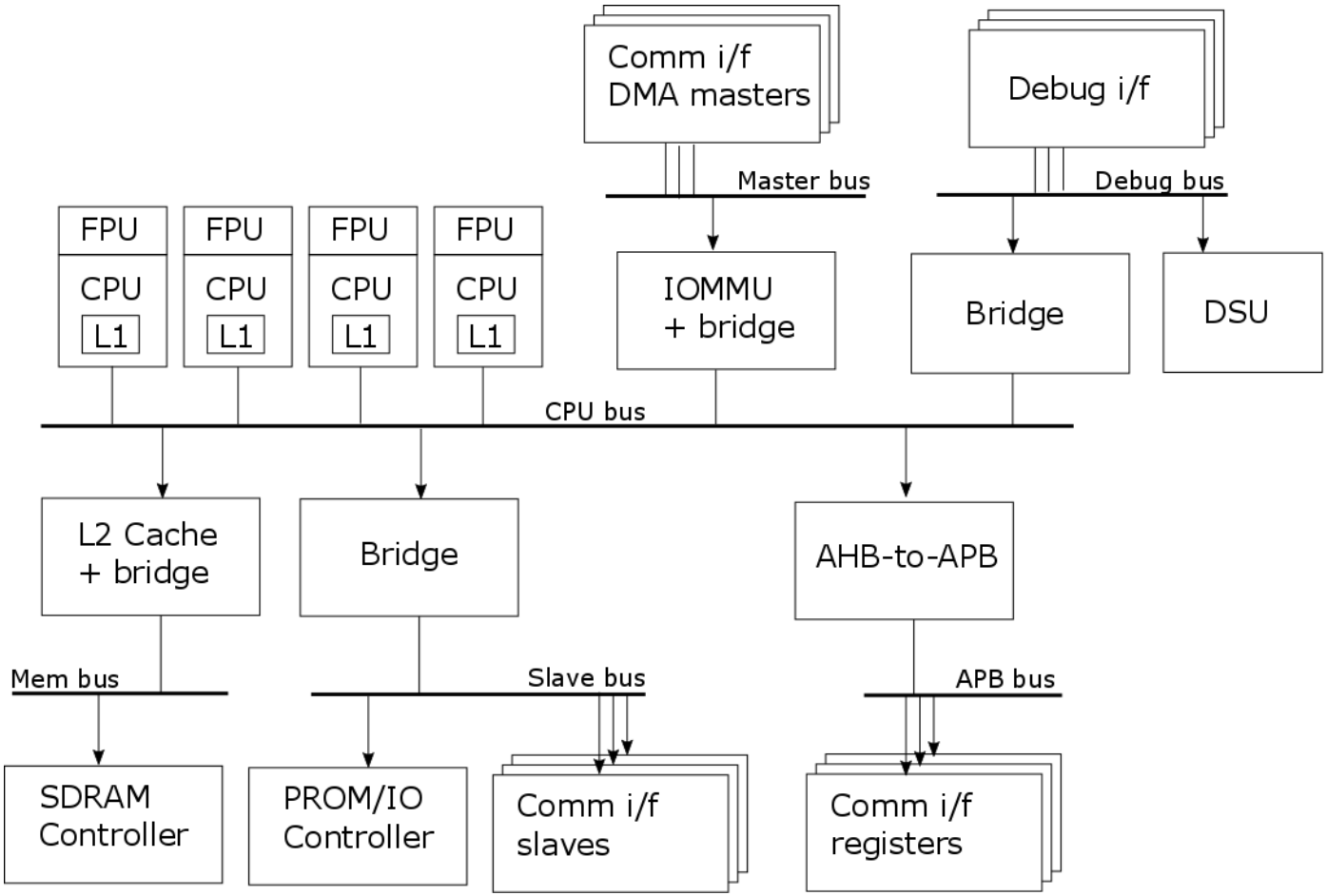
- System-on-chip
  - 4 x LEON4 fault tolerant CPU:s with L1 cache, MMU and FPU
  - 2 MiB Level-2 cache
  - 96/48-bit SDRAM controller with EDAC and scrubber
  - 8/16-bit PROM/IO controller with EDAC
  - 5 x Timer, 5 x IRQ controller
  - IOMMU for peripheral DMA
  - On-chip AHB bus infrastructure
  - PLLs for clock generation
  - Communication interfaces



NGMP Design Overview

Simplified block diagram

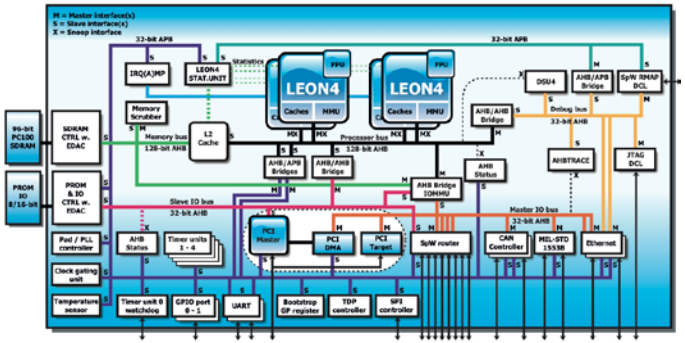
- Architecture block diagram (simplified)



NGMP Design Overview

I/O interfaces – for GR740

- Interfaces
  - 8-port Spacewire router with on-chip LVDS
  - 2 x 1Gbit/100Mbit Ethernet MAC (MII/GMII)
  - PCI master/target with DMA, 33/66 MHz
  - Dual-redundant CAN
  - MIL-STD-1553B interface (bus A/B)
  - 2 x UART
  - 16 x GPIO



- Debug interfaces (for GRMON connection)
  - Ethernet EDCL (using either of the two MACs above)
  - JTAG
  - Spacewire RMAP (separate GRSPW2 for debug only)

NGMP Design Overview

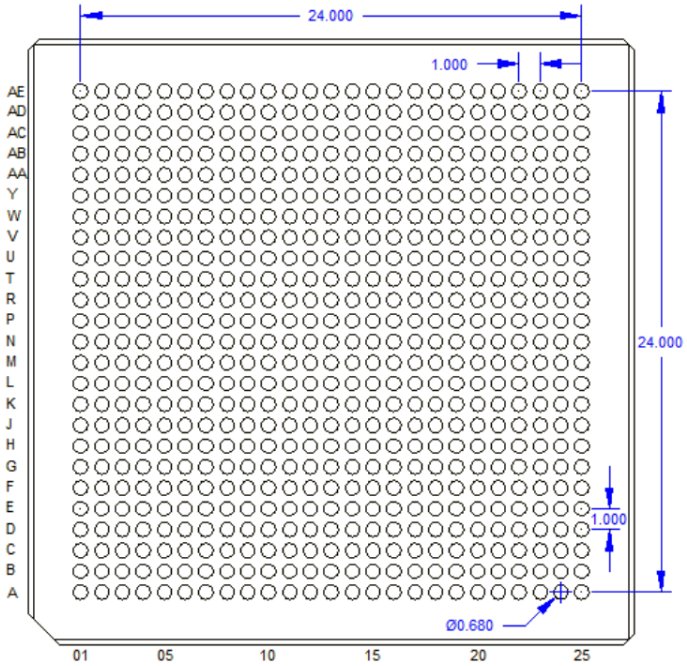
Interface restrictions

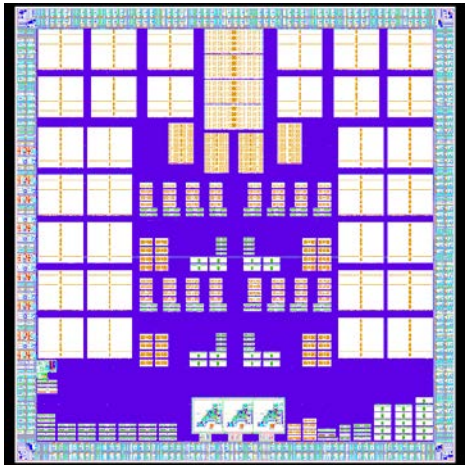
- Some functions have been multiplexed onto the same pins to fit into package
- Either PCI or second Ethernet (not both) can be enabled only when SDRAM is in 48-bit mode.
  - Configured “hard” via bootstrap signals.
- CAN,1553,UART,SpwDebug are shared with PROM top address bits and data bits unused in 8-bit mode.
  - Power-on state of muxing configured via bootstrap signal. Can then be reconfigured by software while running.
  - Configurable pin-by-pin between PROM or peripheral function.
  - Pins that are not used for either function can be used as additional GPIO.

NGMP Design Overview

Package

- Targeted package for prototype is CLGA625
  - Hermetic ceramic package
  - Wire-bond connection to ASIC
  - Approx 30 mm x 30 mm





NGMP Design Overview

Fault tolerance

- Design is radiation hardened using multiple techniques
  - C65SPACE process and cell libraries designed and characterized for radiation hardness
  - Memories SEU-protected at design level using EDAC schemes.
  - Processor register files using block-TMR scheme

  The NGMP shall be fault tolerant against SEU and SET effects tolerating a maximum rate of 10-5 uncorrectable errors per NGMP device per day corresponding to an MTBF of 274 years in geostationary orbit (conditions: solar minimum, Z=1 – 92, Al shielding of 1 g/cm2).
- Hardness to be validated by radiation testing (heavy ion, TID) on prototype.
- Baseline is to re-use exact same ASIC design and package for future flight models.

NGMP Design Overview

Clock frequencies

- Maximum clock frequencies obtained from post-layout STA:
  - System clock (CPU:s, L2Cache, on-chip buses): 250 MHz
    - 4 CPUs x 250 MHz x 1.7 DMIPS/MHz = 1700 DMIPS
  - Spacewire phy: 400 MHz
    - At least 300 Mbit/s data rate in point-to-point scenario (between two GR740:s) expected, limited by D/S skew. To be further characterized when silicon available.
  - SDRAM: 75 MHz expected (pad speed limited)
    - To be further characterized on silicon.
    - Maximum internal frequency 100 MHz.
    - Level-2 cache reduces impact of this limitation
- Timing valid for $T_{junction}$ from -40 to +125°C
- Also 20 years of aging accounted for
- In room temperature likely to be faster than this.

Improvements: Multi-core aspects

SMP and AMP support

- Designed for both SMP and AMP/hybrid operation
  - Peripheral addresses aligned on 4KiB to allow MMU/IOMMU access control
  - Ability to use separate IRQ controller and timer for each CPU
  - IRQ remapping support
- Use cases
  - SMP, one OS (VxWorks, RTEMS-SMP, Linux) running on multiple cores with shared memory space
  - AMP, different single-core OS on each CPU with separate memory, (possibly also with some shared memory area)
  - Virtualized multi-core system with N isolated virtual CPU:s under hypervisor (XtratuM, PikeOS)
  - Hybrid of above approaches
  - ...and traditional single CPU core usage is still supported of course

Improvements: Various

Non-exhaustive list

- Performance
  - Additional processors
  - Level-2 cache
  - Wide buses
- Debugging
  - Dedicated debug bus non-intrusive debugging
  - Higher speed on debug interfaces
  - Performance counters
  - Instruction trace filters, Bus trace filters
  - Data area monitoring
  - PCI trace buffer
  - New features for instrumentation
- Interrupt timestamping – both in timer units and in interrupt controller
- Time synchronization
- Partitioning/Duplication: AMP and SMP
- Interrupt remapping
- Hardware memory scrubber for external RAM
- Async system (AMBA) and SDRAM clock
- Gigabit Ethernet
- IOMMU
- ”Soft” watchdogs via NMI
- Level-2 cache
  - Protection of address ranges
  - Configurable between write-through and copy back
  - Optional use of hit-under-miss
  - Can be placed in ”shallow queue” mode
  - Can be bypassed by IO DMA
- Processor internals
  - Wider datapaths
  - Up counter
  - Soft L1 replacement policy
  - Partial WRPSR
  - Branch prediction extensions
- GPIO interrupt flag register and multi-core-safe GPIO port register interface
- Pin-sharing control
- Reprogrammable PLLs
- Programmability of IOs
- Temperature sensor
- Programmable memory controller timing
- ... and recent version of all Cobham Gaisler IP

Improvements: Level-2 cache

Level-2 cache performance impact

- Reduced memory traffic
  - Level 2 cache has write-back policy so all CPU writes that hit in L1 or L2 do not have to go through to memory
  - DMA masters can also be served by L2
- Non-blocking L2 cache using SPLIT protocol
  - New feature for L2 cache in GR740!
  - CPU waiting on an L2 cache miss does not block remaining CPU:s from being served.
  - Reduce execution time interference between processors.
  - Less impact of external memory latency on overall performance of system.
  - Micro-benchmark shows >400% improvement over blocking L2 cache in worst case (one CPU always generating L2 misses, other CPUs never generating L2 misses)

NGMP Applications

RAM-less / PROM-less

- If 2 MiB RAM memory or less is needed, the chip can be used without any RAM connected at all!
  - Reduce part count for example when we are only interested in using the GR740 as a (very flexible) IO-to-IO bridge chip.
  - All Level-2 cache ways are locked down and tags set to map 1:1 to the lowest 2 MiB of RAM.

- Nominal boot method on GR740 is to boot up from 8-bit parallel PROM (NOR flash or MRAM)
  - Alternatively can be used without any PROM and instead booted up remotely via Spacewire RMAP, Ethernet EDCL protocol, or PCI.
  - Master node can boot up PROM-less slave nodes this way.
    - Upload software to RAM
    - Configure start address of CPU(s)
    - Start execution

NGMP Applications

Time sychronization

- GR740 has been designed to allow time stamping of events and synchronization between CPU:s and interfaces
  - CPU cycle counter
  - Interrupts from any IP in system
  - Spacewire time codes
  - 1553 sync mode commands
- Can also be configured to toggle GPIO output when above events occur without software in the loop.

Software support

- Software for functional verification:
  - Bare-metal (multi-core extensions planned)
  - RTEMS (AMP, RTEMS-SMP from Gaisler in 4.11)
  - VxWorks 6.7 (Supports SMP)
  - Linux 2.6+ (Supports SMP)
  - eCos (Supports SMP, feedback welcome)
- Difference compared to GR712/UT*/LEON3FT*: Memory map + later versions of peripherals.
- GRMON2 debug monitor extended
- NGMP ISS based on GRSIM

Comparison between GR740, NGMP, NGFP

- GR740 Comparison Document (GR740-CMP)
- Main differences between NGMP and GR740: Frequency. Lack of DDR(2) SDRAM and HSSL. Pin-sharing.

Feature	GR740	LEON4-NGX	NGMP
On-chip buses	AMBA, 2xAPB	AMBA, 2xAPB	AMBA, 2xAPB
On-chip bus frequency	Same as CPU	Same as CPU	Same as CPU
CPU bus	128-bit AHB	128-bit AHB	128-bit AHB
Memory bus	128-bit AHB	128-bit AHB	128-bit AHB
I/O bridge bus	32-bit AHB	32-bit AHB	32-bit AHB
I/O bridge access control	8 REGIONS	8 REGIONS	8 REGIONS
I/O on other bus (PCI, if supported)	No	Yes, configurable by software.	Yes, configurable by software.
GRMPCI bus ownership	Who registers and RETRY.	Not supported	Who registers
GRMPCI bus master groups	8	8	6
I/O filter bus	32-bit AHB	32-bit AHB	32-bit AHB
APB bus connected to CPU bus	Yes	No (connected to slave I/O bus)	No (connected to slave I/O bus)
Debug bus	32-bit AHB	32-bit AHB	32-bit AHB
Debug bus clock gating	Yes (via DSUEN)	Yes (via DSUEN)	Yes (via DSUEN)
Main memory controller	DDR/SDR	Multiplexed DDR2/SDRAM or separate pins	Multiplexed DDR2/SDRAM or separate pins
Memory width	64+32 / 32+16	64+32 / 32+16	64+32 / 32+16
Memory speed	Up to 100 MHz DDR/SDR (PC133 Binding Banks)	200 MHz DDR2, 100 MHz DDR/SDRAM	400 MHz DDR2, 133 MHz DDR/SDR
DDR/SDR 2D ring routing	Yes	No	No
Memory EDAC	4x Interleaved RS	4x Interleaved RS	4x Interleaved RS
Wrt/Scrub RS1 Interleave	16-bit base	16-bit base	16-bit base
Memory Refresh	Yes	Yes	Yes
External memory scrubbing interleaver	Yes	Yes	Yes
PSDM controller	FIM CTRL 8/16-bit	FIM CTRL 8/16-bit	FIM CTRL, 8/16-bit
PSDM EDAC	Yes, in 8-bit mode	Yes, in 8-bit mode	Yes, in 8-bit mode
PSDM base-configures	Configurable by SPW	2	4
Spacewire	8 REDUNDANT LINES 8 (SpW ports 4 AMBA ports	8 REDUNDANT LINES 8 (SpW ports 4 AMBA ports	8 REDUNDANT LINES 8 (SpW ports 4 AMBA ports
Spacewire-D supported	Hardware support	No hardware support	No hardware support
Spacewire-FT supported	Yes, subset	No	No
Spacewire clock-Gated Interrupt supported	Yes, 32 interrupts with software/grp events and 64 interrupts, selected also brought as signals and software configurable.	No	No
Spacewire Time Code Handling	Connected to TDP controller and mapped to Time-Code filtering in Spacewire router AMBA ports.	Needs to be implemented in software.	Needs to be implemented in software.
Spacewire clock	200 MHz	200 MHz	200 MHz
Spacewire sampling	DDR	DDR	DDR
Spacewire buffers	Protected RAM	Unprotected RAM	Protected RAM
MIL-STD-1553B	BRM 5538 Enhanced.	BRM 5538 Enhanced.	BRM 5538 Enhanced.

Feature	GR740	LEON4-NGX	NGMP
CAN 2.0B controller	Yes, two	No	Yes, one
PCI Interface	1 BRICK 32-bit, 33/66 MHz	1 BRICK 32-bit, 33/66 MHz	1 BRICK 32-bit, 33/66 MHz
PCI Arbitration on chip	No	Yes	Yes
PCI buffers	Implemented with multi-level flip-flops. Direct interface implemented with unprotected RAM	Unprotected	Protected
Ethernet	2 x 10/100/1000 Mbit	2 x 10/100/1000 Mbit	2 x 10/100/1000 Mbit
On-chip memory for RAM testing purposes (memory for software and others via AHB interface)	Dimensioned	Yes	Yes
On-chip buffers	Protected RAM (except EDCL debug)	Unprotected RAM	Protected RAM
On-chip Debug communication Link (DCL)	8K 512 72 SYNCRAM 8K 512 72 SYNCRAM	8K 512 72 SYNCRAM 8K 512 72 SYNCRAM	8K 512 72 SYNCRAM - 2Y 8K 512 72 SYNCRAM - 3F
Ad Processors			
Up to Bypass Router Links	No	No	Yes
GPU Controller	16PCI 1866, manufacturer	16PCI 1866, manufacturer	16PCI 1866, manufacturer
UARTs	2 x APBUART	2 x APBUART	2 x APBUART
General purpose timers	1x5 + 4x4	1x5 + 4x4	1x5 + 4x4
Timer latch compatibility	Yes	No	No
Watchdog output	Yes	Yes	Yes
Watchdog standard circuitry by to put clocks to unlock PLL related sources	Yes	No	No
GPIO	16 + 22 dedicated pins (additional GPIO port peripheral included backup)	16	16
GPIO bypassing mechanism by software and hardware events	Yes. Timer ticks and latch events can toggle GPIO.	No	No
GPIO interrupt assignable and interrupt routing registers	Yes	No	No
GPIO logical or, and, nor registers	Yes	No	No
Interrupt controller	32IQ APIC P	32IQ APIC P	32IQ APIC P
Interrupt synchronization	Yes	No	No
Timer system synchronization scheme (TSS_A/B) from software and hardware pulse and timer timestamp	Yes	No	No
Performance counters	Yes	Yes	Yes
LAHB statistics unit			
GR1553B TDP controller	Yes	No	No
Number of partitions on one interface to LAHB	16	4	4
Performance monitor events from Header RD bus	Yes	No	No
Performance monitor events for AHB RESERVED	Yes	No	No

Feature	GR740	LEON4-NGX	NGMP
Performance monitor events per monitor from 1-2 modes	Yes (for bit, rates, access)	No (combined for all monitors)	No (combined for all monitors)
Performance monitor events for 1-2 modes EDAC	Yes	No	No
Performance monitor latching and Timestamp	Yes	No	No
Register RD frame buffer filters for MEM RW sequence	Yes	No	No
Spacewire debug list	Yes, separate RREPW2	Yes, separate RREPW2	Yes, separate RREPW2
GRD debug list	No	Yes	Yes
JTAG debug list	Yes	Yes	Yes
Ethernet debug list	Yes [2x]	Yes [2x]	Yes [2x]
Ethernet debug list same as disabled via separate breakdrop	Yes	No	No
DEBUMBI trace buffer size	4 KB	4 KB	4 KB
Instruction trace buffer size	8 KB	4 KB	4 KB
Instruction trace buffer can be written via DRU register IF	Yes	No (just at bus)	Yes
Instruction trace buffer can be read or bits processor is running	Yes	No	No
Instruction trace buffer overflow disabled	Yes	No	No
GRD trace buffers emulated after reset	Yes, when DSUEN='1' and DSUBR='0'.	No	No
Debug mode clock gated by DSUEN	Yes	Yes	Yes
Reset and standby scheme	Single reset input is connected to all internal blockers and clock domains (including PCI, Ethernet, MIL-STD-1553B and SpaceWire) reset lines. Checking scheme differs from MIL-STD-1553B specification. Error reset command and clocks stored for debug.	Multiple reset inputs for different interfaces. Checking scheme differs from MIL-STD-1553B specification. Error reset command and clocks stored for debug.	Multiple reset inputs for different interfaces.
Clock gating cell	Yes, connected to other manual gating of multiplexed portions.	Yes	Yes
FPU clock gating controlled separately from CPU clock	Yes	Yes [for shared FPU]	No
Dynamic PLL control	Yes	Yes	Not specified
Dynamic Port control	Yes	Yes	Not specified
Pin multiplexing	Yes	No	Yes (between DDR2 SDRAM and SDRAM)
Temperature sensor	Yes	No	No
General purpose register for breakdrop signals	Yes	No	No

PLIT No No transactions

Difficulties faced during the work

- Specification
  - Trade-off for a general purpose microprocessor.
  - Multi-core aspects. Issues poorly understood.
- Increased verification and software effort due to refresh of RTL after activity was put on hold
- Creating a representative (timing accurate) simulator for GR740 based on existing simulator framework
- Trade-off between radiation hardening strategies
- Performance (timing) optimisations
- Disconnect between target technology development and needs/requirements on microprocessor device.
- Hit-under-miss-processing extension to Level-2 cache
- GLS: Several Mbit of memory, signal init (6h on core i7, later improved), default timing checks in sim lib introduced ’X’es

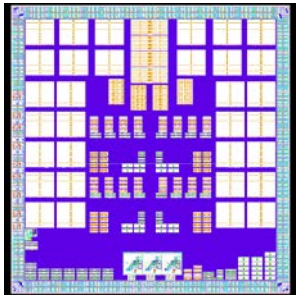
Implementation results

- Toolflow
  - FE: DC+DFT Compiler, Formality, TetraMax, Questa/RivieraPRO, Avery Design SimXact
  - BE: Standard ST flow
- Timing (worst-case, TBC)

  System clock: 250 MHz SpaceWire clock: 400 MHz

  SDRAM clock: 75 MHz Ethernet GTX clock: 125 MHz

  PCI clock: ~50 MHz (limited by IO timing)
- Power estimate (worse than worse-case): [redacted]
- Design complexity:
  - 15(+) clock domains
  - SRAM bits: 25281728 (25.3 Mbit, 3 MiB), 268 instances
  - Hard FFs: 130k Soft FFs: 93k Comb+ICG: 773k
  - Buf/inv: 157k PLLs: 3 Pads: 152



Benchmark Results

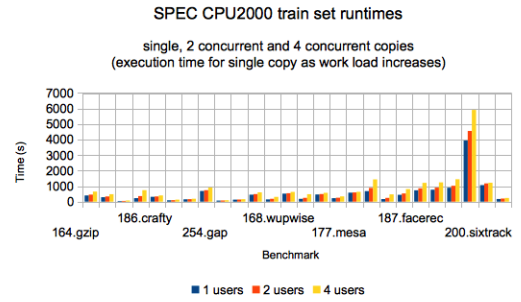
- LEON4 datasheet performance: 1.7 DMIPS/MHz, 2.1 CoreMark/MHz
- Results from technical note, released December 2010

Benchmark	AT697	UT699	GR712RC	NGMP
164.gzip	1	0.94	1.1	1.31
176.gcc	1	0.79	0.97	1.3
256.bzip2	1	0.93	1.06	1.33
AOCS	1	1.2	1.52	1.79
Basicmath	1	1.3	1.46	1.62
Coremark, 1 thread	1	0.89	1.09	1.21
Coremark, 4 threads	1	0.89	2.05	4.59
Drystone	1	0.94	1.05	1.39
Drystone, 4 instances	1	0.94	1.61	4.81
Linpack	1	1.2	1.26	1.71
Whetstone	1	1.94	2	2.22
Whetstone, 4 instances	1	1.94	3.7	8.68

Table 2: Performance comparison

Benchmark Results: Multi-Core

(Slide from 2012)



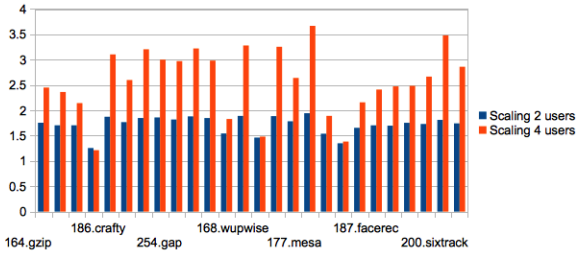
(Pessimistic) Average of scaling measurements:

Activating one additional core gives speed-up of 1.6 (range 1.3 – 1.94)

Activating three additional cores gives speed-up of 2.4 (range 1.2 - 3).

.. in tests where workload is multiplied with number of cores!

Test is pessimistic as all (sequences) of accesses to shared resources will occur simultaneously.



Benchmark	Two parallel instances			
	System A (Ideal speedup)	System B	System C WS	System C SPLIT
164.gzip	1.25	1.11	1.08	1.06
175.vpr	1.25	1.08	1.04	1.02
176.gcc	1.25	1.12	1.09	1.08
181.mcf	1.25	1.05	1.02	**0.99**
186.crafty	1.25	1.03	**0.97**	**0.96**
197.parser	1.25	1.17	1.16	1.12
252.eon	1.25	1.09	1.04	1.04
253.perlbmk	1.25	1.07	1.02	1.01
254.gap	1.25	1.16	1.12	1.11
255.vortex	1.25	1.12	1.09	1.08
256.bzip2	1.25	1.18	1.17	1.13
300.twolf	1.25	1.12	1.10	1.06
168.wupwise	1.25	1.23	1.23	1.19
171.swim	1.25	1.10	1.09	1.04
172.mgrid	1.25	1.23	1.23	1.17
173.applu	1.25	1.22	1.22	1.18
177.mesa	1.25	1.24	1.24	1.23
178.galgel	1.25	1.10	1.09	1.06
179.art	1.25	1.19	1.18	1.03
183.equake	1.25	1.19	1.18	1.09
187.facerec	1.25	1.20	1.20	1.18
188.ammp	1.25	1.17	1.16	1.10
189.lucas	1.25	1.22	1.22	1.19
191.fma3d	1.25	1.12	1.09	1.08
200.sixtrack	1.25	1.22	1.21	1.20
301.apsi	1.25	1.19	1.18	1.15

Table 2: SPEC CPU2000 speedup

- Other benchmark efforts: Dedicated FPU vs. shared, LEON double clocking, IO traffic routing, ...

	No SPLIT, 128-bit		SPLIT, 128-bit		No SPLIT, 32-bit		SPLIT, 32-bit	
Total	149194338		97371011		388420963		85449832	
CPU0	2579067	1.73%	2579067	2.65%	2579067	0.66%	2579067	3.02%
CPU1	2578234	1.73%	2578311	2.65%	2578184	0.66%	2579281	3.02%
CPU2	2578256	1.73%	2578326	2.65%	2578206	0.66%	2578169	3.02%
CPU3	2639689	1.77%	1365166	1.40%	2639641	0.68%	595467	0.70%
AHB utilization:		6.95%		9.35%		2.67%		9.75%
"Fair" speed-up:			1.34				3.65	

Benchmark results: EM / GR740

SPEC Benchmarks

- Impossible to exactly prototype GR740 system on FPGA for SPEC benchmarks
  - Not enough on-chip RAM on FPGA to implement 2 MiB L2-cache
  - FPGA boards using SDRAM do not have enough RAM to run SPEC
  - Different AHB/memory clock ratio when using DDR memory
  - Only the training set can be run within reasonable time
- General conclusion looking at multiple benchmarking campaigns during development:
  - We expect 10-15% improvement/MHz in SPECint/fp compared earlier LEON3 components in single-CPU case
  - Speedup of 2.54 measured when running 4 separate, independent, copies in parallel on 4 cores compared to 4 copies in sequence on 1 core.
    - Less than the ideal of 4.0 because of contention for L2 cache, effectively size reduced to 1/4 for each benchmark instance.
  - Together with frequency increase (from ~100 to 250 MHz), this gives about 600% improvement in processing power on SPEC-type applications compared to UT699/GR712 in single-core
- To be benchmarked on the real silicon

Outputs

Deliverables to ESA

- Architecture Exploration Report
- **NGMP Specification**
- Development Plan
- SEE Mitigation Plan
- Feasibility Report with Spreadsheet
- Software Requirements Specification
- Architecture Definition Report
- Verification Document
- Preliminary NGMP Data sheet
- Documentation of Changes/Configuration of OS, Compiler and the Drivers
- **Technical Note on NGMP Evaluation**
- Preliminary Radiation Report
- Technical Data Package
- **Abstract and Executive Summary**
- **FPGA board with FPGA database**
- **High-level simulation models**
- Architectural Design Database
- Software databases
- Test database

- Detailed Design Database
- Detailed Design Document
- Layout Design Document
- **Preliminary datasheet for ST65 Prototype Implementation**
- **Bitstream for FPGA board – representative of full NGMP**
- **Bitstream for FPGA board – representative of GR740**
- Final design database

- Detailed block diagram (addition)
- ST65 ASIC Design Description (addition)
- ST65 DFT Specification (addition)
- **GR740 Comparison Document (addition)**

Bold = Public (free/non-free)

Lessons learned

- Requirements and feedback are valuable but difficult to obtain
- Release prototypes early
  - Go for SW development and porting of existing applications
  - Minimize number of different FPGA configurations
- Early trials: don’t forget the IOs
- Keep space volumes in mind for DFT
- Try (harder) to align backend iterations with FE deliveries
- Watch out for swapping of RH elements (happened, checks were in place)

Summary, Outlook and Conclusion

- To develop a microprocessor (NGMP) with higher performance than earlier European space-microprocessors: Check
- NGMP Phase 2 (GR740) started, PG estimated for Friday CW24
  - Radiation hardening measures, manufacturing on C65SPACE
  - Package ”qualifiable”
  - Possiblity to take EM silicon to FM
- NGMP/GR740 already in use through FPGA prototypes and functional prototype
- Multi-core aspects being evaluated – more work needed
- Technology advancement may provide gains for ”small” design revision:
  - Memory interface, Communication interfaces, Computational perf.
- Extensions and improvements also available through IP

Thank you for listening!

Questions?

Latest status of GR740 development:
http://www.gaisler.com/gr740