AGGA4

(Advanced GPS/Glonass and Galileo ASIC)

Isaac Tejerina, Airbus D&S
Mohsin Syed, Airbus D&S
Paul Rastetter, Airbus D&S
1st June 2015

AIRBUS
DEFENCE & SPACE

Agenda

- AGGA4 Overview
- AGGA4 Implementation Details
- Project Challenges
- Final Results
- Conclusion

AIRBUS DEFENCE & SPACE

AGGA4 Overview

AIRBUS DEFENCE & SPACE

AGGA4 Background

- In 2000, the AGGA2 was developed and made available as an Atmel product (T7905E).

- In 2003, the development of AGGA3 based on the AGGA2 architecture was started. However:
  - Feasibility-check in ATC18RHA technology confirmed that the implementation was not possible.
  - Continuous re-definition of the Galileo signals meant that the AGGA3 design needed significant modifications.
  - AGGA3 was therefore never manufactured.

- In 2008, the development of AGGA4 started which included the design adaptations required by Galileo. The AGGA4 devices are again planned to be made available as an ATMEL ASSP (Application Specific Standard Product).

- Functionality of AGGA designs:
  - AGGA2: Limited GPS & Glonass; off-chip ADSP 21020 processor.
  - AGGA3: GPS + Glonass + limited Galileo; LEON2-FT processor, more interfaces.
  - AGGA4: All GNSS signals; LEON2-FT processor; space-specific interfaces.

AIRBUS DEFENCE & SPACE

AGGA4 ASIC Development - Overview

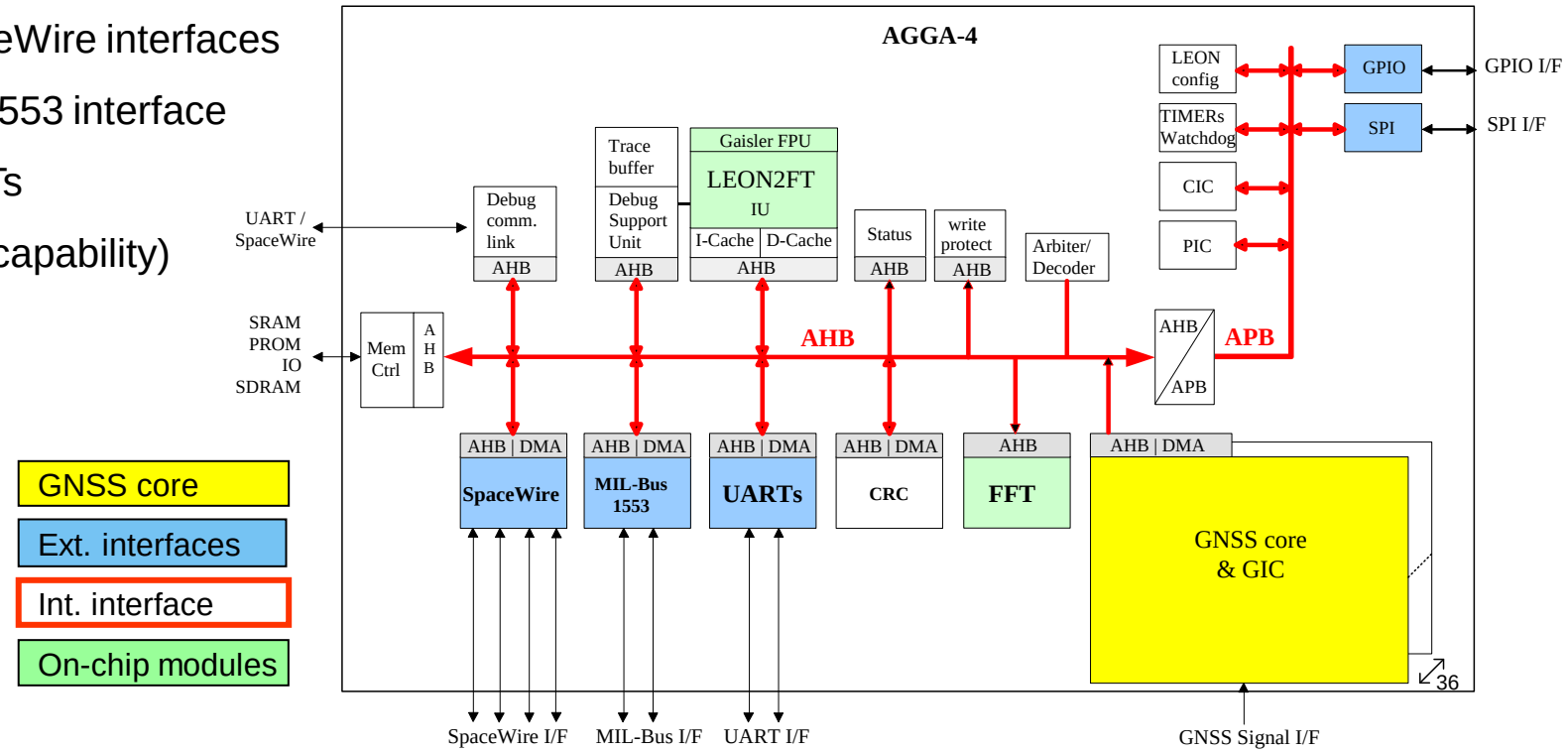
- The activities under AGGA4 development in ESA Contract 16831/03/NL/FF were performed by an industrial team composed of:
  - Airbus DS GmbH in Ottobrunn, as the main Contractor towards ESA.
  - RUAG Space GmbH as Sub-Contractor.
  - Atmel involved as an external service provider to perform the foundry related activities and to provide support.

- The ASIC is capable of processing modernized GPS, Galileo and others GNSS systems like Glonass and Compass.
- Target applications:
  - Precise Orbit Determination (POD)
  - Radio Occultation

AIRBUS DEFENCE & SPACE

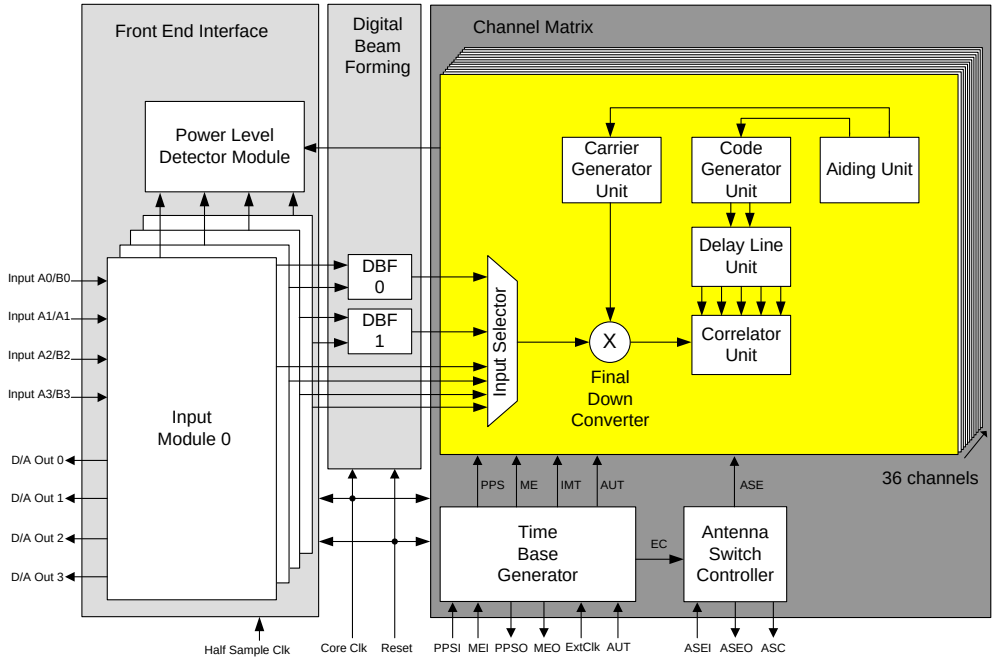
AGGA4 Architecture

- LEON-2 Fault Tolerant processor including Gaisler Research Floating Point Unit (GRFPU).
- On-chip AMBA APB and AHB busses.
- External SRAM memory Interface.
- Hard-coded 128 point 32-bit fixed-point FFT unit.
- Interfaces:
  - 4 x DMA capable SpaceWire interfaces
  - DMA capable Mil-Std-1553 interface
  - 2 x DMA capable UARTs
  - SPI (master and slave capability)
  - RF front-ends
  - 32 bit GPIO



GNSS Core Architecture

- Interfacing with up to 4 RF Front-ends
- Digital Beam-forming unit
- 36 single frequency double code GNSS channels
  - Aiding functionality for all channels (code and carrier aiding for autonomous NCO update)
  - Flexible primary code generators (LFSR and memory based)
  - Support of Binary Offset Carrier and secondary codes



AIRBUS DEFENCE & SPACE

GNSS Channel Characteristics

- Embedded memory 1280x8 bits, combined with LFSR to support all open GNSS signals.
- Dual Code Capability (Pilot and Data Tracking in one channel).
- Flexible Integration Length for Pilot and Data independently.
- Flexible Delay Line to support different correlator spacings.
- Autonomous Update of Code and Carrier NCO by HW (Aiding Unit).
- Slaving capability of multiple channels.
- DMA transfer of measurement observables.

AIRBUS DEFENCE & SPACE

AGGA4 Implementation Details

AIRBUS DEFENCE & SPACE

AGGA4 Verification Strategy

- RTL Simulations (VHDL)
- FPGA based verification using Xilinx Virtex 5 boards.
- FPGA version only includes 4 Channels and runs at 40 MHz.
- Design verification performed by three independent Teams:
  - RUAG Space Austria
  - Astrium GmbH
  - Deimos
- ASIC Backend netlist verified by formal verification tool and gate level simulations.

AIRBUS DEFENCE & SPACE

Backend Design Challenges

- Operating frequency challenging due to large size of design.
- Critical paths located in Leon2FT processor. It was slightly adapted compared to Atmel AT697 Chip.
  - Register File implemented in SEU-hardened flip-flops saving RF-EDAC and avoiding falling-edge triggered path.
  - Random replacement strategy used in multi-set cache controller, avoiding the storage and comparison with the allocation history.
- Even after the optimization step: routing congestion, degraded hold-fix, voltage drop and cross-talk issues were observed and then fixed.

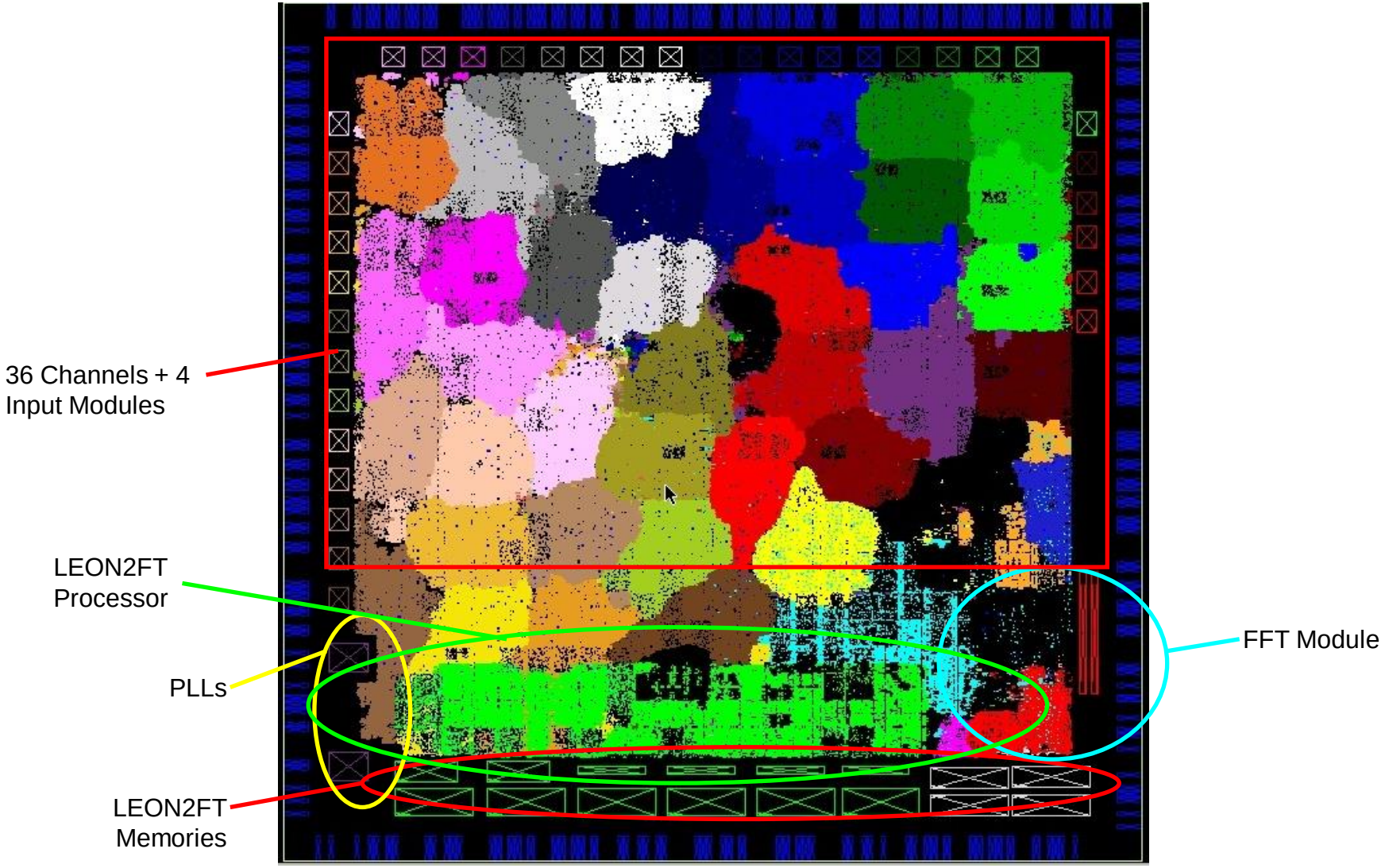
AIRBUS DEFENCE & SPACE

ASIC Backend Design

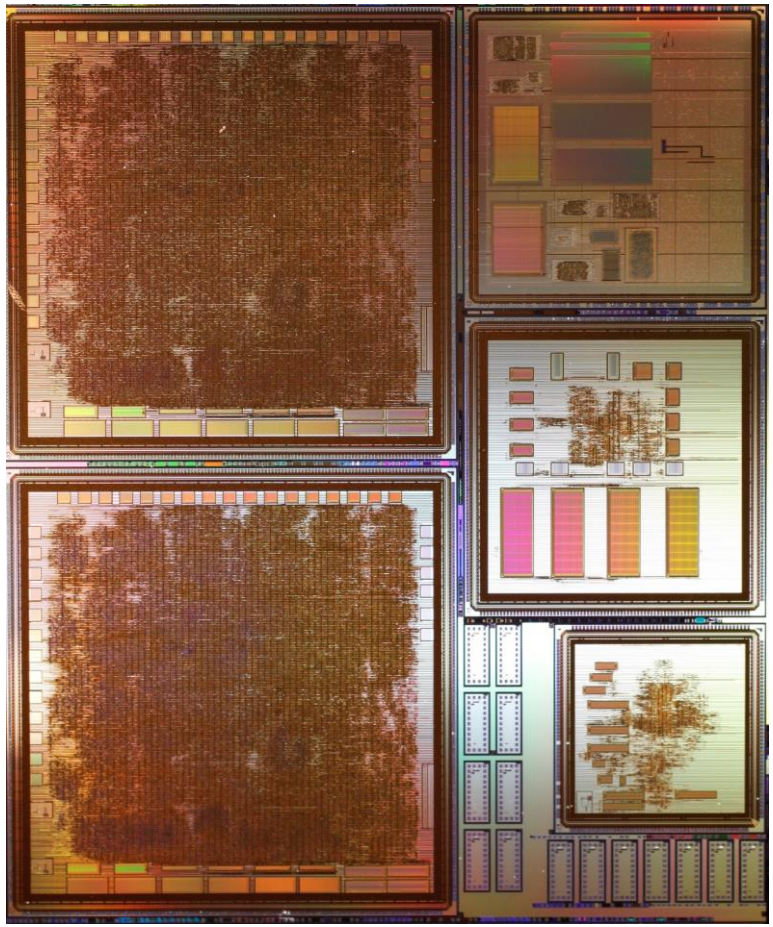
- ASIC manufactured in radiation hardened 180 nm process ATC18RHA MPW from Atmel.
- MQFP package with 352 pins.
- ASIC design on the upper limit of technology.
- Approx. 4.6 M gates pre-layout (without pads).
- Approx. 6.1 M gate post-layout final design.
- 67% of design corresponds to GNSS Core, where 95% are the 36 x GNSS Channels.
- All channel registers analyzed to determine impact of using hardened or non-hardened flip-flops.
- Approx. 20% of FFs are non-hardened.

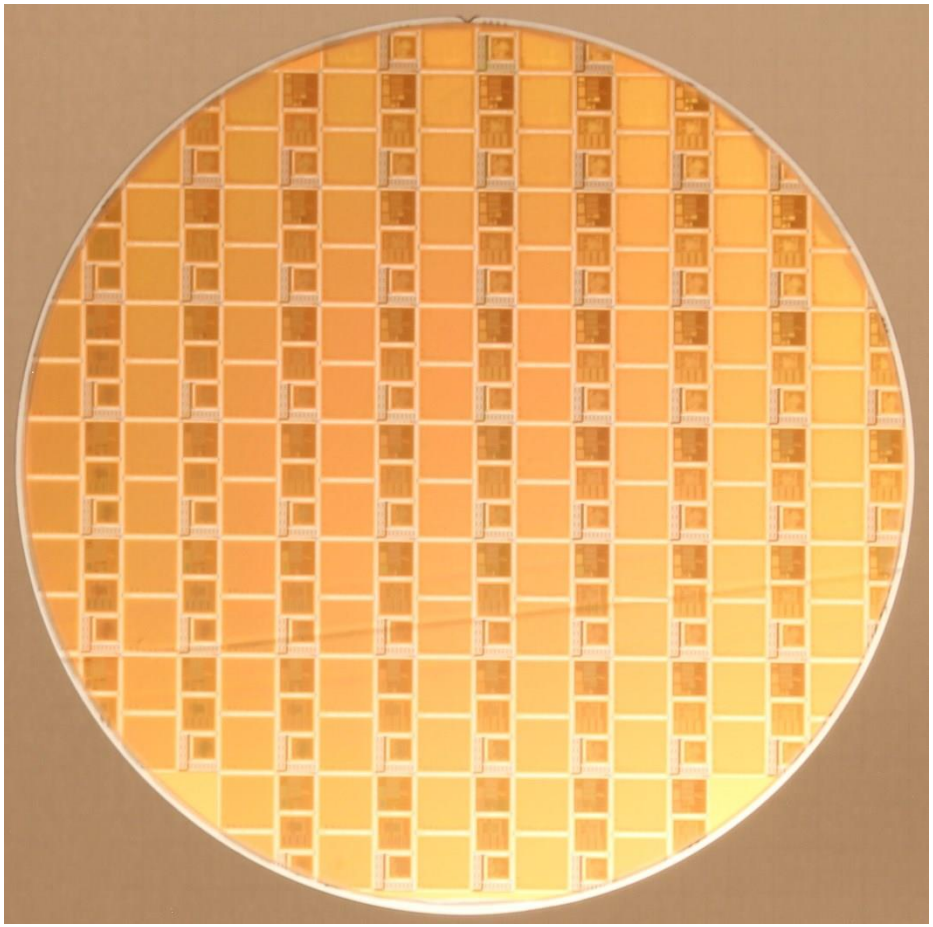
AIRBUS DEFENCE & SPACE

AGGA-4 Floorplan



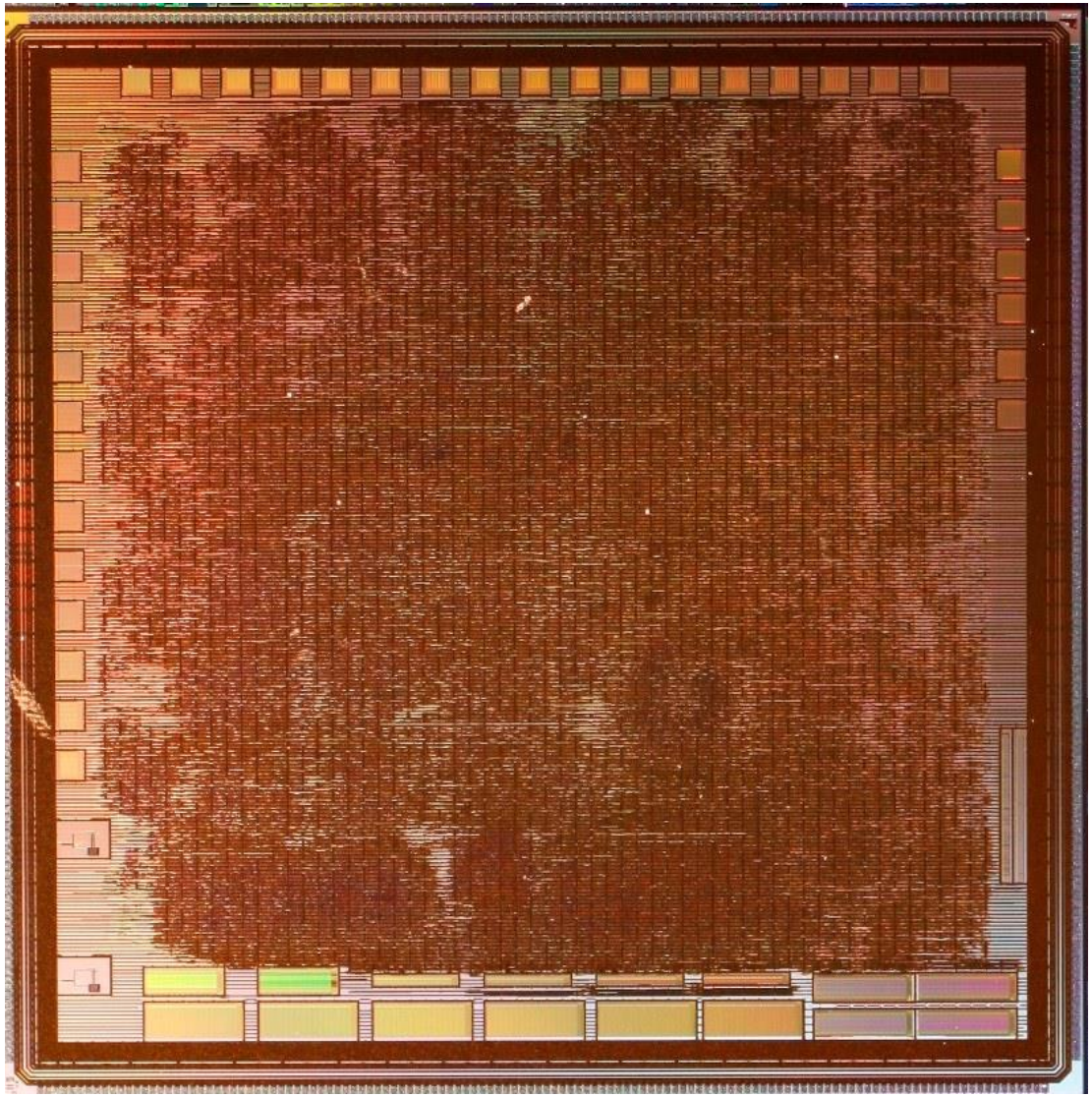
AGGA4A Reticle and wafer





AIRBUS DEFENCE & SPACE

AGGA4 Die



AIRBUS DEFENCE & SPACE

Project Challenges

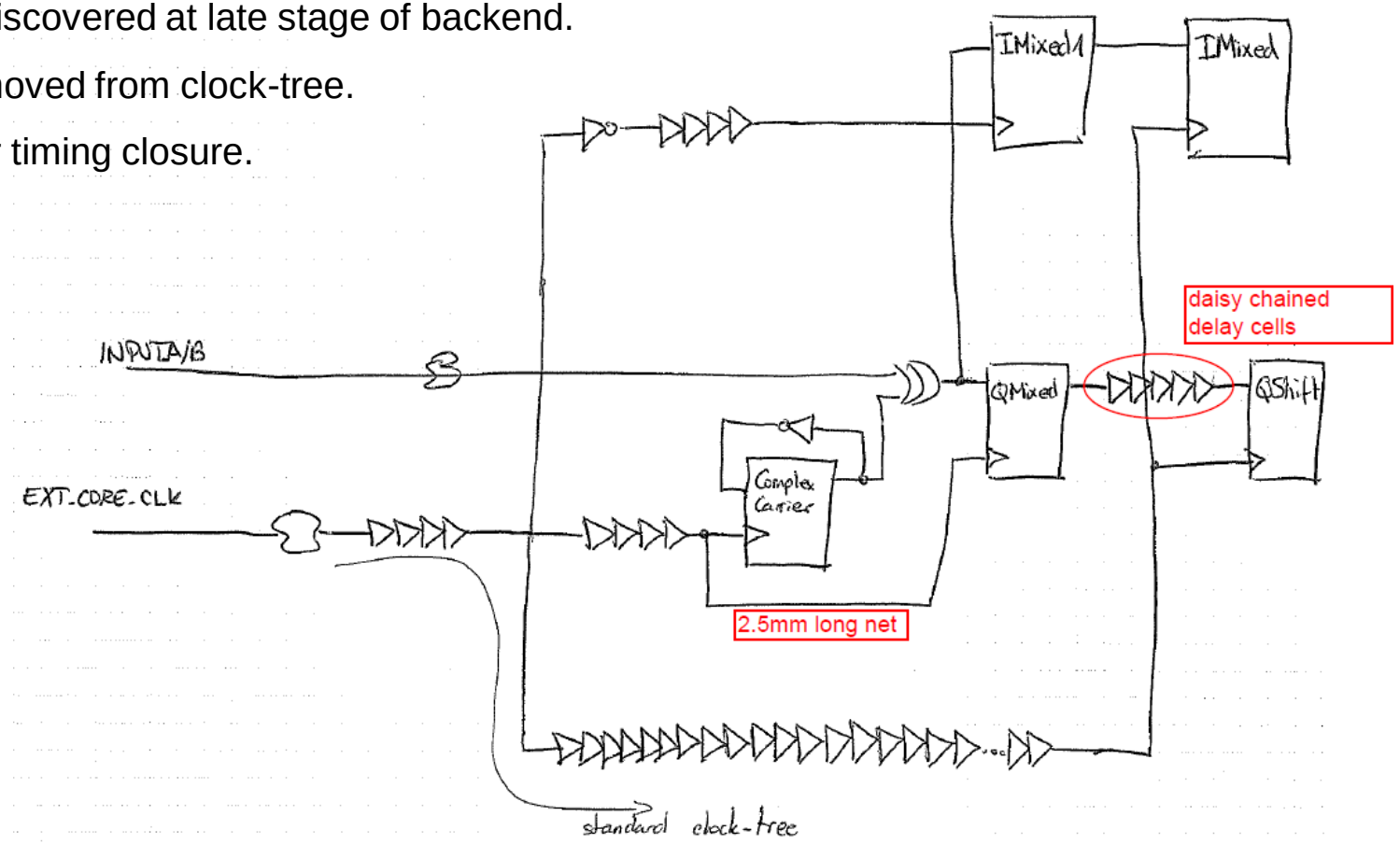
Challenges after 1st Manufacturing Run

- Fail in Production test at Atmel → DLY Cell characterization.
- FPU IP Bug.
- LUT Anomaly reported in libraries.
- Change of Foundry for the 2nd run.

AIRBUS DEFENCE & SPACE

DLY Cell Bug Fix (1)

- Clock tree synthesis performed for each clock domain.
- Latency 5 – 14 ns in GNSS clock (> 100K FFs).
- Input data timing violations discovered at late stage of backend.
- ECO required -> Registers moved from clock-tree.
- Use of Delay Cells chains for timing closure.



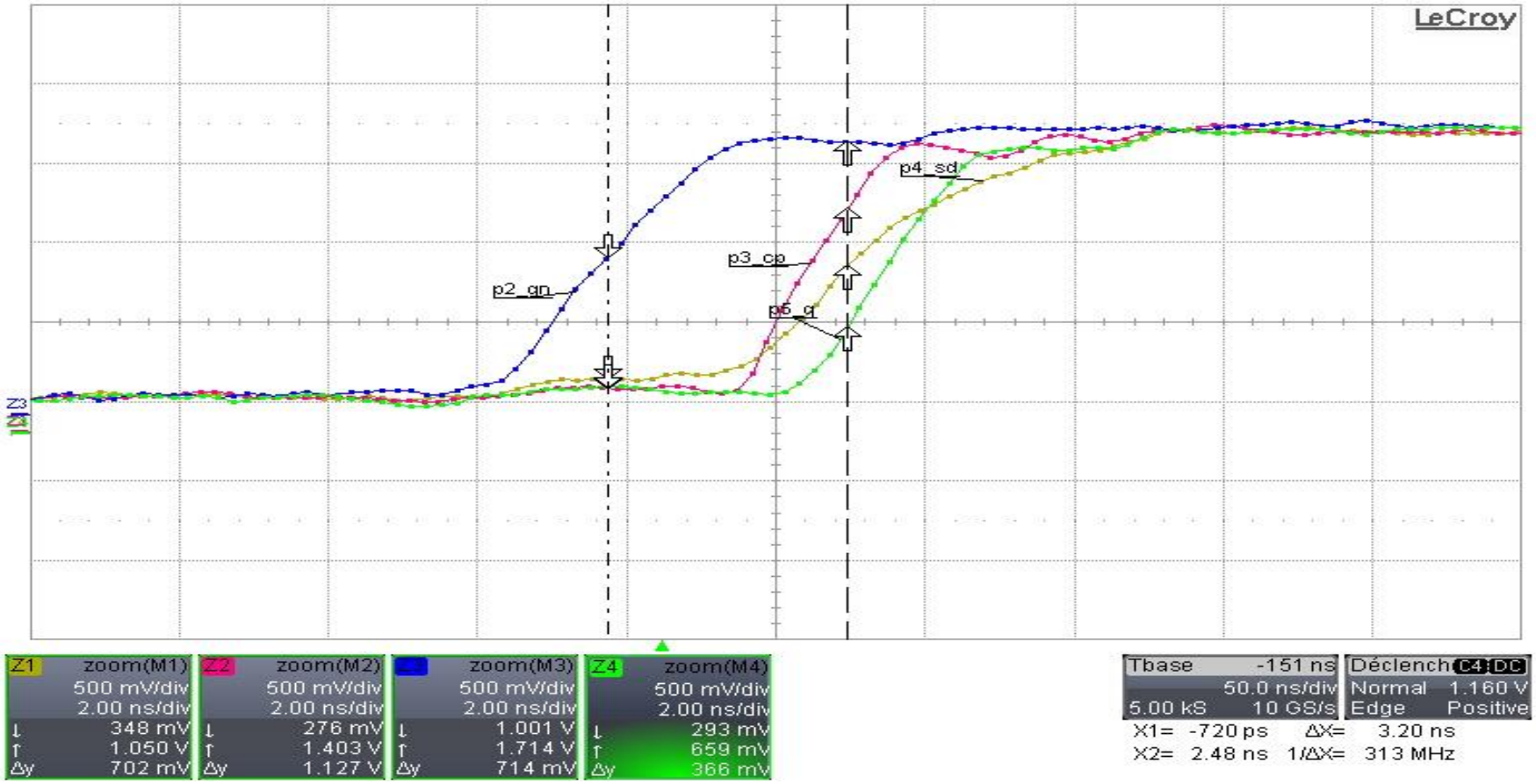
AIRBUS DEFENCE & SPACE

DLY Cell Bug Fix (2)

- ATPG tests and functional tests failed.
- Generated dedicated test vectors for debugging.
- Hold violations in the FFs moved from clock-tree.
- Micro-probing in chip for debugging performed at Atmel.
- Correction directly on chip. Connection broken after some tests in temperature, but it confirmed the root cause.
- Metal Fix implemented.

AIRBUS DEFENCE & SPACE

DLY Cell Bug Fix (3)



Red line is the clock input and yellow line in data input.

- P4 changes sooner than expected. Should change 400ps later.
- P2 and P4 slope cannot be compared as P2 has less output load than P4

AIRBUS DEFENCE & SPACE

DLY Cell Bug Fix (4)

- Problem confirmed to be located in the chain of DLY cells.
- Individual DLY Cells were characterized, but the DLY cells chain were not.
- Characterization of DLY Cell chains was performed by Atmel, but the updated timings were not updated in the library.
- After metal fix, additional margin added for hold timing:

		1st run (before)		2nd run (after)	
Path start point	Mode	Min	Max	Min	Max
QMixed (setup)	Functional	18.19	16.79	17.71	15.20
QMixed (hold)	**Functional**	**0.47**	**0.61**	**0.94**	**2.20**
QMixed (setup)	Scan	128.28	126.77	127.86	125.72
QMixed (hold)	**Scan**	**0.16**	**0.59**	**0.70**	**1.91**

- The final implementation compensates more than 20% deration in DLY Cells.

AIRBUS DEFENCE & SPACE

FPU Fix (1)

- During validation of ASIC prototype, observed functional problems in FPU.
- FPU is an IP delivery in two Netlists:
  - EDIF format for Xilinx prototype
  - Verilog Netlist for ASIC
- Confirmed that EDIF netlist was correct, but Verilog netlist was incorrect generated.
- FPU IP was only verified in detail in FPGA version.

FPU Fix (2)

- Analysis carried-out by Airbus DS and Aeroflex Gaisler.
- Hardware fix suggested by Aeroflex Gaisler.
- Implementation of the bug-fix is located in an area with high gate density and timing critical.
- Hardware fix and incorrect FPU mapped in RTL level.
- New FPGA version created with the same error as in ASIC to confirm root-cause.
- Verification of the FPU Fix based on:
  - RTL simulations
  - Gate level simulations
  - FPGA model tests
  - Equivalent check
  - Static Timing Analysis (STA)
  - Additional FPU tests added for RTL, Gate Level and functional test vectors.

AIRBUS DEFENCE & SPACE

LUT Anomaly (1)

- In 2013, Atmel created an “8D Corrective Action Report” for the ATC18RHA technology.

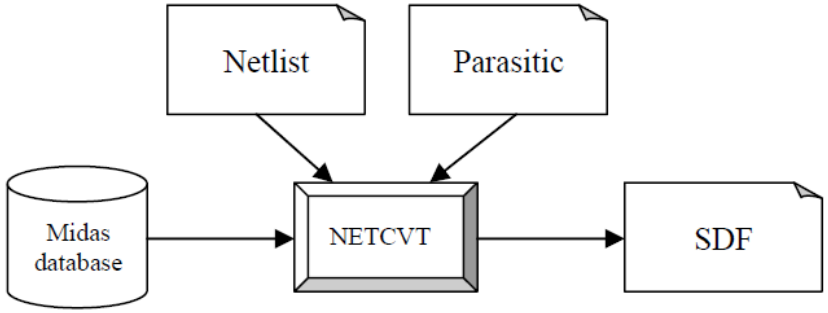
- *“On January 22nd 2013, during the development of a circuit and trying to find the reason why some severe violations remain during the Static Timing Analysis step after layout although the P&R task has been completed with minor violations, it has been found that the tables including the margins (setup timing checks) to insure the correct behaviour of the sequential cells have been translated in a wrong way from the characterization tool to the files needed for synthesis to P&R including STA, simulation, aka .lib file.”*

- AGGA4 is affected by this anomaly.

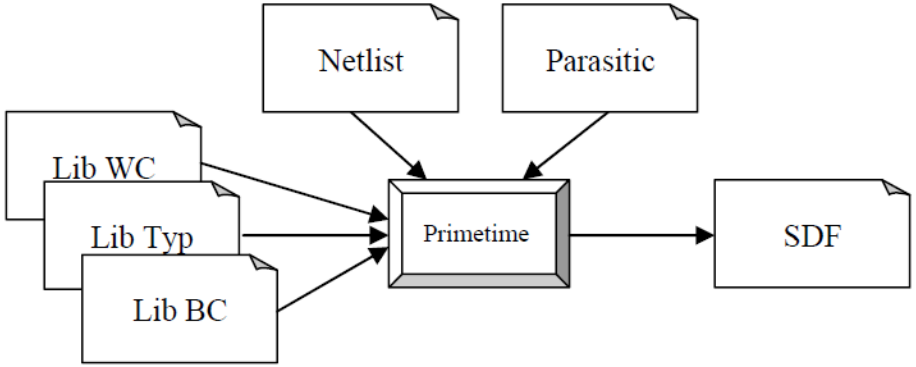
- The setup time of flip-flops are not correctly characterized. It leads a timing violations in high frequencies.

LUT Anomaly (2)

- Root cause based on the incorrect setup time LUT generated.
- Old generation flow:



- For AGGA4, the SDF file was generated using a different flow, using PrimeTime instead of the Atmel standard tool:



AIRBUS DEFENCE & SPACE

LUT Anomaly (3)

- New timing files (SDF) were generated.
- STA repeated and setup timing violations reported using maximum frequency (90 MHz) scenario.
- Violations were identified, but are located only in three paths.
- After analysis, it was concluded that:
  - The area is critical and any change can have consequences in other paths.
  - In this area on the Die, there are fewer spare cells available than those required for a metal fix.
  - The final conclusion was that a metal-fix only on AGGA4 was not feasible.
- Atmel tried to assess fixing these timing violation using a full mask-layer fix.
- Atmel later confirmed that it is possible the correction but this fix was discarded due to the high risk involved.
- Impact of this anomaly is the loss of 4 MHz in performance.

AIRBUS DEFENCE & SPACE

AGGA4 2nd Run Manufacturing

- Once all the previous problem was solved, 2nd run was planned.
- A new problem came up:
  - LFoundry has filed for insolvency protection in France.
  - ATMEL could not manufacture any more in Le Rousset (France)
  - The manufacturing of the second run had to be transferred to UMC (Taiwan).
  - Atmel's UMC qualification performed under supervision of ESA and CNES (see next Slide).
- The Technology transfer was performed successfully
- AGGA-4b (2nd run) was manufactured.

AIRBUS DEFENCE & SPACE

Qualification of the UMC Process by Atmel

Certificates

ESA and DLA Certifcates

- Certificate ESCC QML by ESA vs ESCC25400 std valid in Jun-14 until Aug-16
- Certificate QMLV by DLA vs MIL-PRF-38535 std expected in Sep-14
- Certificates based on

DELIVERABLES	TCV	REPORT #
WLR	PM	2013_EC_079
Etest Matching	MPW/AT	2014_EC_084
Electrical Characterization	V40,47	2014_EC_085
Radiation test qualification • TID (PCM and SEC) lots 1&2 • TID Milanion • SEE (SEC)	 V40, PM V40 58C06,V40	 2013_EC_043 2013_EC_044 2013_EC_059,45
Device reliability • HTOL 4000H 125°C Group C • electrical LU • ESD HBM/CDM	 V40 V47 V47	 2013_EC_047 2013_EC_042 2013_EC_046
Package reliability • D-Group • Construction analysis	V40	 2013_EC_062 2013_EC_061
ESCC & MIL (DLA) ASIC ATC18RHA technology Documentation and qualification ready for certification		PID 032 Qualpack

european space agency
agence spatiale européenne

Certificate of Technology Flow Qualification No. 312A

This is to certify that ATMEL, Nantes, France has been qualified by ESA for the supply of Microcircuits, Silicon, Digital, CMOS, Cell Based, 0.18µm technology, based on ATC18RHA for use in ESA space programmes, according to the ESCC Qualified Manufacturers List, Basic specification 25400, Generic Specification 9000 and associated Detail Specification 9202/080.

This certificate is valid until August 2016.

Head of the Product Assurance and Safety Department

Date 6 June 2014

3 © 2014 Atmel Corporation Select Insert > Header & Footer > Type Title in Footer field 5/27/2015 Atmel

AIRBUS DEFENCE & SPACE

Final Results

AIRBUS DEFENCE & SPACE

Achieved Operating Frequencies

- Flexible clock generation:
  - With external clock: 10 – 90 MHz.
  - Generation of system clock with 40 MHz, 80 MHz using internal PLLs.
  - Generation of 16 MHz Milbus clock using internal PLL.
- System / Leon Processor: 90 Mhz (max)
- SpaceWire interface: 80 MHz
- GNSS Core: 50 MHz
- GNSS front end interface at sampling frequency 250 MHz

AIRBUS DEFENCE & SPACE

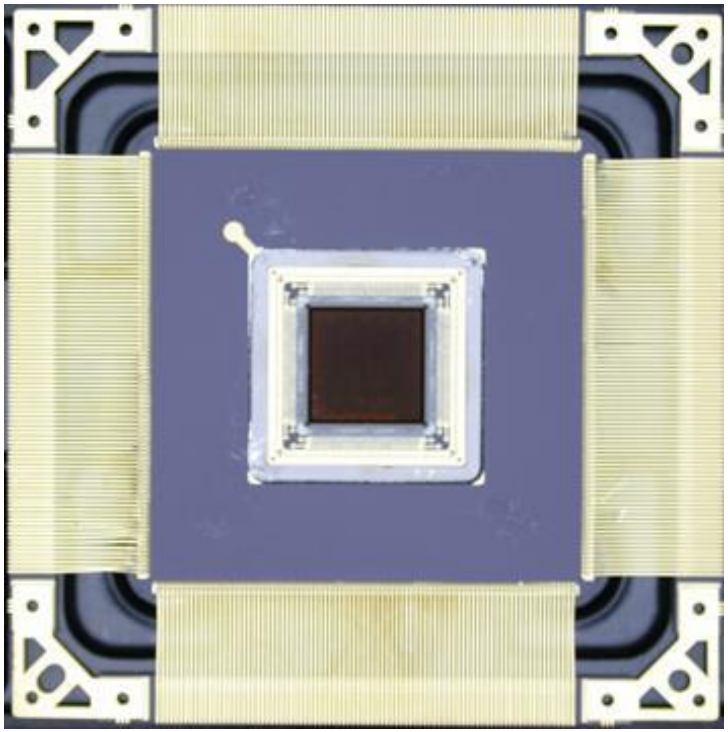
Power Consumption

- Estimated power consumption figures:
  - Core : 4.7 W @ 80 MHz
  - IO : 2.7 W @ 80 MHz
- AGGA4 allows the complete and independent deactivation of every Channel for power consumption reduction.

AIRBUS DEFENCE & SPACE

AGGA4b availability

- AGGA4b prototypes are currently available
- AGGA4b will be available as Application Specific Standard Product (ASSP) from Atmel.
- Availability of additional tools (e.g. commercial evaluation boards) is planned.



AIRBUS DEFENCE & SPACE

Conclusions

- AGGA4 includes:
  - enhanced GNSS signals from a larger number of GNSS systems (GPS / Galileo / Glonass, Compass-Beidou).
  - Increased on-chip functionality (e.g. processor, SpW, SPI, etc).
- AGGA4 is an enabler for the development of advanced multi-GNSS receivers.
- Device already used at R&D level (viz. GAMIR) and later at equipment level (viz. MetOP SG).
- Prospects for use in future missions, as well as in GEO Telecom satellites look very promising.
- The project has been long due to many reasons:
  - changes in the Galileo signal specifications.
  - complexity of this 6 Mgates device and its validation.
  - Failure of the 1st manufacturing run and consequently the 2nd manufacturing run.

But the walk was worth it!

AIRBUS DEFENCE & SPACE