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ADVANCED ELECTRONIC SOLUTIONS | AVIATION SERVICES | COMMUNICATIONS AND CONNECTIVITY | MISSION SYSTEMS

FDIR Validation Test-bed Development and Results

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FDIR Overview

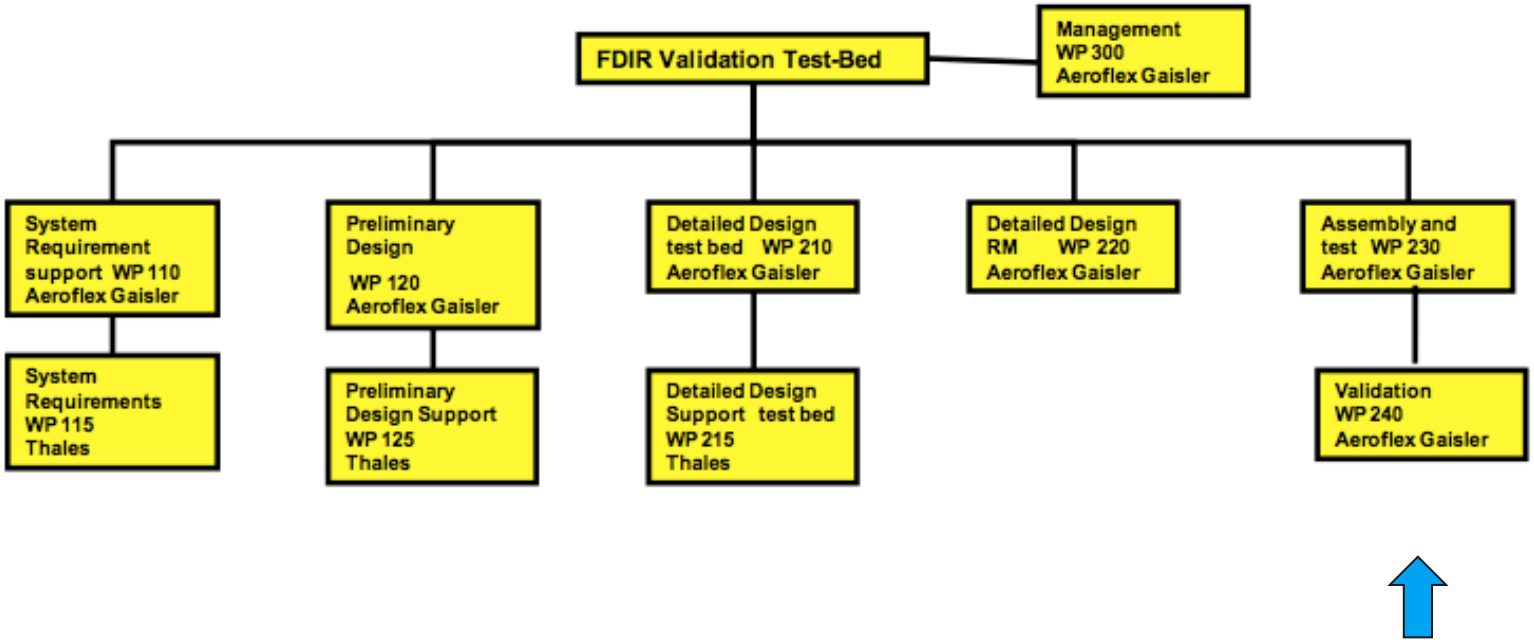
- Development of a FDIR Validation Test-bed is an activity initiated and funded by ESA/ESTEC under contract 4000109928/13/NL/AK.
- Cobham Gaisler and Thales Alenia Space France are to develop an extension of the existing avionics system testbed facility in ESTEC's Avionics Lab.
- The resulting FDIR testbed will allow to test concepts, strategy mechanisms and tools related to FDIR. Ultimately the purpose of the output of this activity is to provide a tool for assessment and validation at laboratory level.
- Team:
  - ESA: Farid Guettache, Gianluca Furano
  - TAS-F: Jean-Christian Nodet, Brice Dellandrea
  - Cobham Gaisler: Anandhavel Sakthivel, Alexander Karlsson, Martin Aberg, Sandi Habinc, Jan Andersson

Outline

- Activity flow
- Objectives
- Current RASTA system
- Work performed
- Test-bed
- Board design
- Reconfiguration Module
- Test-bed controller tool
- Summary

Activity Flow

- Simple waterfall:
  - Phase 1: System requirements, Preliminary Design
  - Phase 2: Detailed Design Development, Assembling, Integration and Test, Validation and test case

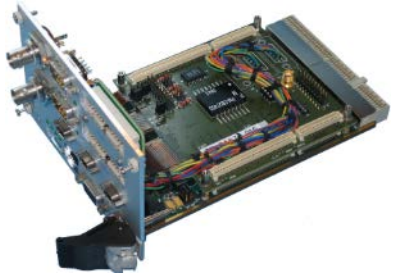


Objectives

- Extend the capability of the existing RASTA facility from a single string to a dual redundant string, supporting different redundancy schemes.
- Develop a test-bed controller software tool which enables the user to perform system-level emulation of full FDIR functionality using the RASTA facility.
- Engineering objectives:
  - Reuse the existing hardware as much as possible.
  - Design and develop a new RASTA module providing reconfiguration and safeguard memory.
  - Integrate the newly developed module in ESTEC's RASTA facility based on two identical chains, re-using the existing equipment.
  - test-bed controller software tool that enables the user to load, run and analyse applications and simulations, as well as inject error cases in the dual redundant system.

Current RASTA System

- RASTA system consisting of
  - Processor board: GR-CPCI-AT697
    - PCI, UART, ...
  - I/O board: GR-CPCI-XC4V



    - PCI
    - MIL-STD-1553B, CAN (redundant),
    - SpaceWire - three independent links with RMAP
    - 10/100 Ethernet, Discrete I/O, UART and JTAG debug interfaces
  - TMTC board: GR-CPCI-XC4V

    - PCI
    - ECCS/CCSDS TM and TC functions, including a CPDU which also has a PacketWire interface towards an external Reconfiguration Module. It also contains On-Board Time and support for automatic time transfer via SpaceWire.
- SW on processor board typically accesses peripheral units on I/O and TMTC boards through PCI

Work Performed

- Requirements established and mapped to RASTA building blocks
  - Review of FDIR architecture and characteristics in selected space missions TN 1-1
    - Covered SB4000, S1, S3, SAVOIR, L3G-AURUM
- Developed Hardware
  - GR-RASTA-FDIR: RM, SGM and CPDU inside FPGA. Mezzanine to support external interfaces
  - GR-CPCI-SPW4: New accessory board that consists of 4xSpW. Main purpose is to connect GR-RASTA-FDIR to GR-RASTA-TMTC with minimum changes to the latter system

Work Performed

continued

- Developed Reconfiguration Module IP core
- Updated GR-RASTA-TMTC
  - Connections to ensure that FDIR unit accessible from ground
- Interconnects between PM, TMTC and FDIR units
- Established Verification and Validation Plan
- GRMON2 support for LEON2
- Developed RTEMS drivers required for Reconfiguration Module and GR-RASTA-FDIR (PCI target driver).
- Controller tool development (Ongoing)
- Verification and Validation of the test-bed (Ongoing)
- Test application software development (Ongoing)

Test-bed

Single chain

- The configuration of each RASTA single chain contains:
  - Processor Module (PM) based on AT697E/F
  - I/O Module
  - Telecommand (TC) and Telemetry Module (TM)
  - FDIR Module with RM and Safeguard Memory
  - Crate with power supply

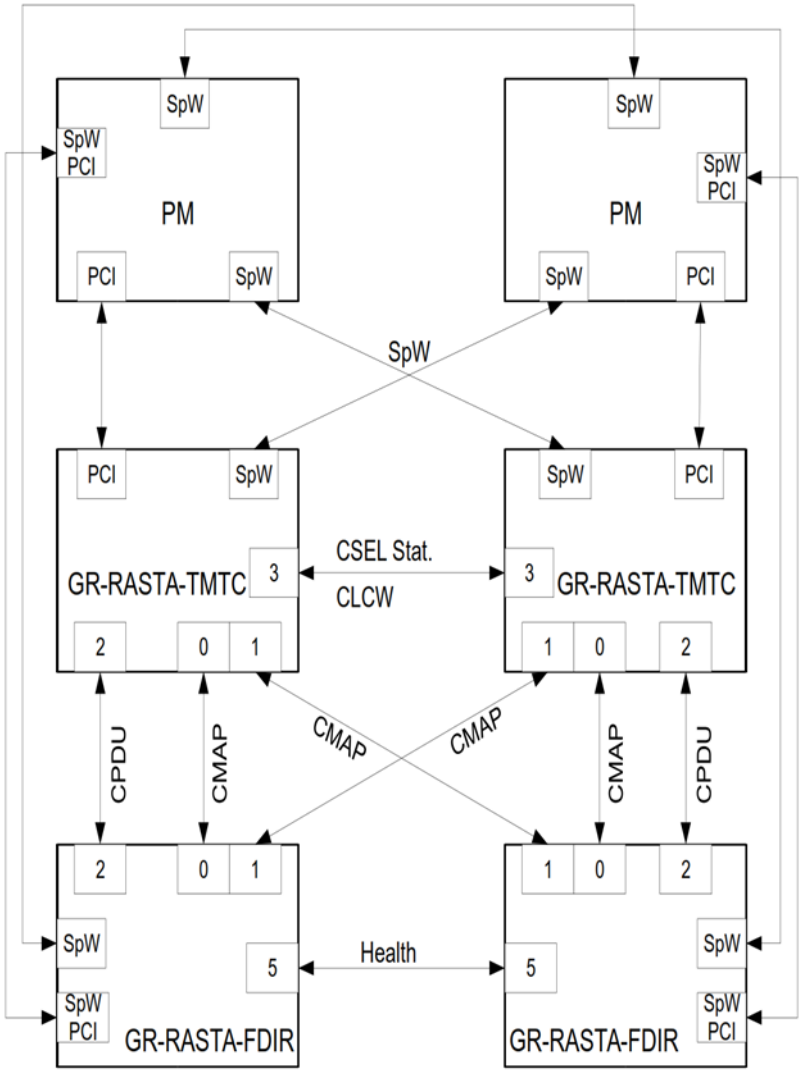
Test-bed

Single chain

Test-bed

Dual chain with interconnects

- PM here is LEON and GR-RASTA-IO
- PM - TMTC - FDIR
  - PCI bus is the main communication interface within each chain
  - While SpaceWire is used for cross-strap links
- FDIR 2 – TMTC 2
  - CPDU links encapsulated in a PacketAsynchronous interface
- FDIR 0 – TMTC 0
  - TC and TM communication FDIR and TMTC (direct link) that is encapsulated in a PA interface
- FDIR 1 – TMTC 1
  - TC and TM communication FDIR and TMTC
  - (cross-strap) that is encapsulated in a PA interface
- TMTC 3 N – TMTC 3 R
  - Link Between the TMTC modules carrying CLCW and CSEL Status
- FDIR 3 N – FDIR 3 R
  - Health communication between RM's



Test-bed

Dual chain

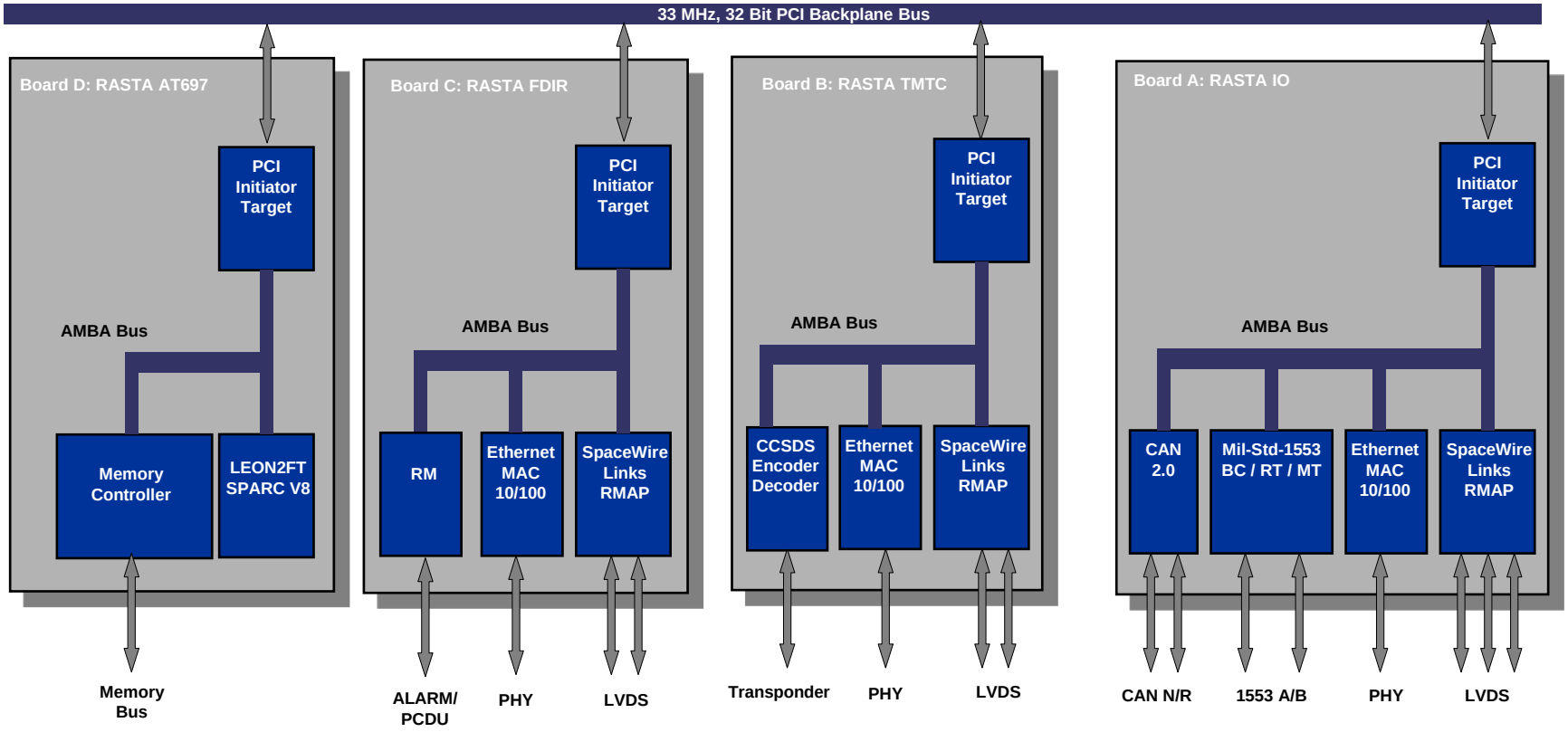
Test-bed

Dual chain with interconnects

cPCI Crate Arrangement

	PCI 1 (HOST)	PCI 2	PCI 3	PCI 4	PCI 5	PCI 6	PCI 7	PCI 8				
GR-CPCI-SER	GR-CPCI-AT697	GR-ACC-SPW4	GR-RASTA-FDIR		GR-RASTA-TMTC		GR-TMTC-PW	GR-RASTA-IO				GR-ACC-SPW4
1 (ACC → PCI 1)	2	3 (ACC → PCI3)	4	5	6	7	8 (ACC → PCI 5)	9	10	11	12	13 (ACC → PCI 5)

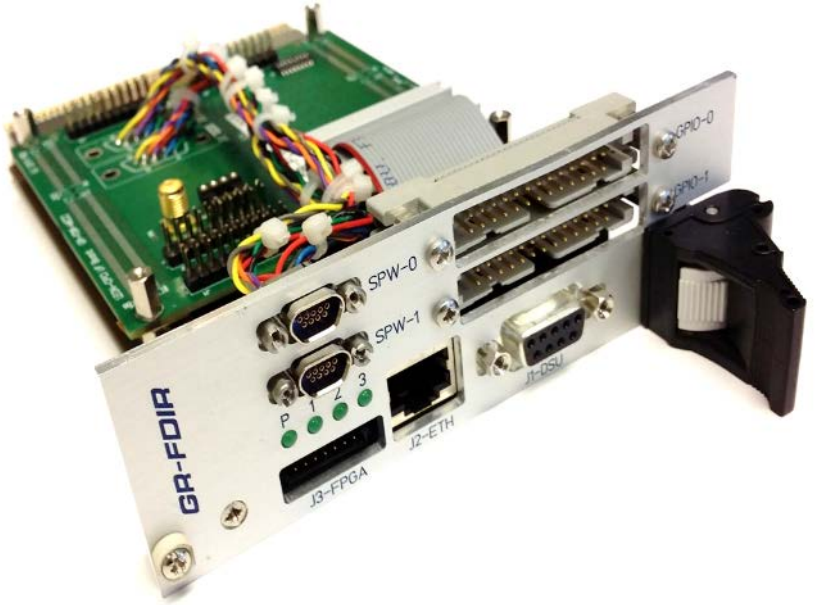
Block Diagram



Board Design

GR-RASTA-FDIR (1)

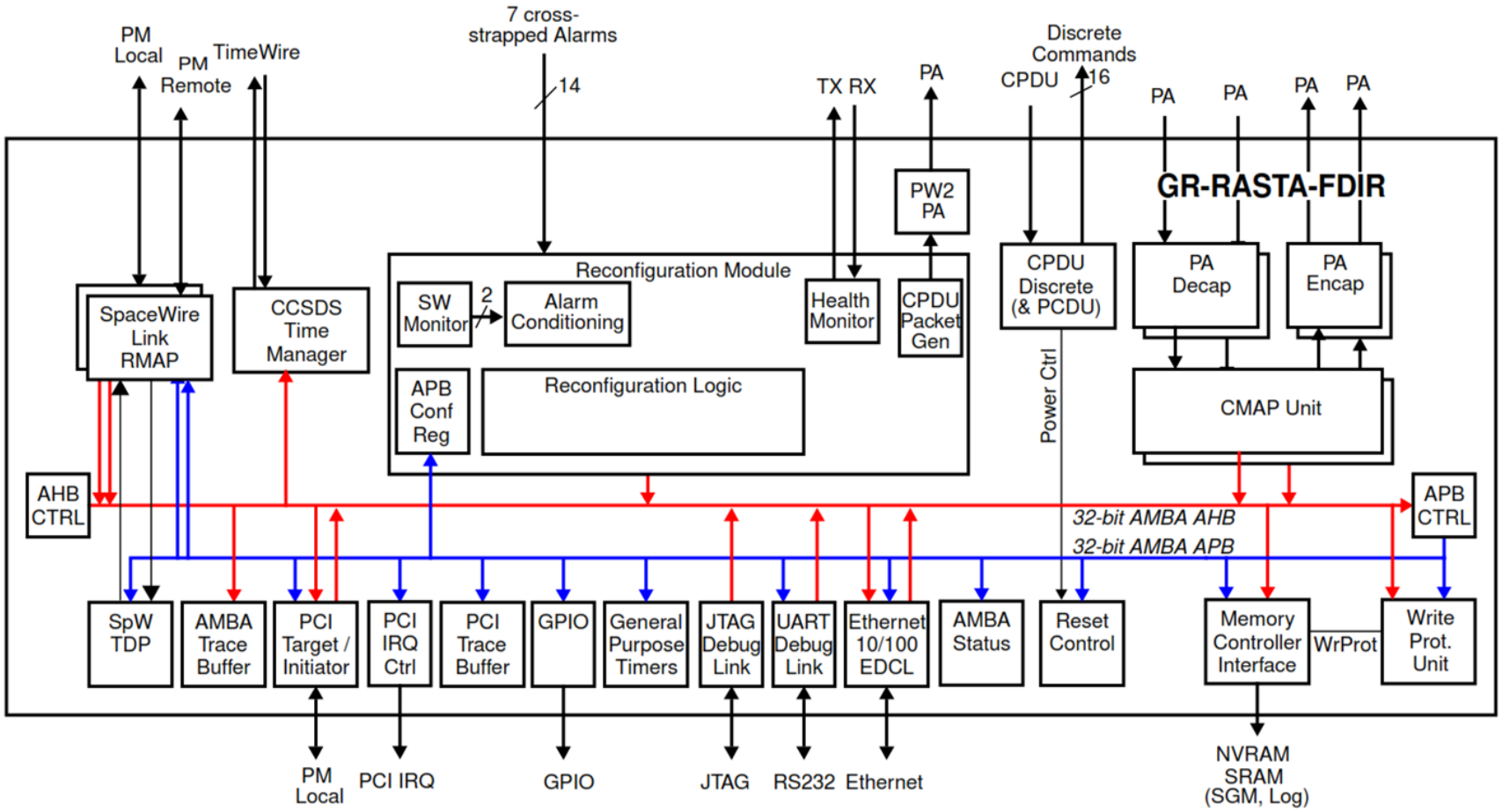
- The GR-RASTA-FDIR board is based on the GR-CPCI-XC4V:
  - Two SpaceWire interface
  - Ethernet core
  - JTAG Interface
  - Debug serial link UART
  - Compact CPCI
  - Memory
    - 128 MB SDRAM
    - 8 MB Flash PROM
  - Two GPIO interfaces:
    - 18 LVTTL input/output digital I/O
    - 2 LVDS input/output digital I/O



- Reprogrammable FPGA with programming interface
- FPGA programmed from on-board configuration memory at reset
- On-board configuration memory is reprogrammable via JTAG I/F
- In addition one GR-ACC-SPW4 accessory board provides 4 MDM9 connectors with LVDS electrical levels

Board Design

GR-RASTA-FDIR (2)



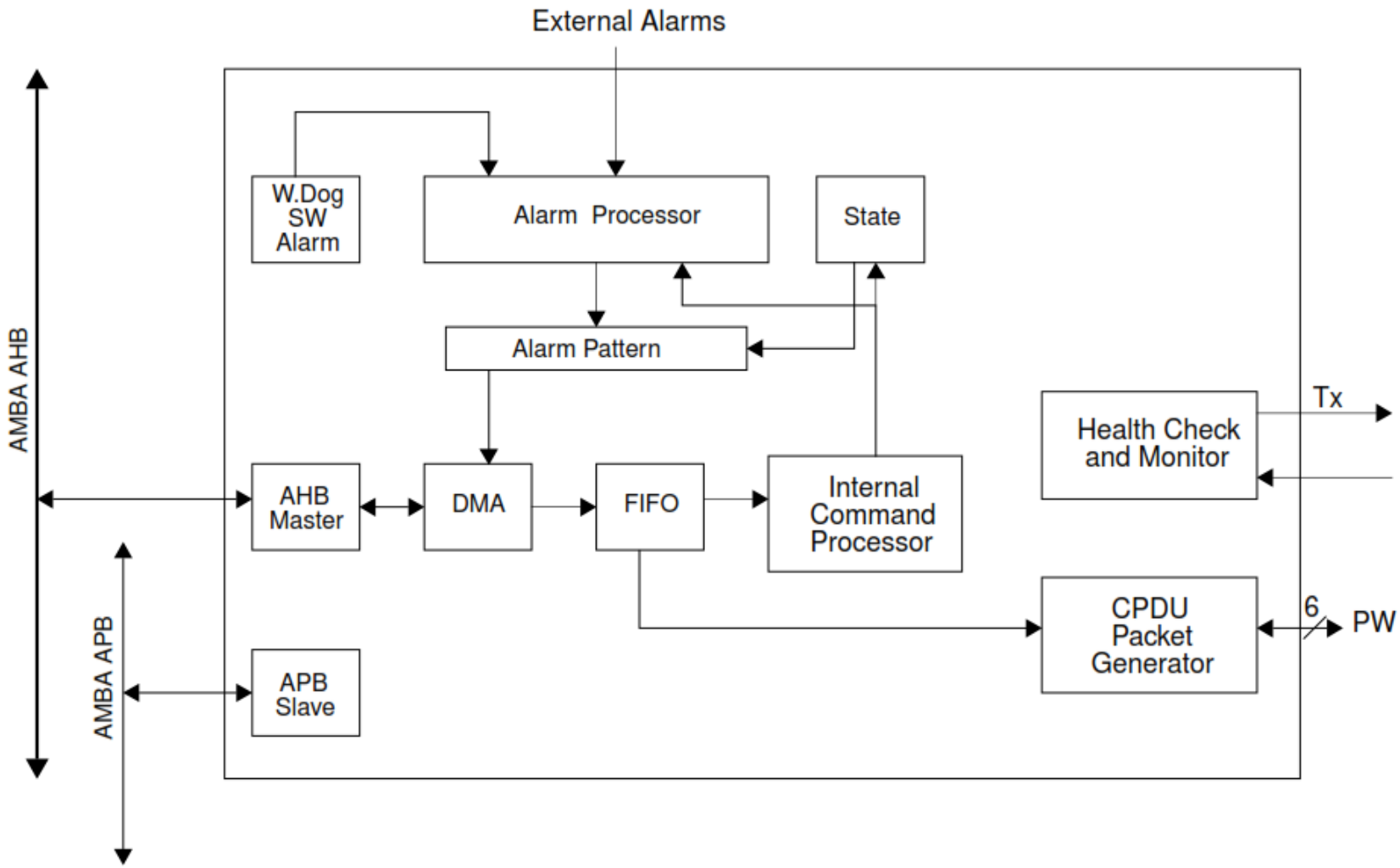
Board Design

GR-ACC-SPW4

- Consist of four SpaceWire interfaces
- Connects to the extension connectors available on the GR-TMTC-MEZZ and GR-FDIR-MEZZ
- LVDS drivers available on the accessory board

Reconfiguration Module

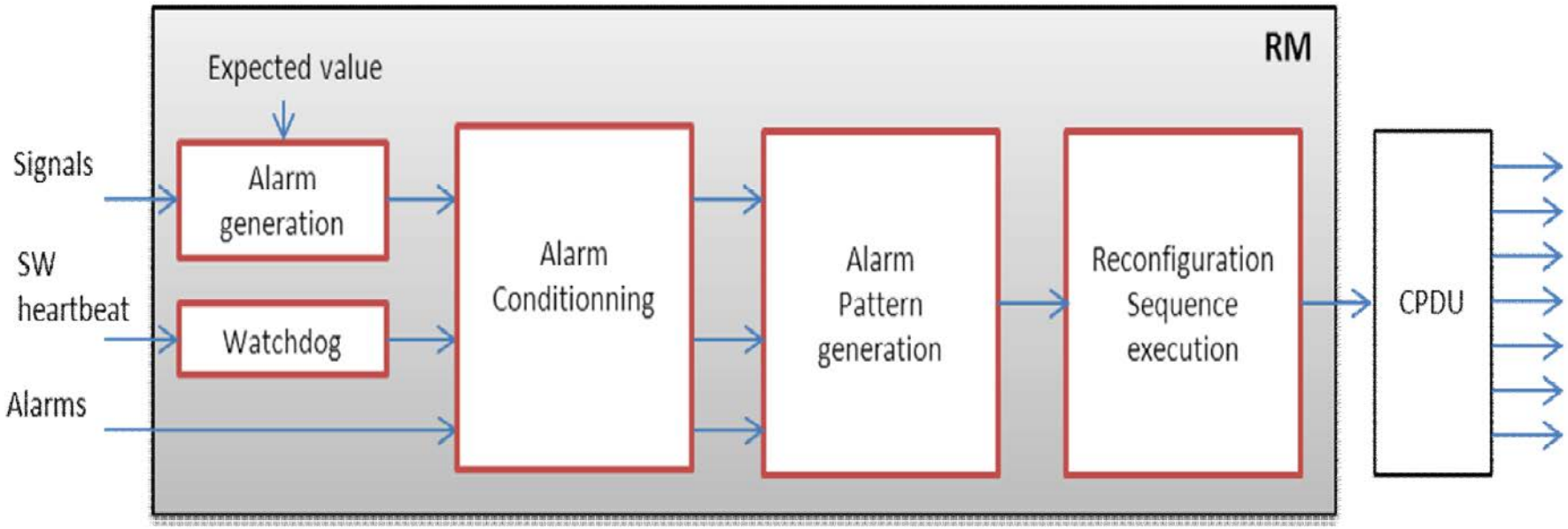
Block Diagram



Reconfiguration Module

Function

- Various options are provided for configuration of the alarm inputs such as masking, shaping and activation delay
- Based on the alarm configuration and input signals (alarm event) the RM IP core will execute user defined reconfiguration sequences (internal and external commands)



Reconfiguration Module

Reconfiguration sequences

- The internal 64 commands are split into 2 blocks each containing 32 commands
  - Clear all pending
  - Clear current pending
  - Mask all, Mask current
  - Unmask all, Unmask current
  - Rearm Watchdog
  - Delay
  - Set state
  - Check alarm
  - Do nothing
- The external commands are formed into packets and sent to the command pulse distribution unit using PacketWire interface

Reconfiguration Module

Function

- The alarm pattern provides the address from which the reconfiguration sequences should be fetched.
- The AMBA AHB bus is used for retrieving the reconfiguration sequences in memory external to the core.
- When an alarm persists after performed reconfiguration the internal state-machine can be utilised to execute alternative reconfiguration sequences that depend on previously executed reconfigurations
- The alarms are logged with the time instance at which the alarm is triggered.

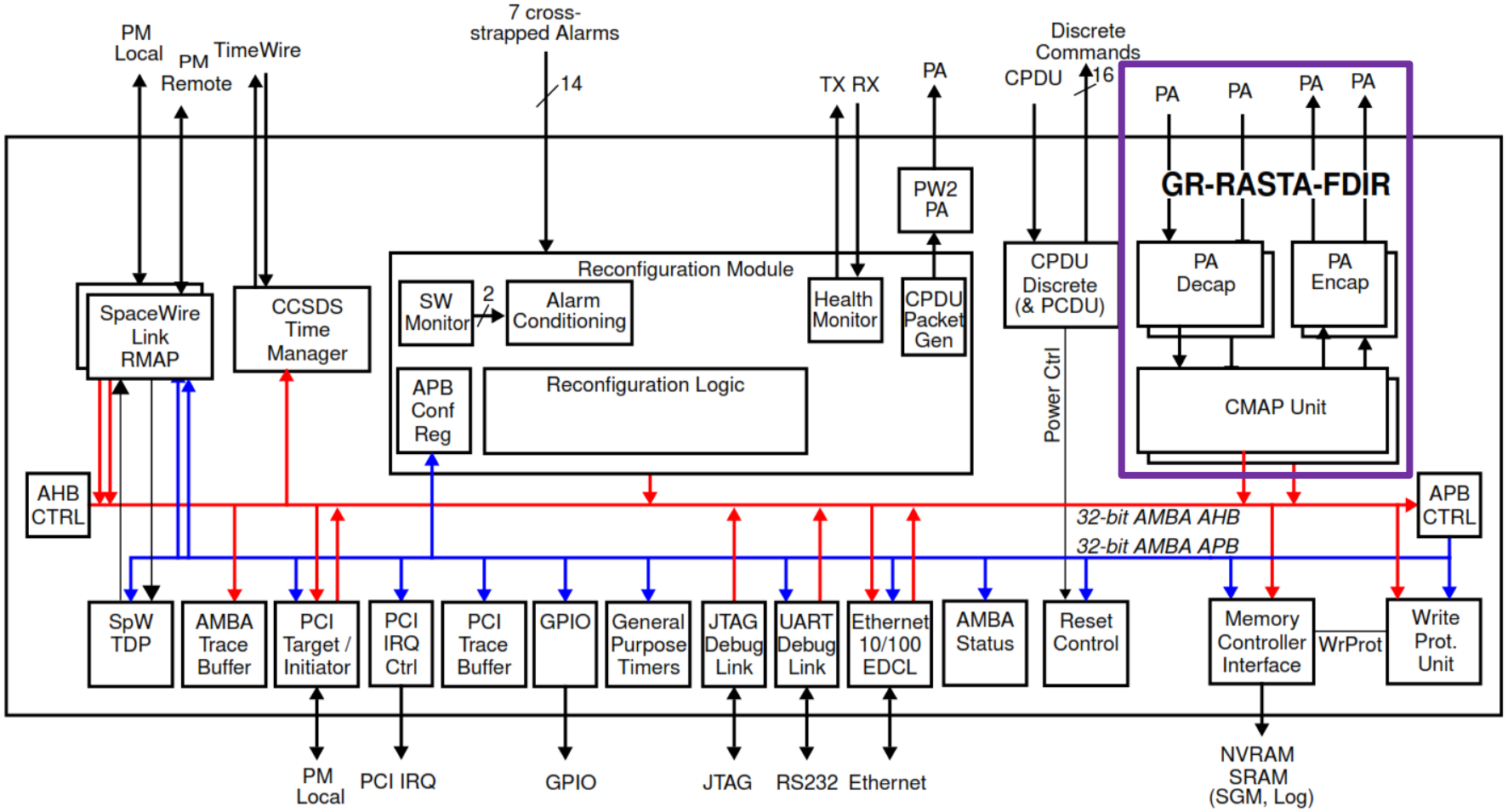
Reconfiguration Module

Features

- Features
  - External, Watchdog and Software alarms
  - Alarm monitoring unit
  - Alarm log (with time instance)
  - Dedicated health link
  - AMBA APB bus for configuration, control and status handling
  - Reconfiguration sequences (internal and external commands)
  - CPDU Packet Generator
  - Configurable reconfiguration sequences

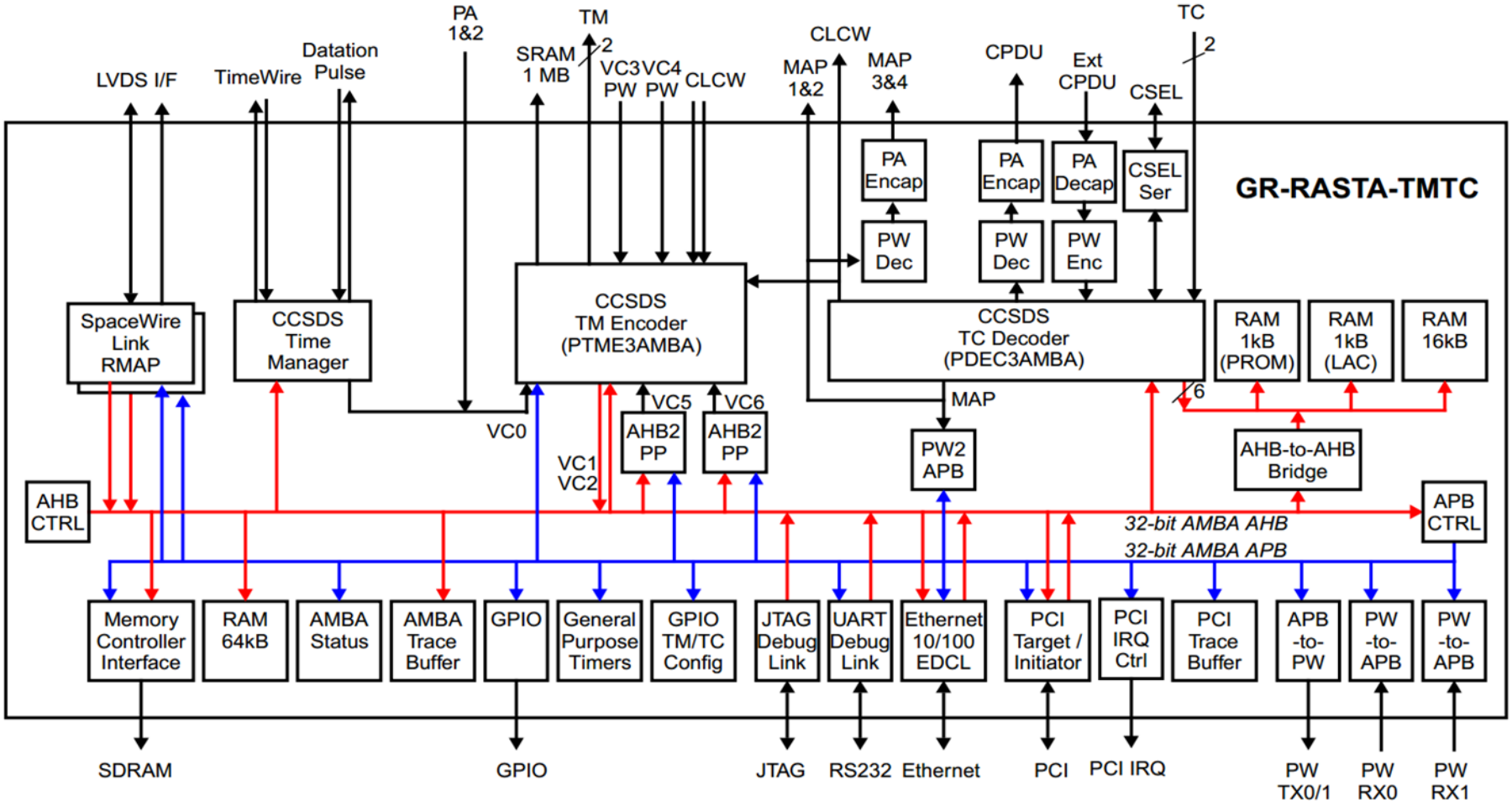
Communication between FDIR and TMTC unit

FDIR unit



Communication between FDIR and TMTC unit

TMTC unit



Communication between FDIR and TMTC unit

CCSDS Memory Access Protocol Unit (CMAP)

- CCSDS packet interface for performing AMBA bus accesses.
  - Packets conform to the Packet Utilization Standard (PUS)
  - Register load commands
  - Load and Dump Memory commands
- Hardware IP-core
  - Requires no software involvement
  - RM and spacecraft recovery
- Interfaces directly with a TC MAP and a TM VC
  - Asynchronous bit serial link (PacketAsynchronous) used for data transfers

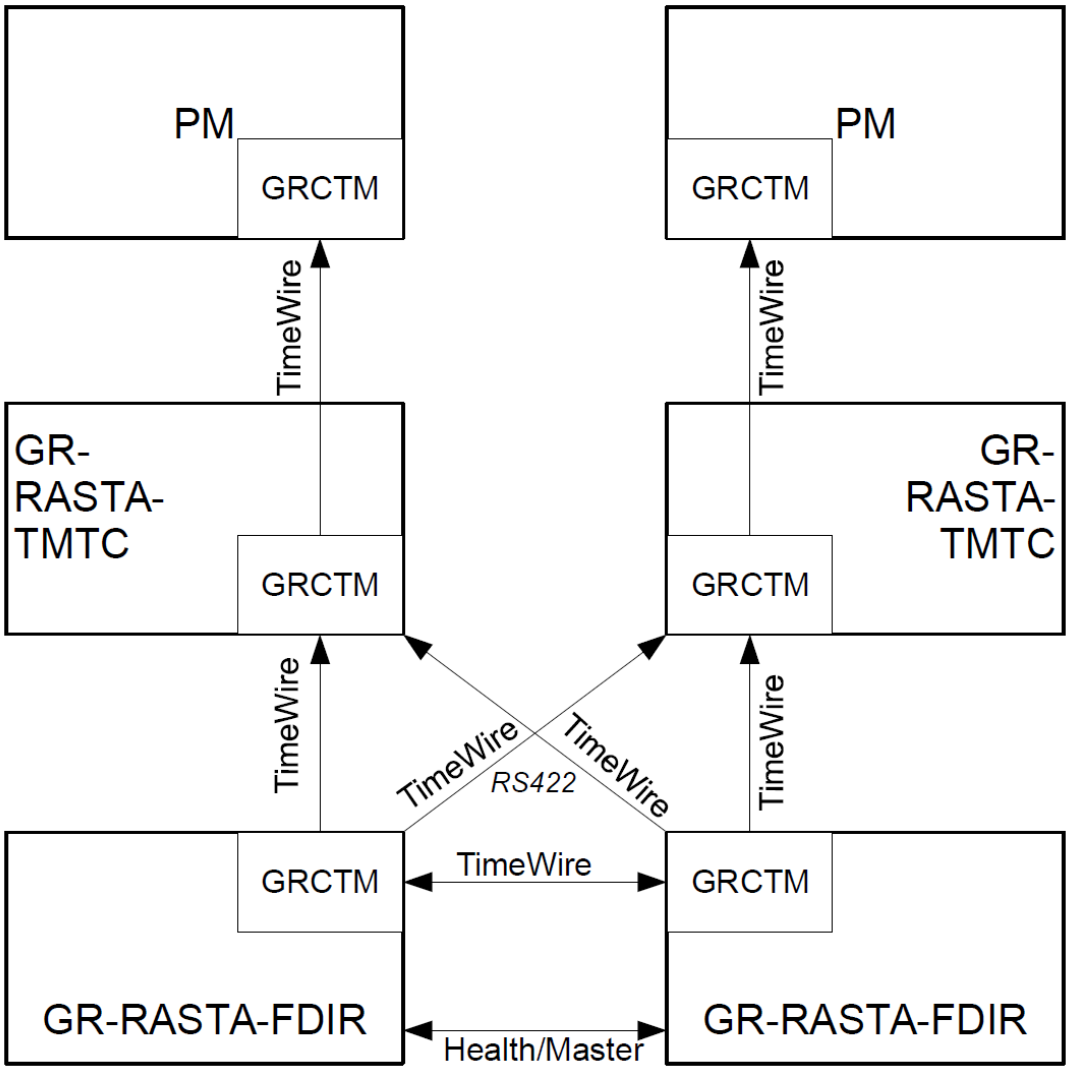
Communication between FDIR and TMTC unit

CMAP unit event report service

- Automated TM packet generation
- Generation may be triggered by external events:
  - RM Error
  - RM Reconfiguration
  - Bus Error Interrupt (EDAC Errors)
  - Timer Units (for periodic status)
- Report Data for each trigger is fetched through AMBA Bus
- Available trigger Configuration options:
  - Severity Level
  - Transfer start address
  - Data length

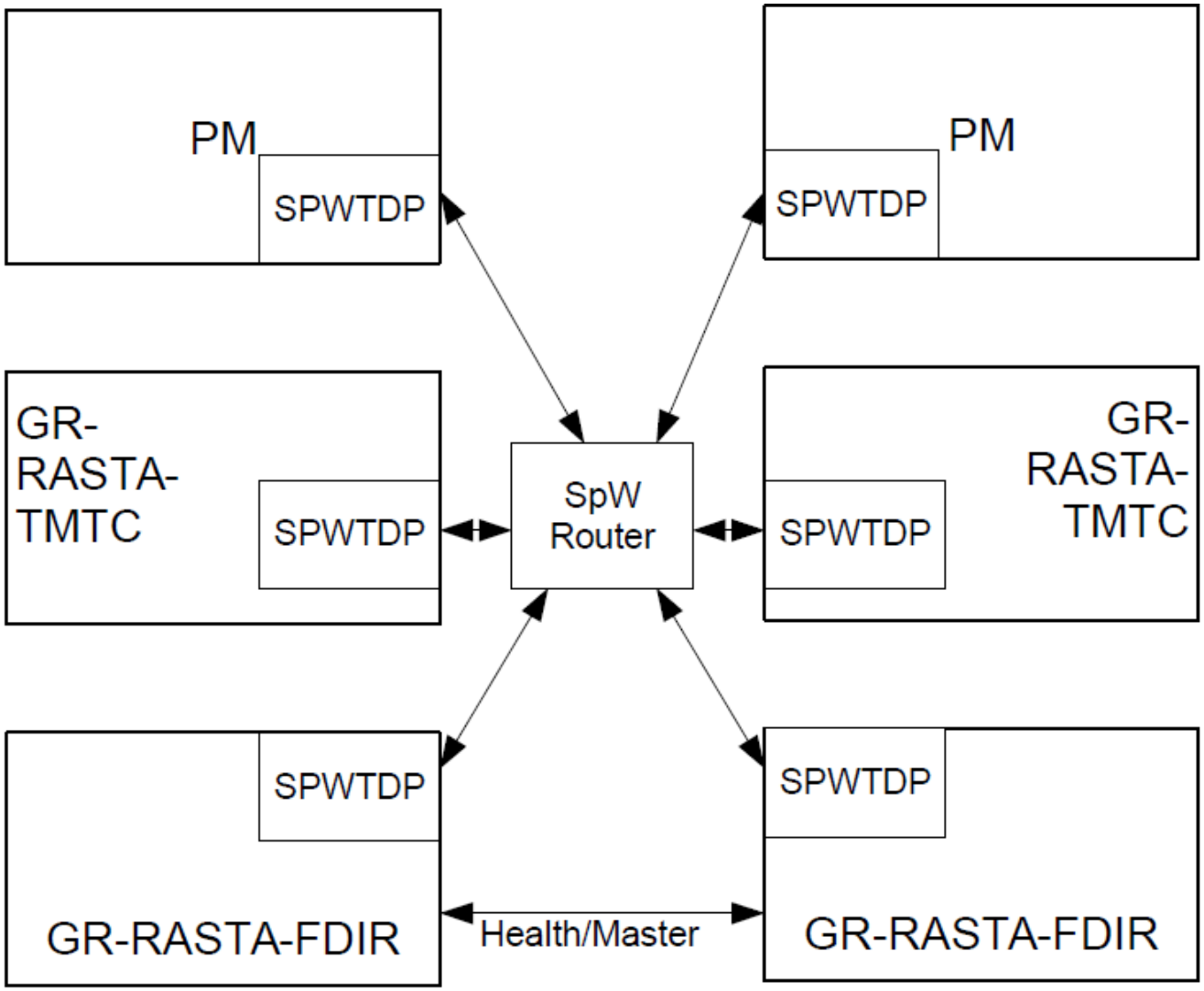
Time Distribution

Using GRCTM



Time Distribution

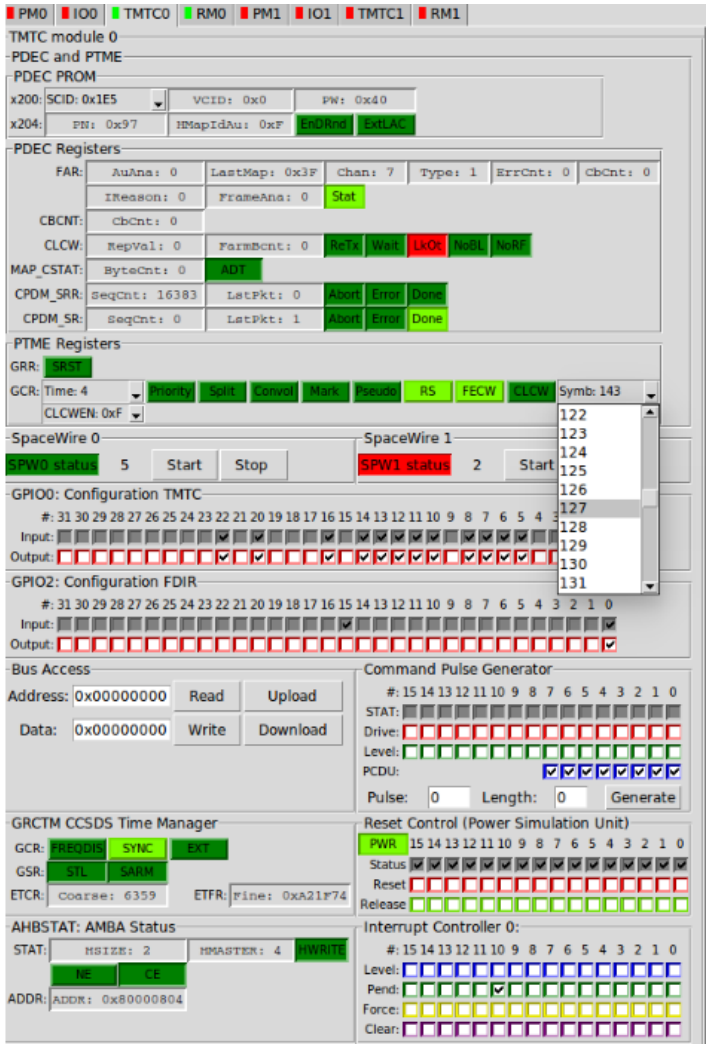
Using SpaceWire



Test-bed Controller Tool

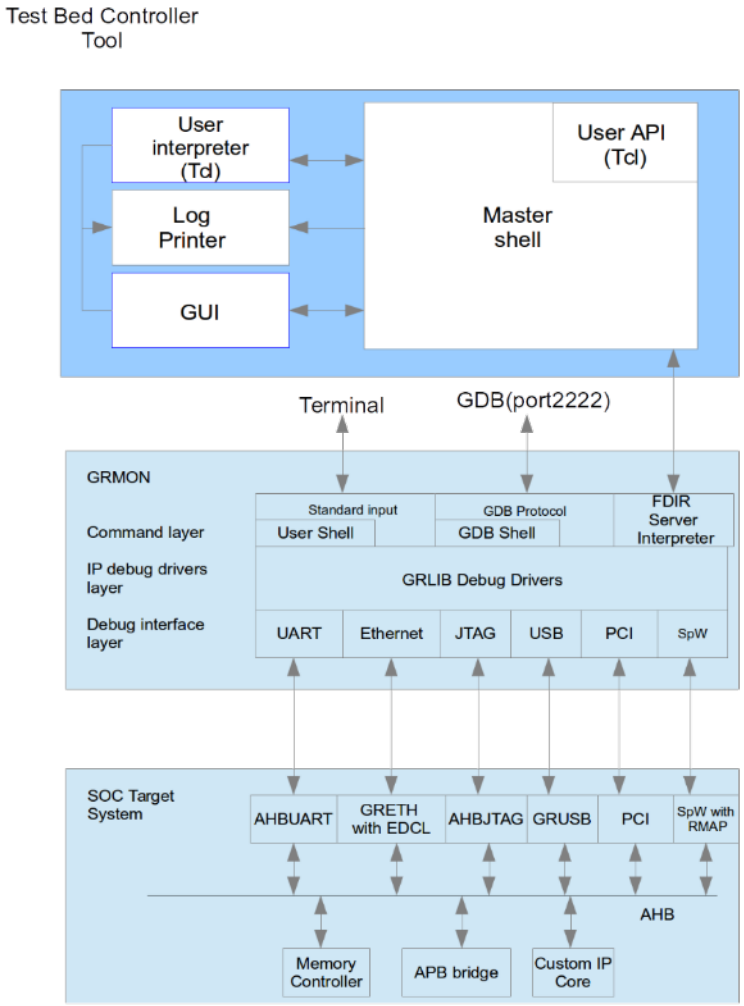
Overview

- 8 GRMON instances to connect all the RASTA units
- Continuous monitoring and presentation of register values on GUI
- Up to 20 hz pollrate
- Essential control of key IP-cores
- Load Programs to PM memory and execute/break
- Reset of individual IP cores
- Power management of RASTA units
- Inject error cases in the dual redundant system
- Work ongoing



Test-bed Controller Tool

Interaction with GRMON



Test-bed Controller Tool

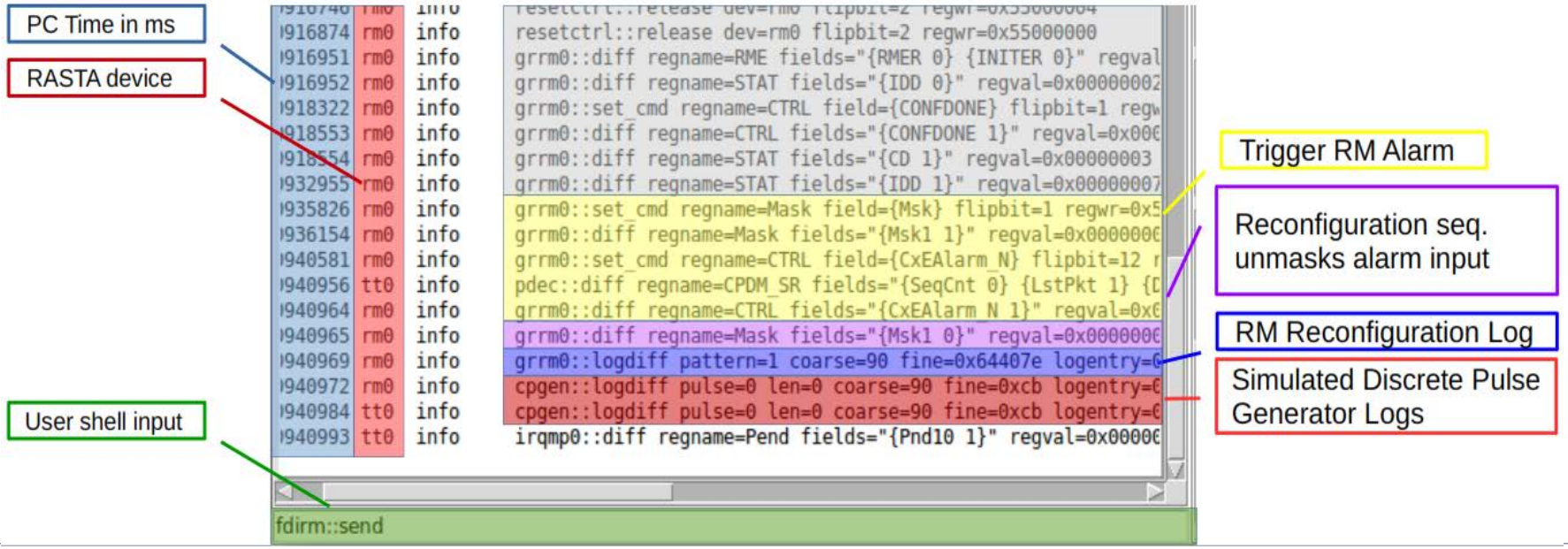
Example 1 : Control and Monitor of RASTA-FDIR

Test-bed Controller Tool

Other features

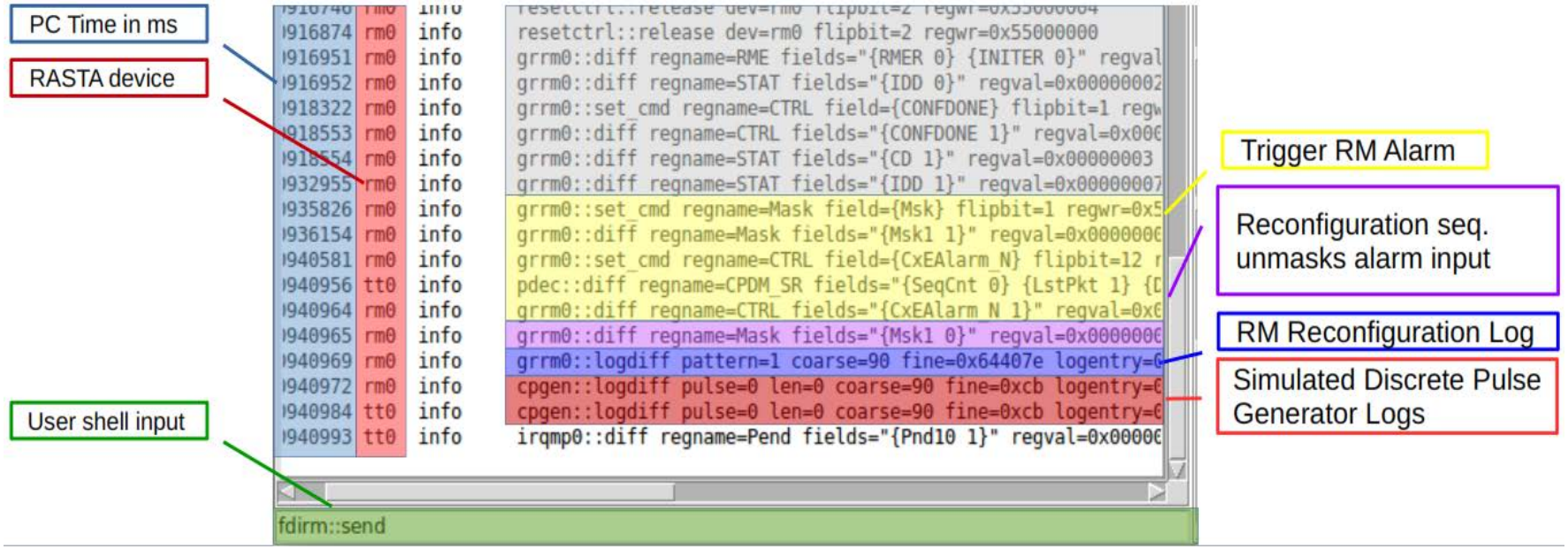
- TCL Scripting Language
  - Used for developing tool
  - Powerful user scripts
- Logs
  - User generated commands
  - Register changes

- Store value from 0x40000000 into set
  - set val [::fdirm::send pm0 {mem 0x40000000 4}]
- Write value of set to 0x40000008
  - ::fdirm::send pm0 "wmem 0x40000008 $val"



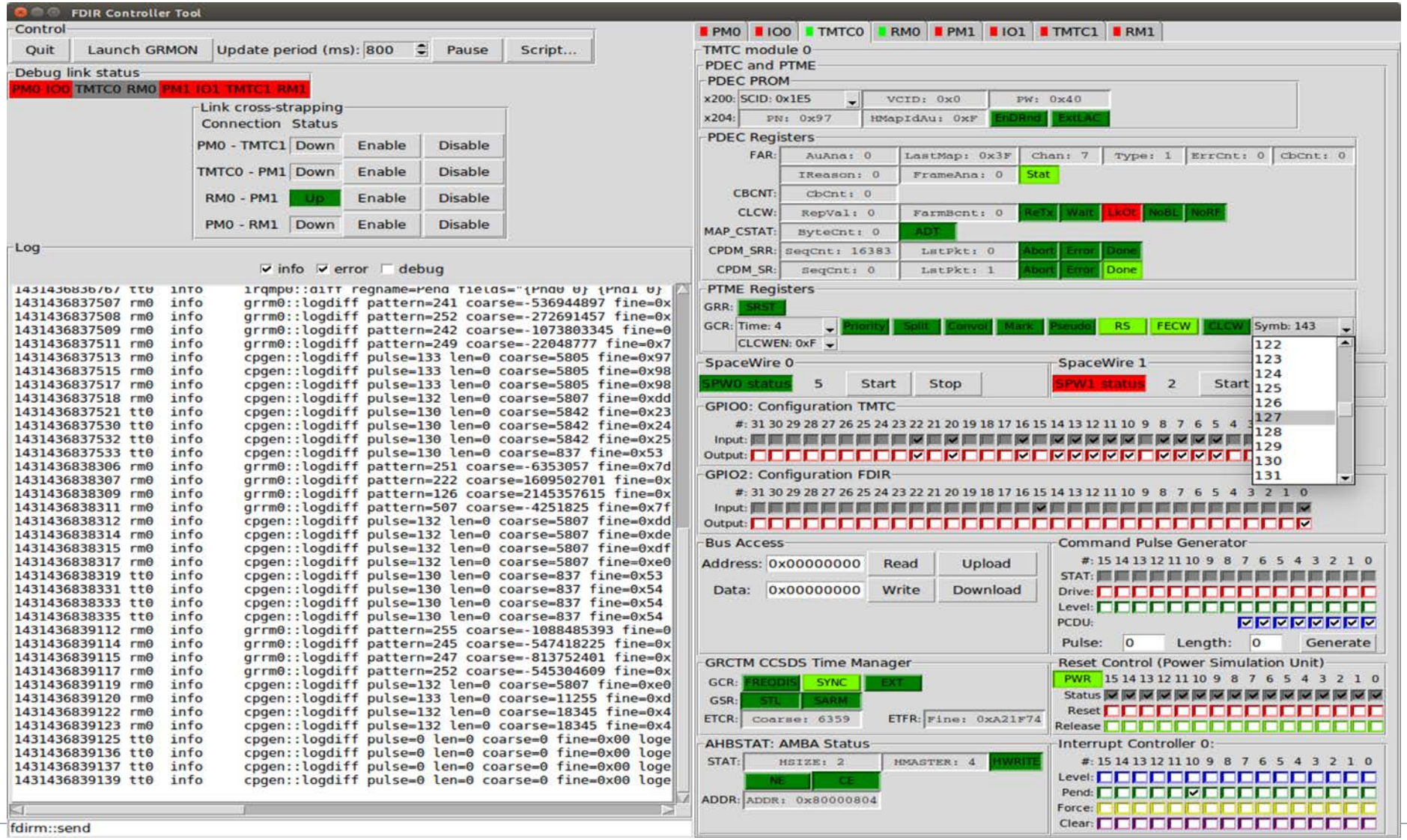
Performance Evaluation

- Controller tool log the events, the time originates from the timer on the PC running the tool
- Additionally time units (CUC Time Manager) in all modules
- Dedicated time tag units for alarm events and command generation
  - To accurately measure time difference between alarm events and command generation



Test-bed Controller Tool

Example 2 : Control and Monitor of RASTA-TMTC



Test Application Software

- RTEMS 4.10
- Several examples available (SpW, CAN, 1553, ...)
- New FDIR test applications are developed
- RTEMS drivers required for Reconfiguration Module and GR-RASTA-FDIR (PCI target driver) available
- Validation of the Test-bed

Features

Overall activity features

- Evaluation platform for a dual redundant system
- Allow upgrade and evolution of architecture
- A user interface able to access the system resources and easy to use
- Ability to perform recording of simulation events and results
- Ability to measure the switching time between system re-configurations
- Ability to inject errors and to simulate failure mode
- Ability to time stamp events
- Configurable cross strap
- Generate on board time and provide the time synchronization and distribution function
- Example application software

Summary

- In this activity, a dual redundant architecture based on the current single chain RASTA architecture is developed.

- An RM IP core is developed together with a new RASTA-FDIR hardware module that will complement the existing RASTA hardware by providing the necessary functionality to support dual redundant architecture.

- Testbed controller tool will be developed which will enable the users to load, run and analyse applications and simulations, as well as inject error cases in the dual redundant system.

Thank you for listening!

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