

Workshop on Memristive systems for Space applications
30 April 2015
ESTEC, Noordwijk, NL

Resistive Memories (RRAM) - principles & technology

Dirk J. Wouters

RWTH Aachen, Institut für Werkstoffe der Elektrotechnik, Aachen, Germany

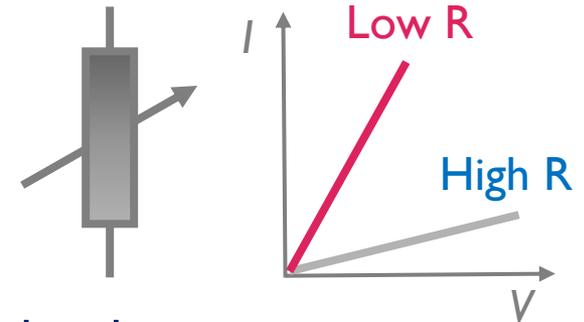
30 April 2015

Outline

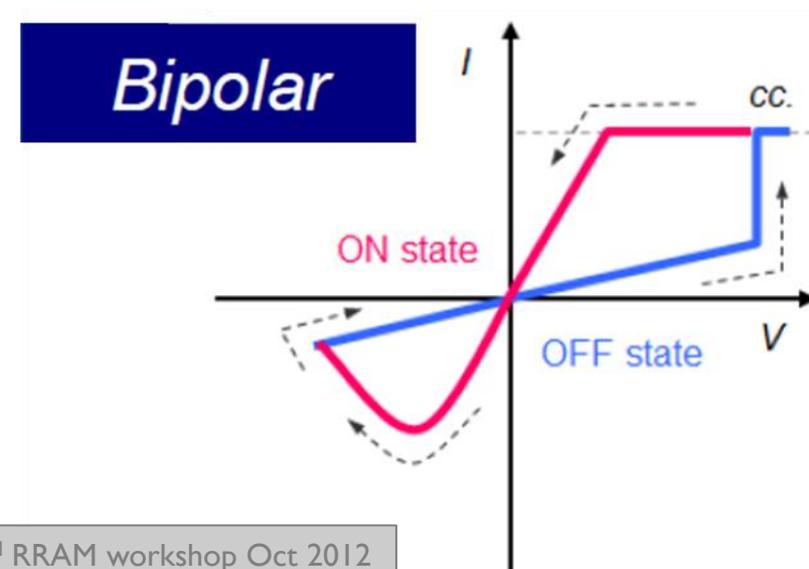
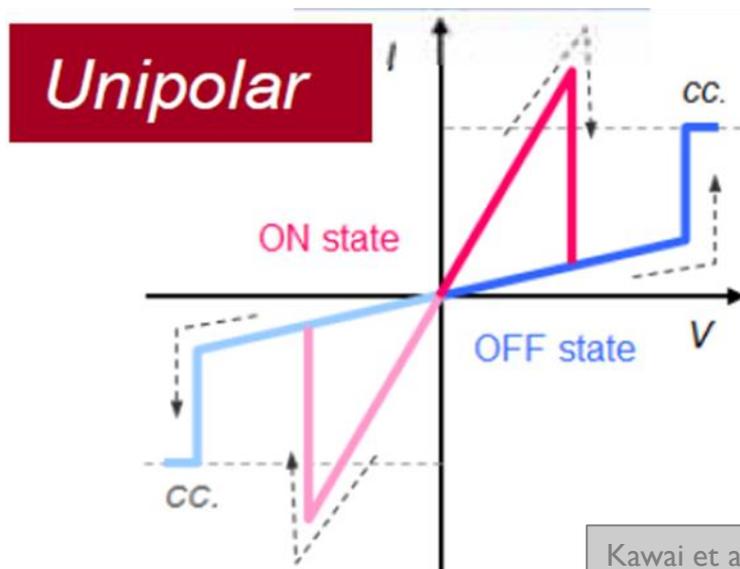
1. Definition and classification
2. Filamentary switching
 - Oxygen vacancy based (VCM)
 - Metal cation based (ECM)
3. Interfacial switching devices
4. RRAM array organization
5. Status and outlook

Resistive Switching Memories

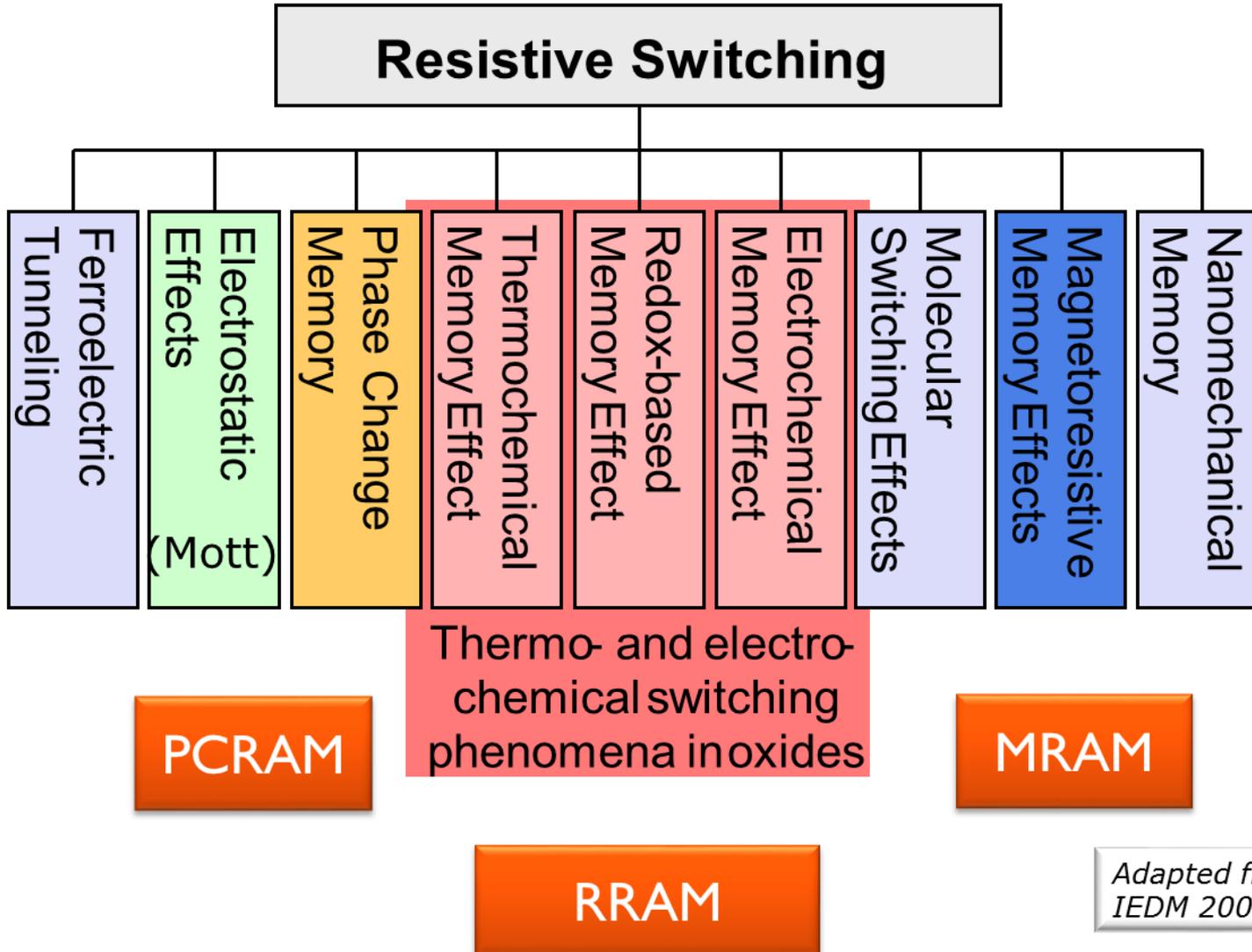
- Memory element is R (MIM-type 2-terminal)
 - r can be altered by applying V/I on R
 - readout R at low voltage



- Bipolar or Unipolar Switching depending on mechanism



Taxonomy of Resistive Switching Memories : based on Mechanism



Adapted from R. Waser,
IEDM 2008

Resistance Modulation Geometry

1D Filamentary

2D Interfacial

3D Bulk Transition

Thermo-
Chemical
Fuse/
antifuse

Oxygen
vacancy
migration

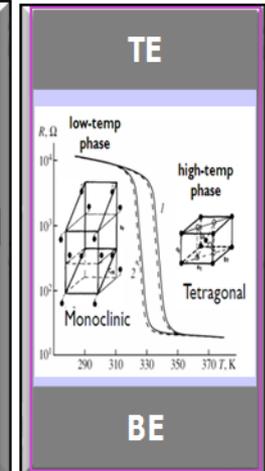
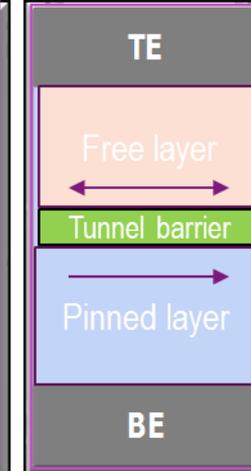
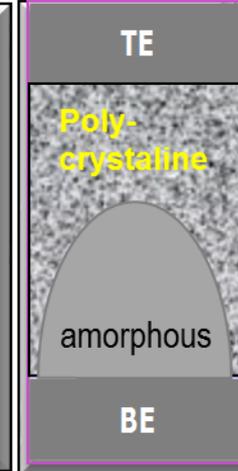
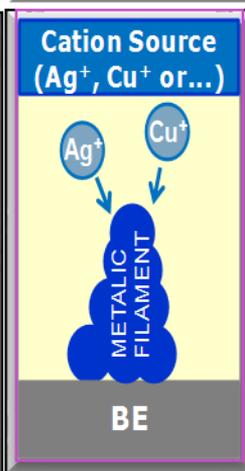
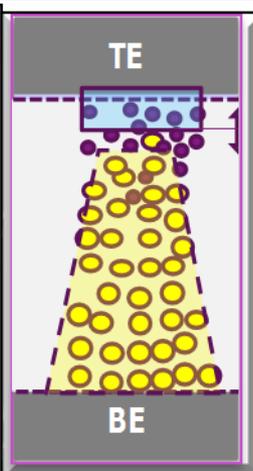
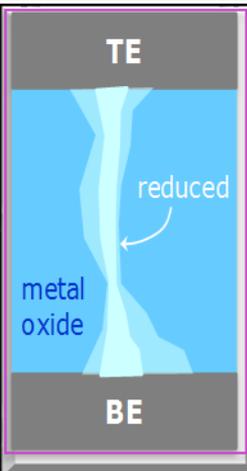
Electro-
chemical

Schottky
barrier

Phase
change

Tunnel
Magneto
resistance

Electronic
MIT
(Mott)



UNIPOLAR

BIPOLAR

BIPOLAR

BIPOLAR

UNIPOLAR

BIPOLAR

UNIPOLAR

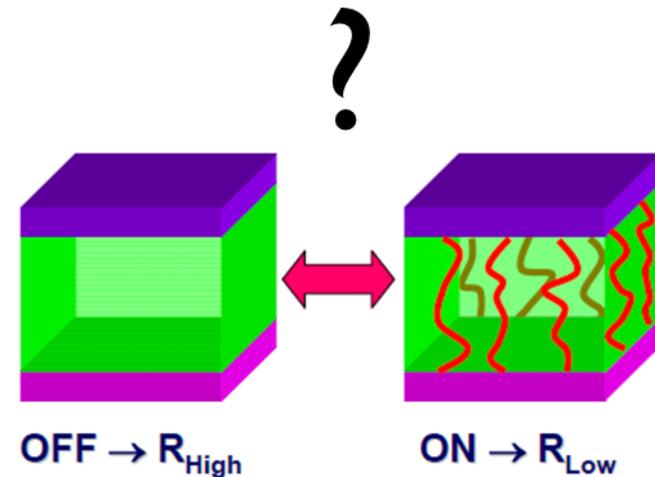
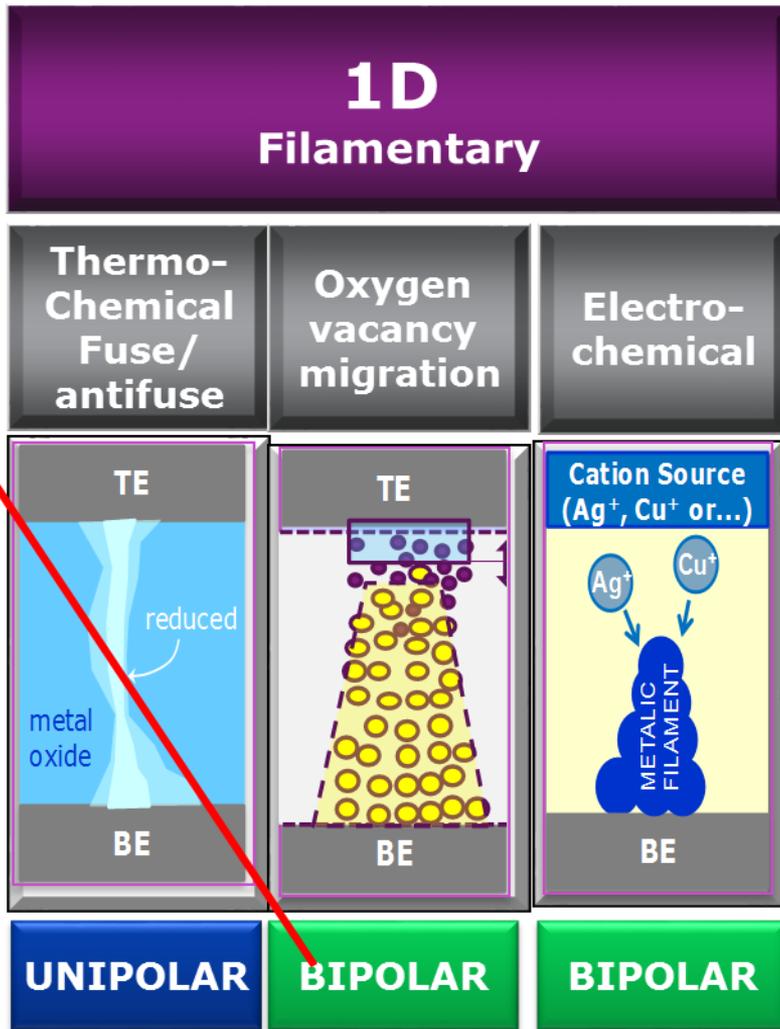
RRAM

PCRAM

MRAM

?

1D Filamentary switching

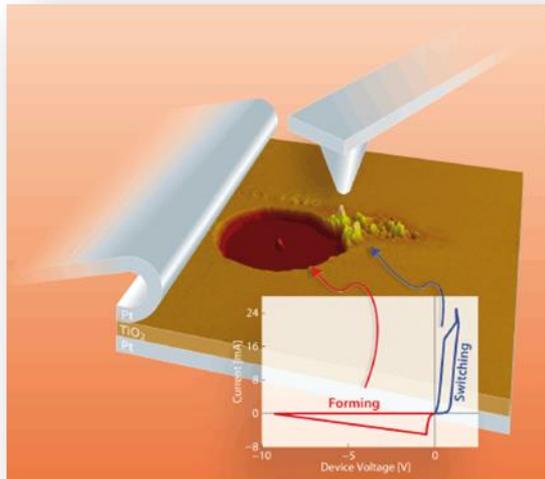


Unipolar :

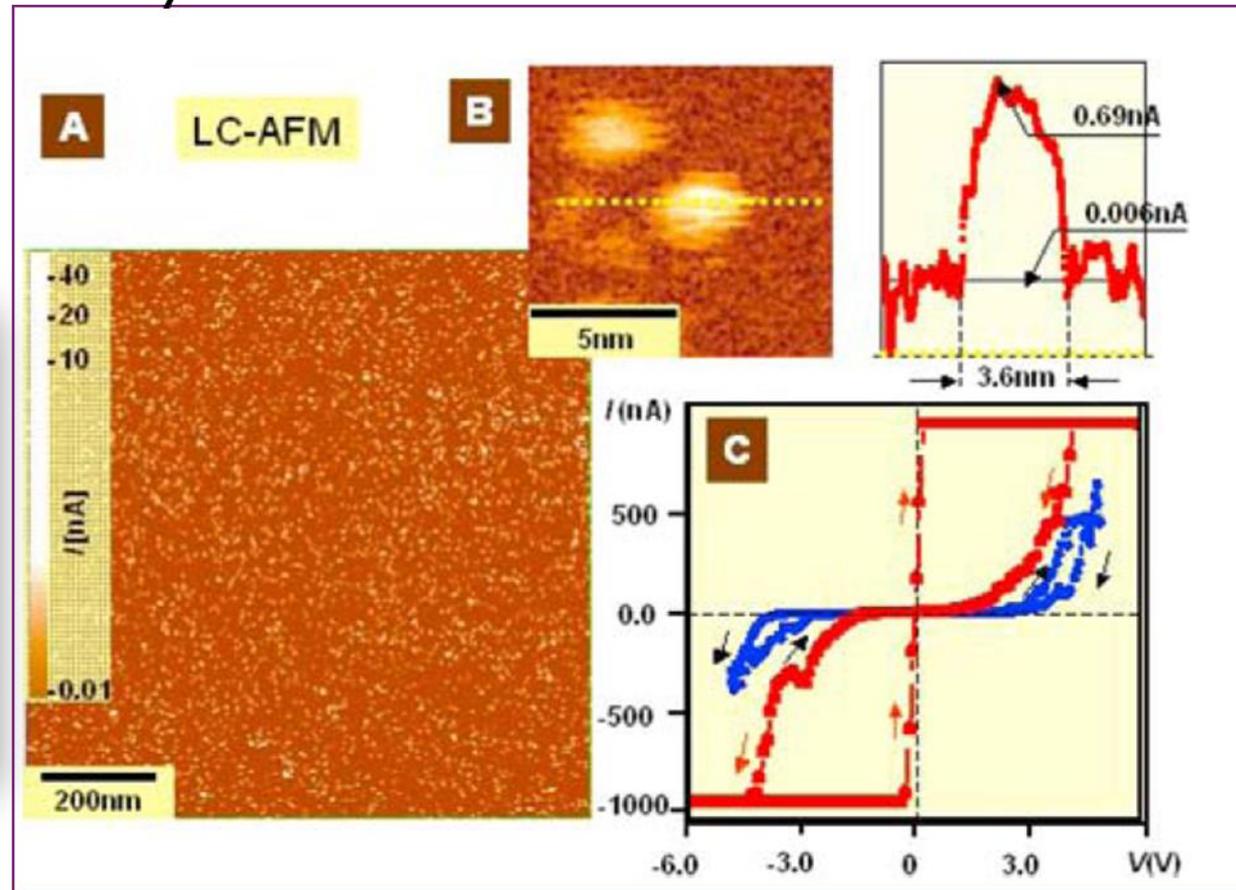
- Higher power
- Less cyclability

Indications for filamentary switching

From *physico-chemical analysis*



R. Münstermann et al.,
PSS RRL4 (2010) 16-18

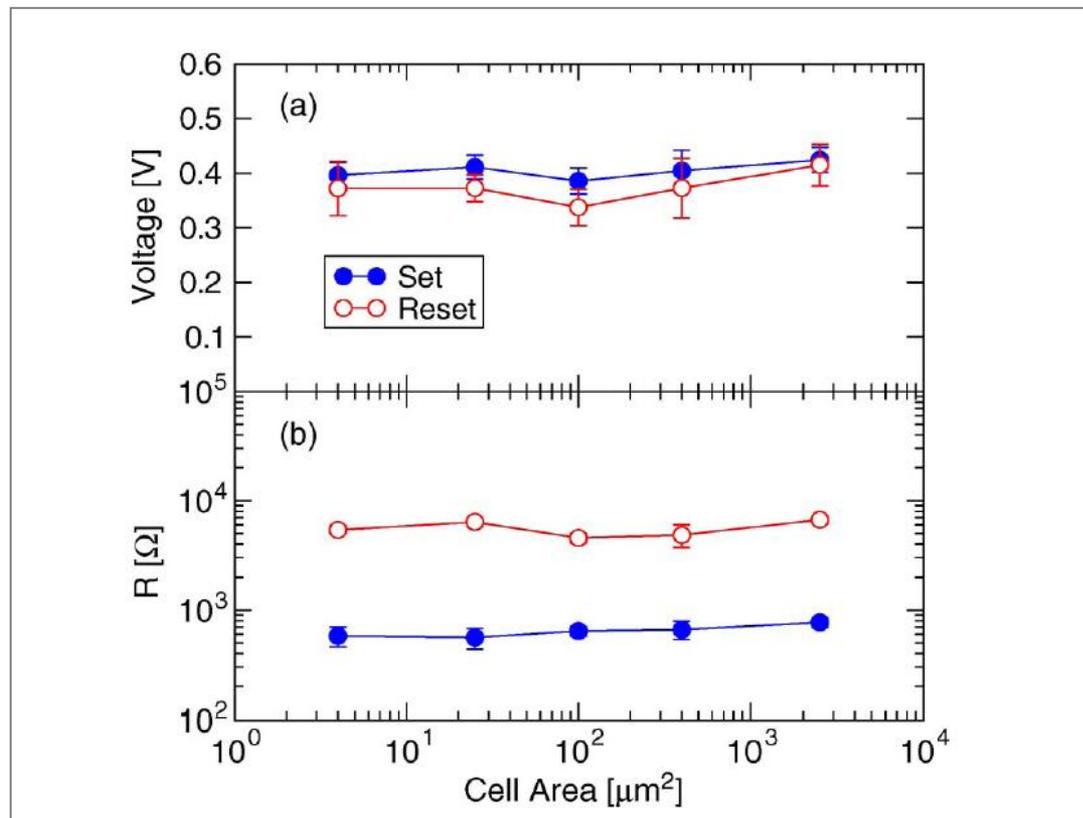


K. Szot, Phys. stat. sol. (RRL) 1, No. 2, R86–R88 (2007) / DOI 10.1002

Indications for filamentary switching

Electrical fingerprint from device characteristics

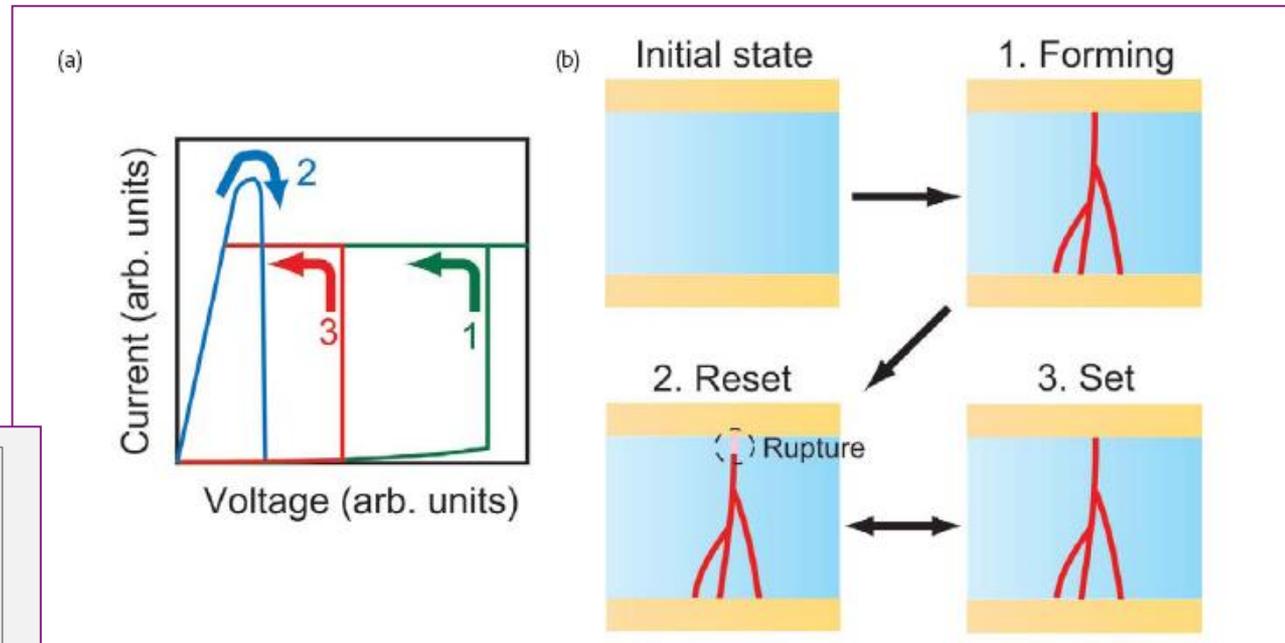
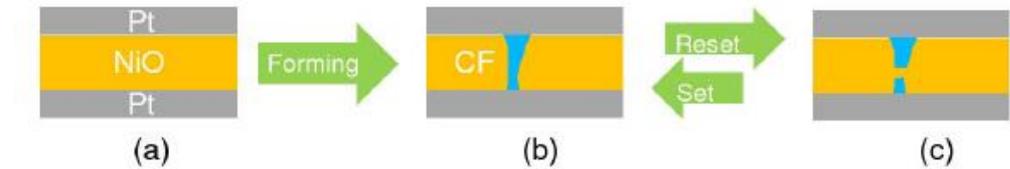
- Area (in)dependence of LRS/HRS and switching voltages



Different steps in a filamentary switching process

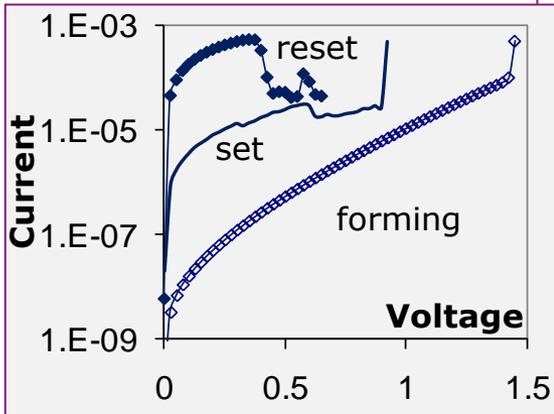
C.Cagli, IEDM 2008

- ▶ Forming
- ▶ RESET
- ▶ SET



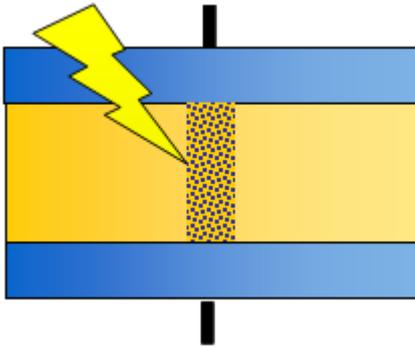
Akihito Sawa, materialstoday, Vol 11(6), 2008

real switching curves

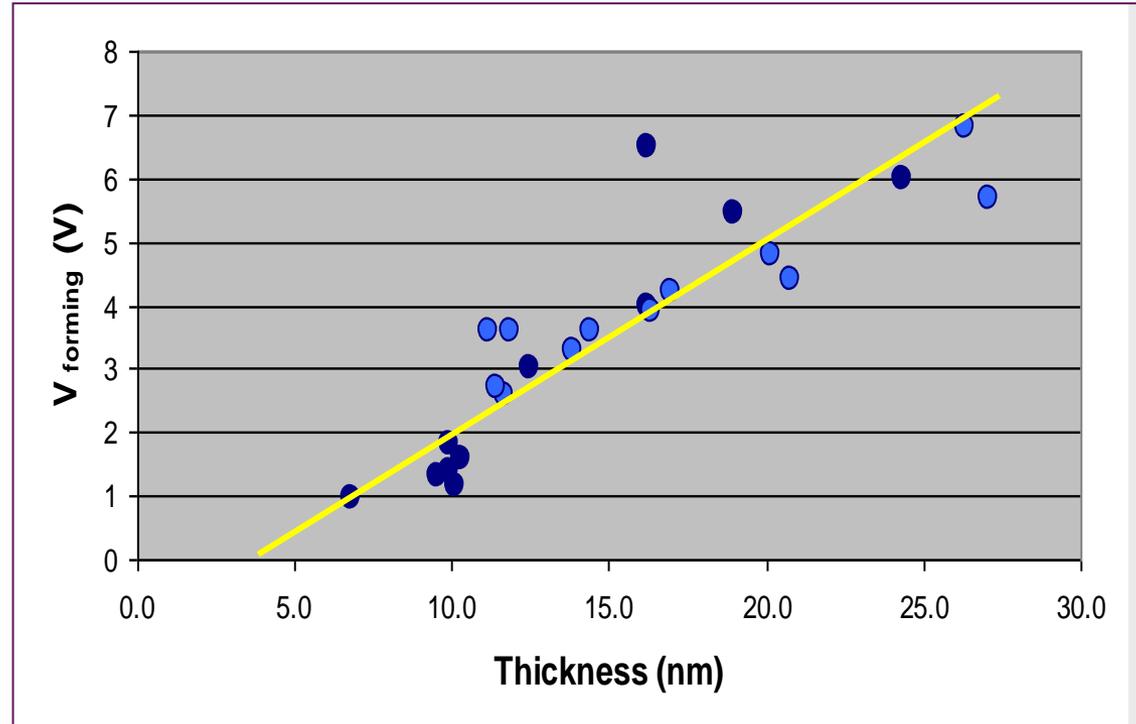


L.Goux (imec), NiO/Ni RRAM cell

Forming: creating a conduction path by “breakdown”



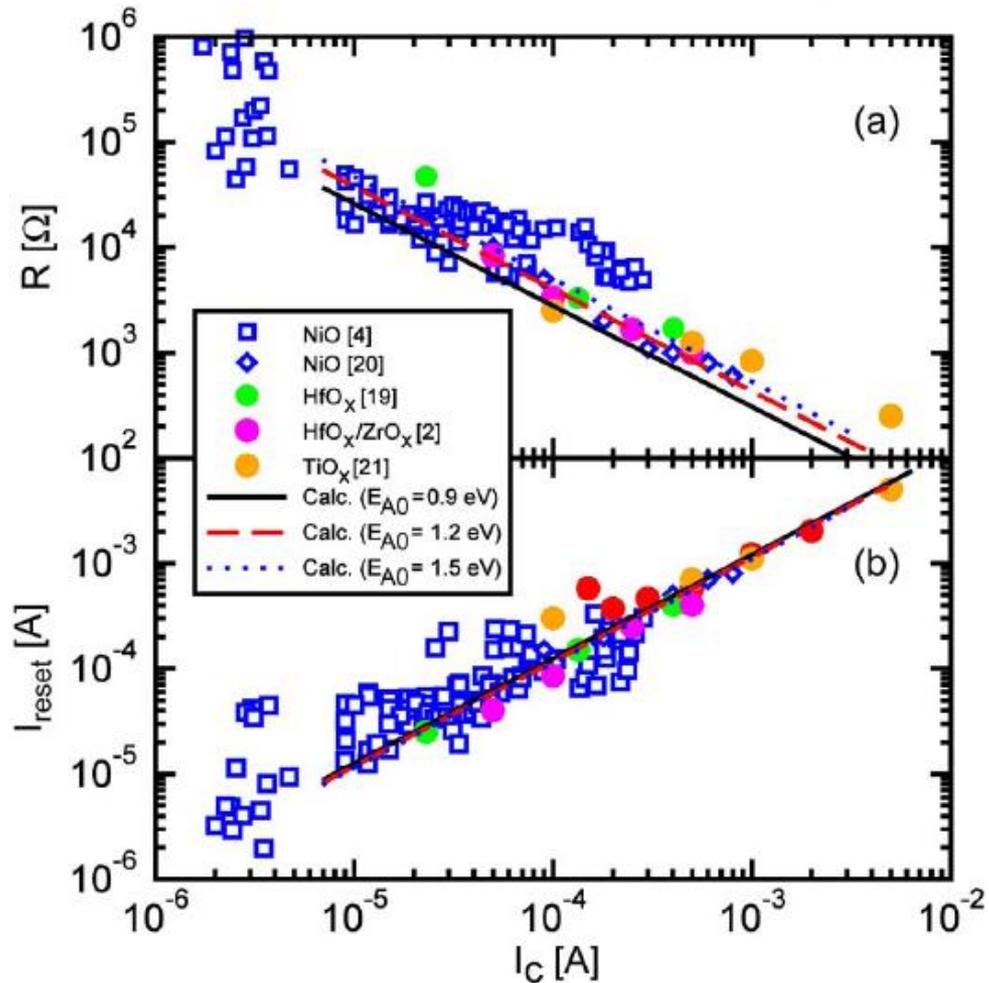
Forming
voltage scales
with thickness



NiO by MOCVD imec

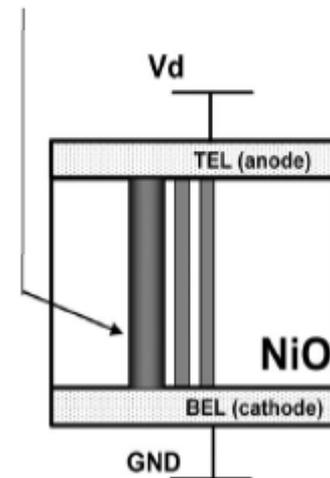
Similar to (soft) breakdown in dielectrics (defect & percolation path generation)

Maximum current during Forming(/SET) controls filament "Strength"



D.Ielmini et al, Trans.El.Dev. 58(12), p.4309, 2011

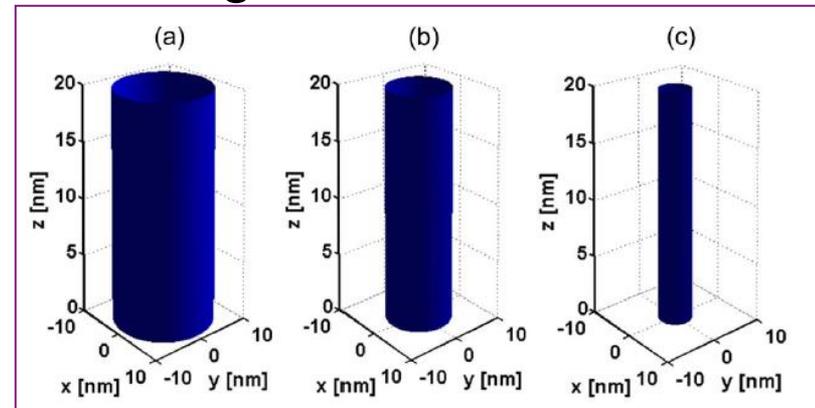
Filament size determined by SET current compliance



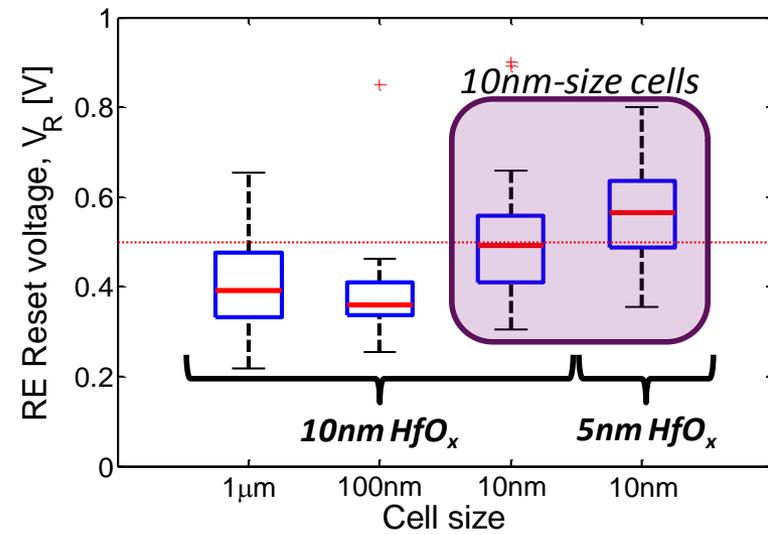
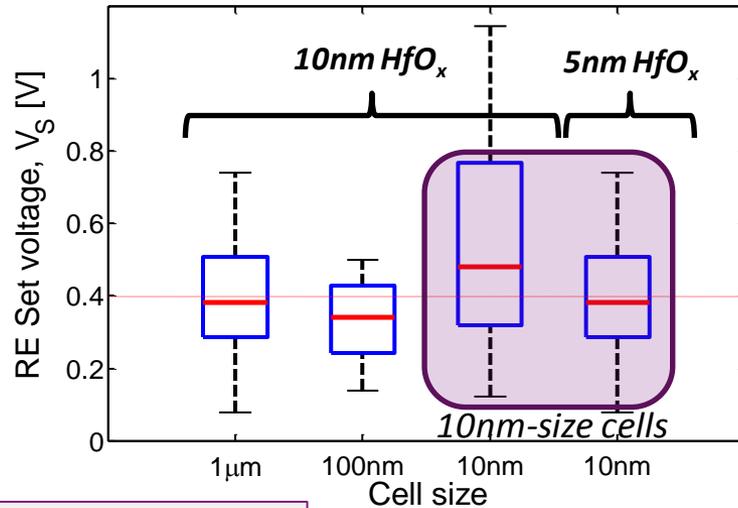
Y.Sato et al, Trans.El.Dev. 2008

“Scaling of filamentary switching”

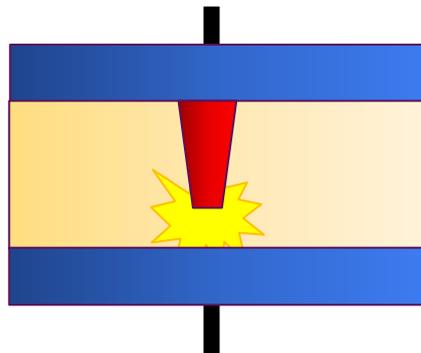
- ▶ 2D and 3D switching:
 - Current levels scale with area of the cell $\sim F^2$
- ▶ 1D switching:
 - Current levels **independent of cell area**
 - Current level determined by filament “diameter”
 - **Determined by operation conditions** (Forming/SET CC)
 - We can have small current even in large device
 - Limitations ?
 - Cell area \sim filament size..
 - Smallest filament size ?
 - \sim nm ??



Switching during SET/RESET: SET \neq Forming



B.Govoreanu, IEDM2011

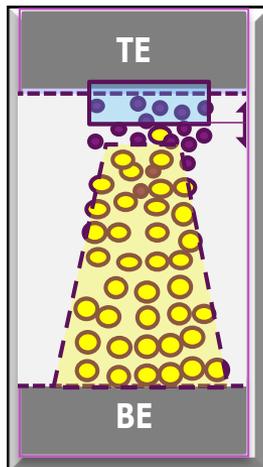


Absence of oxide thickness effect on $V_{\text{SET/RESET}}$ indicative of LOCAL filament switching

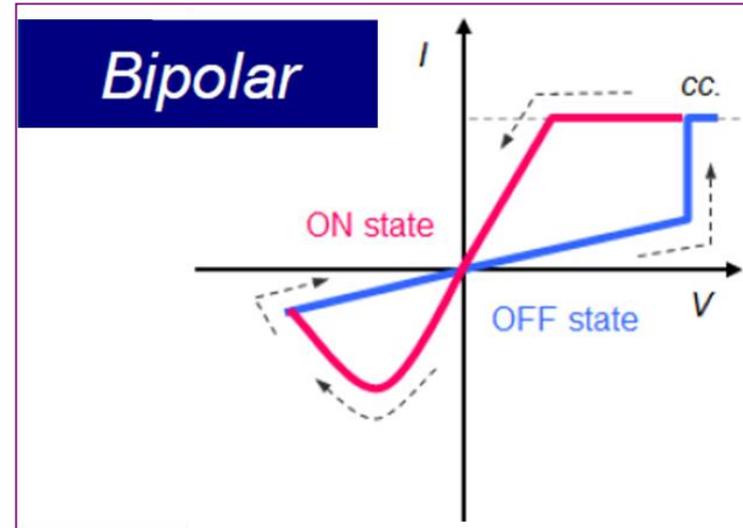
Bipolar Switching OxRRAM : “Oxygen Vacancy Migration”

1D
Filamentary

Oxygen
vacancy
migration

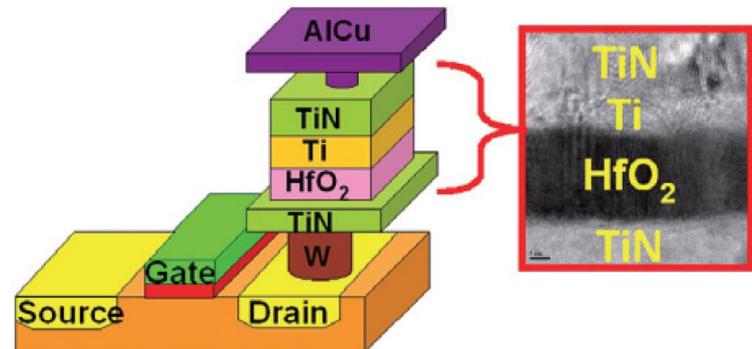


BIPOLAR



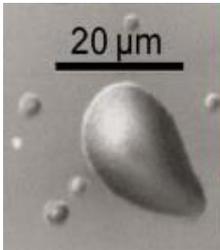
Material : TMO's , e.g. HfO, TiO, TaO..

H.Y.Lee et al, “Low Power and High Speed Bipolar Switching with A Thin Reactive Ti Buffer Layer in Robust HfO₂ Based RRAM”, IEDM, Tech. Dig., pp. 297, 2008



Role of oxygen / oxygen vacancy defects in OxRRAM memories

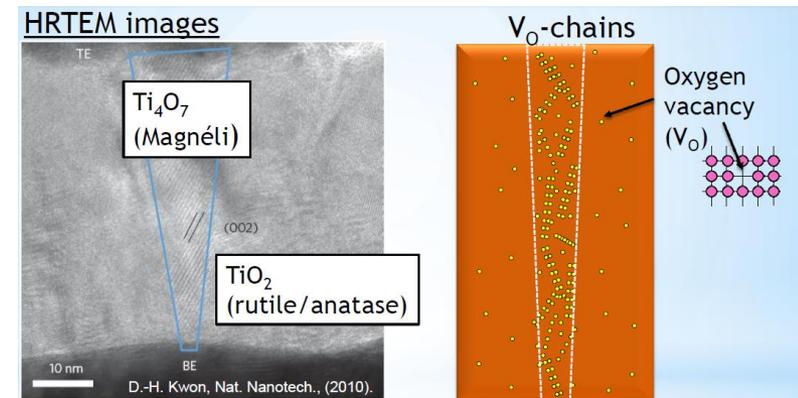
- ▶ Filament switching involves oxygen transport



Bubbles < O₂ released to the gas phase or adsorbed by the grainboundaries of the Pt electrode

Szot et al., Nature materials (2006)

- ▶ Filament observations indicate local lower O concent
 - Magnelli phase of Ti₄O₇ or Ti₅O₉ , essentially TiO_{2-x}
 - Oxygen vacancy defects

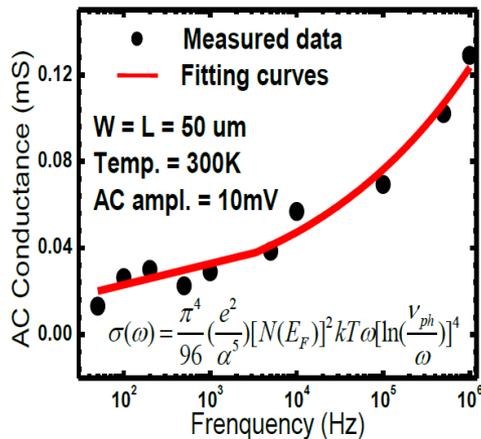


D. H. Kwon et al., Nature Nano technology(2010)

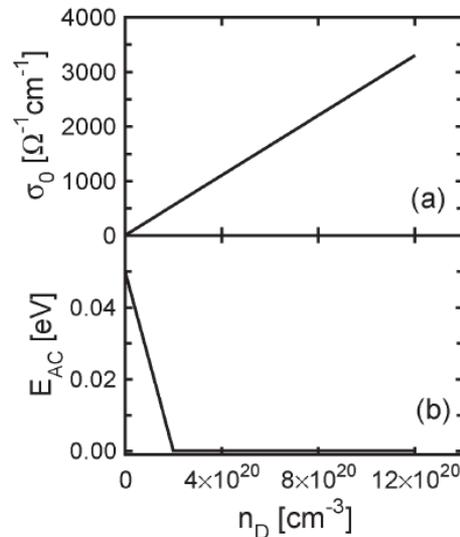
Oxygen vacancy filament conduction

- ▶ Oxygen vacancies influence conduction
 - Electron hopping from one vacancy to another
 - Act as local “doping” → thermally activated conduction
 - aka **VCM** : **valency change mechanism**
 - Create conductive defect band in Metal Oxide (e.g. at GB)

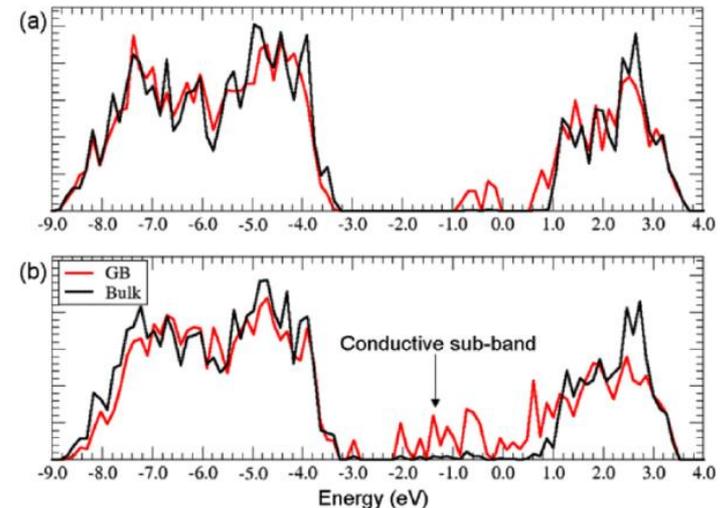
→ Metallic conduction



N.Xu et al,
VLSI Technology, 2008

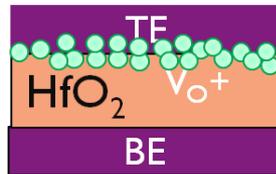


S.Larentis et al,
Trans. El.Dev. 59(9), 2012, p.
2468

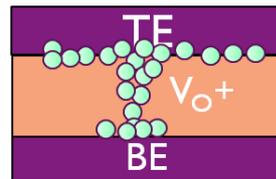


G.Bersuker et al.,
J. Appl. Phys. 110, 124518 (2011)

“Oxygen vacancy drift” based RRAM

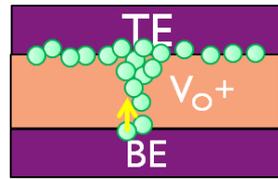
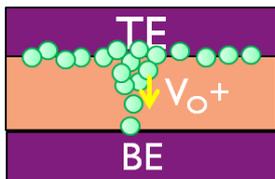


Forming

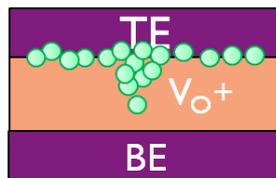


LRS

Set



Reset



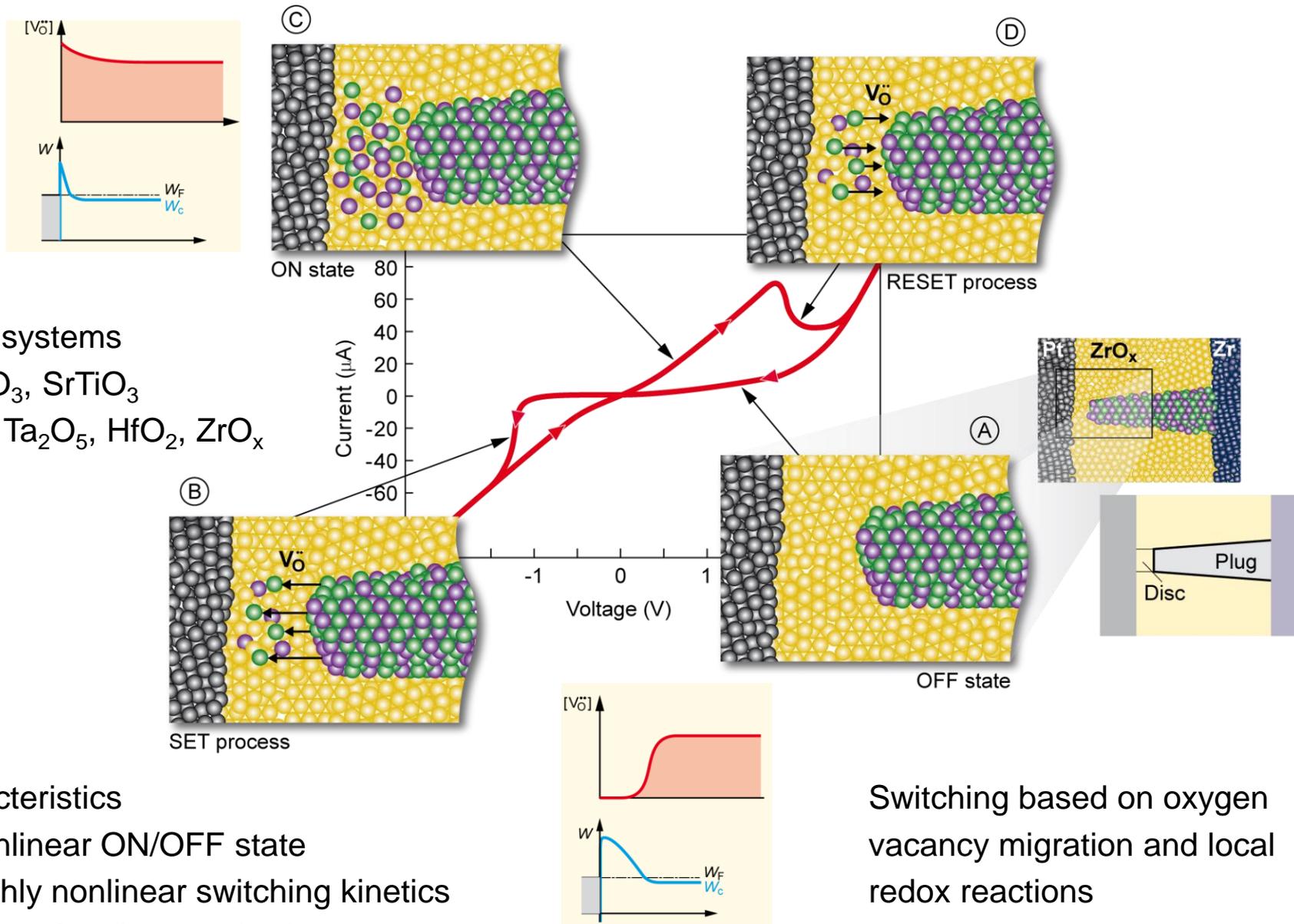
HRS

► Reset/Set :

- Transport = drift of oxygen vacancies
- Filament constriction shrinks/expands with drift of oxygen vacancies up/down

► Closed system:

- NO Generation/Recombination of V_O



Material systems

- SrZrO_3 , SrTiO_3
- TiO_2 , Ta_2O_5 , HfO_2 , ZrO_x

Characteristics

- Nonlinear ON/OFF state
- Highly nonlinear switching kinetics
- Electroforming required

Switching based on oxygen vacancy migration and local redox reactions

“Oxygen vacancy drift” based RRAM

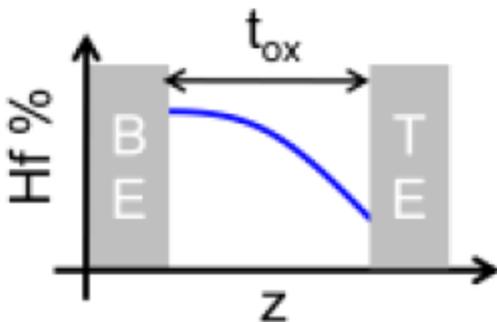
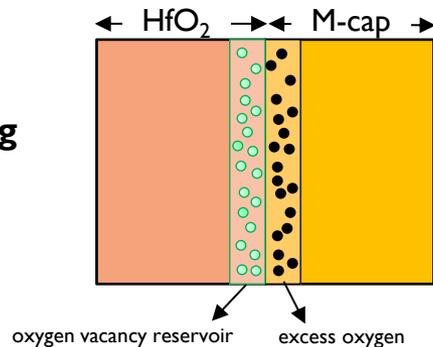
Stack



▶ **Controlled** introduction of oxygen vacancy by **process**

- Oxygen scavenging metal cap layer on top of stoichiometric HfO_2 (ALD)
 - Ti, Hf, Ta,....
 - Local formation of $\text{HfO}_{2-\delta}$
- Deposition of substoichiometric HfO_x (PVD)

After processing



▶ Need for **asymmetric** profile of oxygen vacancies

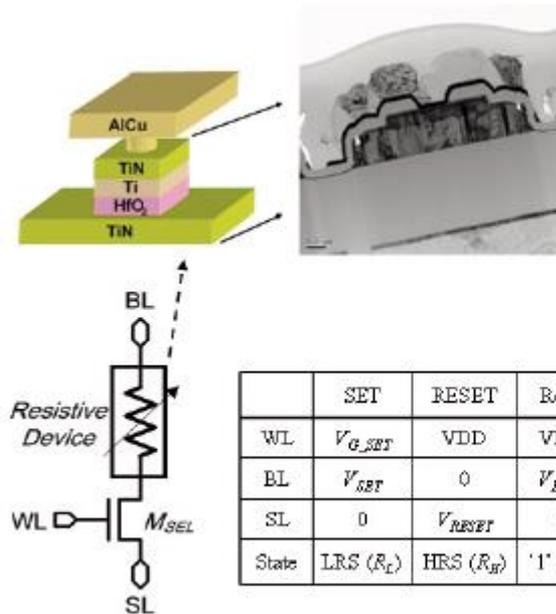
- Otherwise competing switching layers [1]

HfO₂ RRAM demonstrator

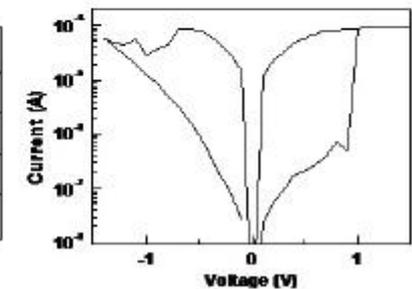
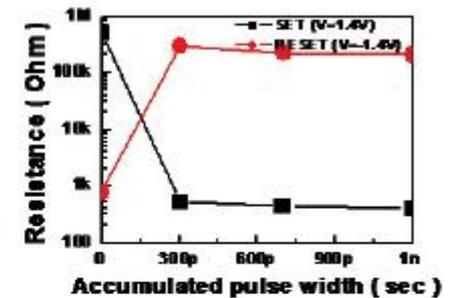
A 4Mb Embedded SLC Resistive-RAM Macro with 7.2ns Read-Write Random-Access Time and 160ns MLC-Access Capability



Process	CMOS: 0.18μm 1P4M ERAM: 0.64μm x 0.48μm
Memory Capacity	4Mb (32 x 128Kb sub-blocks)
Chip size	11310um x 16595um (with test-mode circuits)
Device	HV path: 3.3V device Cell array: 3.3V device Peripheral: 1.8V device
VDD	HV path: 3.3V Core: 1.8V
Read-Write Access Time (SLC-mode)	Random access: 7.2ns Burst-mode: 3.6ns



	SET	RESET	Read
WL	V_{G_SET}	VDD	VDD
BL	V_{SET}	0	V_{BLR}
SL	0	V_{RESET}	0
State	LRS (R_L)	HRS (R_H)	'1' / '0'

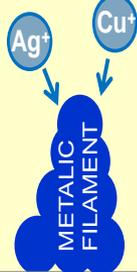


Conductive Bridge RRAM : “Programmable Metallization Cell”

1D
Filamentary

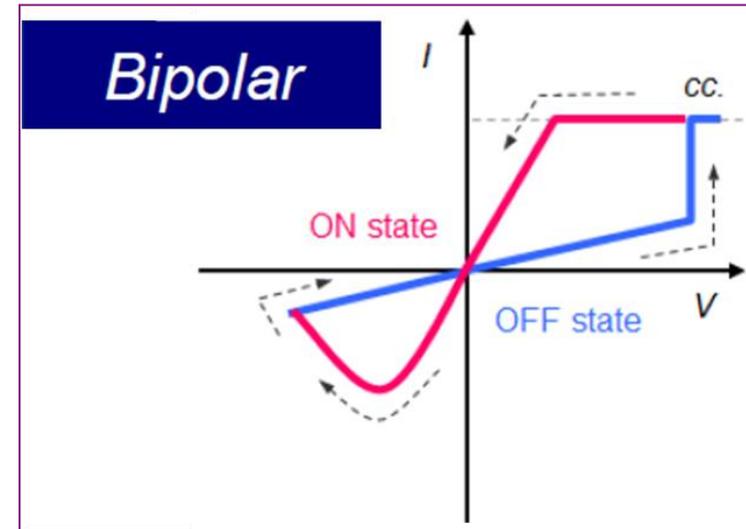
Electro-
chemical

Cation Source
(Ag⁺, Cu⁺ or...)



BE

BIPOLAR



Material :
Ag or Cu based

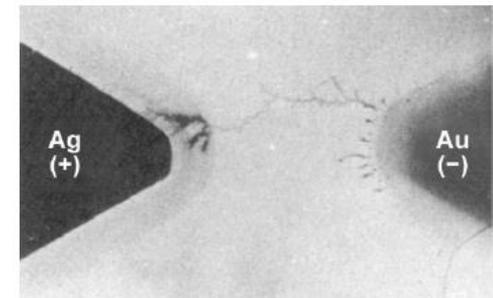
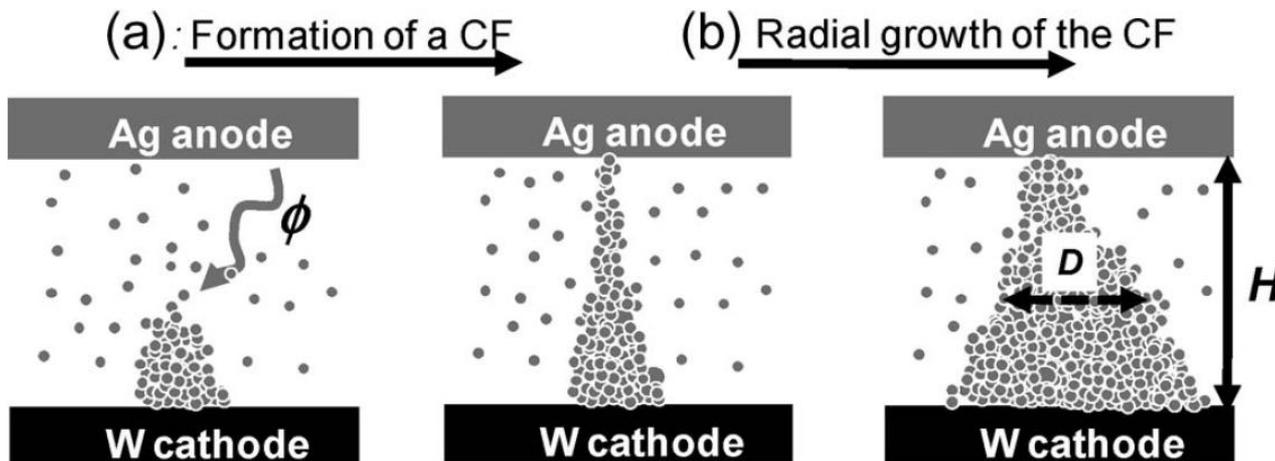
Ag/Cu electrode



Inert electrode

Electrochemical filament formation

- ▶ Oxidation at anode: forming of metal ions ($\text{Ag} \rightarrow \text{Ag}^+ + \text{e}^-$)
- ▶ Drift of metal ions through insulating switching layer
- ▶ Reduction at cathode: plating out of metal ions ($\text{Ag}^+ + \text{e}^- \rightarrow \text{Ag}$)
 - Growing filament forms “virtual cathode”



Rainer Waser et al., Adv. Mater. 2009, 21, 2632–2663

U. Russo et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, 56(5), p. 1040, 2009

Material systems

- AgI, GeSe, GeS_x, Cu:TCNQ
- SrTiO₃, SiO₂, WO_x
- TiO₂, Ta₂O₅, HfO₂

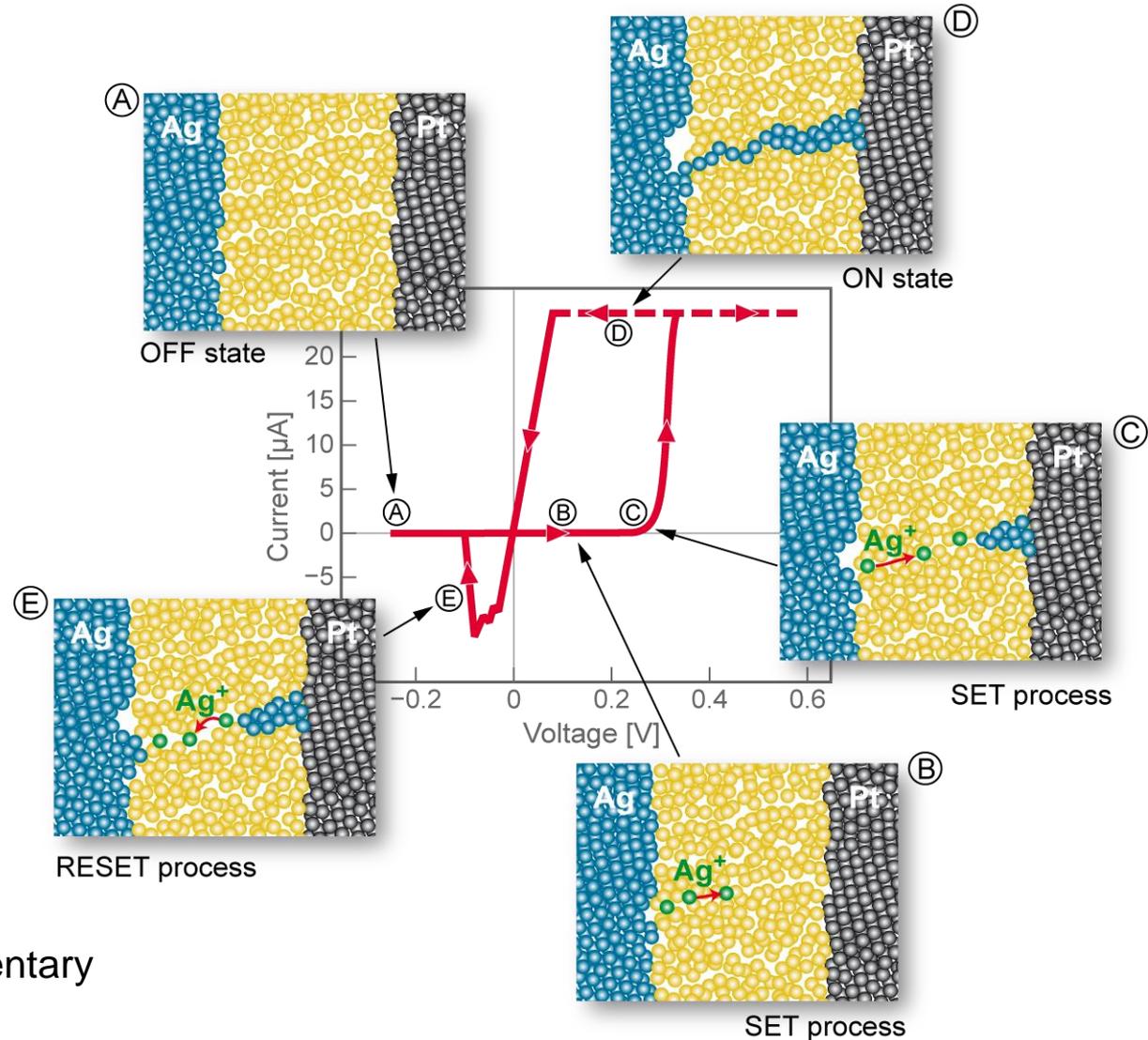
Electrodes

- Ag or Cu active electrode
- One inert electrode

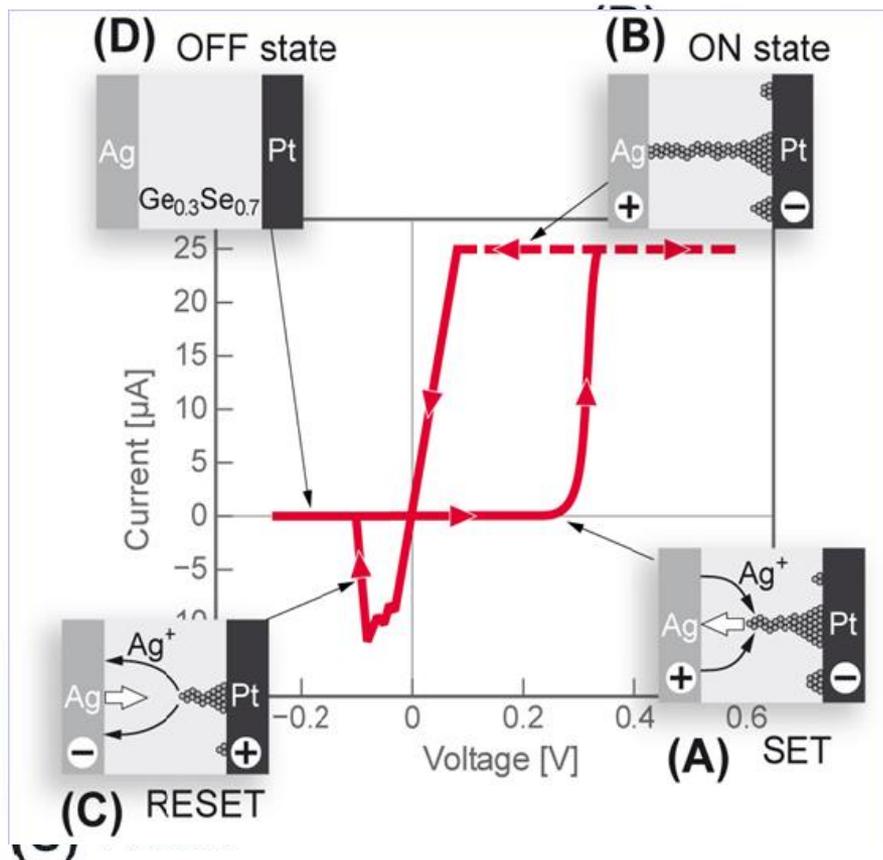
I-V Characteristics

- Linear I-V in ON state
- Nonlinear OFF state

Switching based on Ag/Cu filamentary growth and dissolution



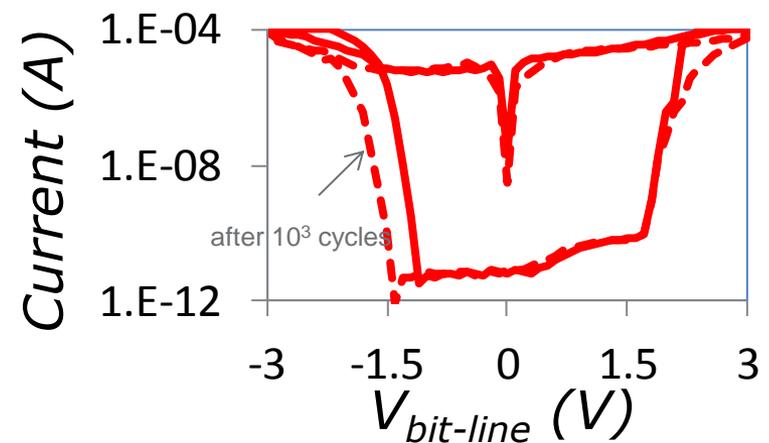
Bipolar Switching



C. Schindler et al., *IEEE T-ED*, 54 (2007) 2762

Asymmetric switching
 $\rightarrow V_{\text{RESET}} < V_{\text{SET}}$

Deep RESET
 \sim complete filament annihilation?

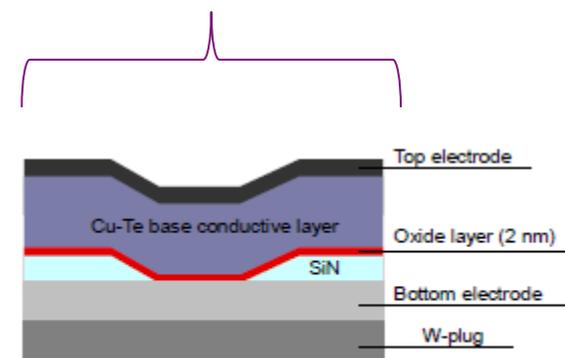
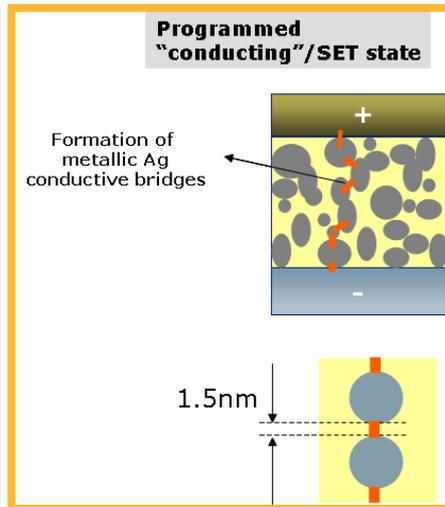
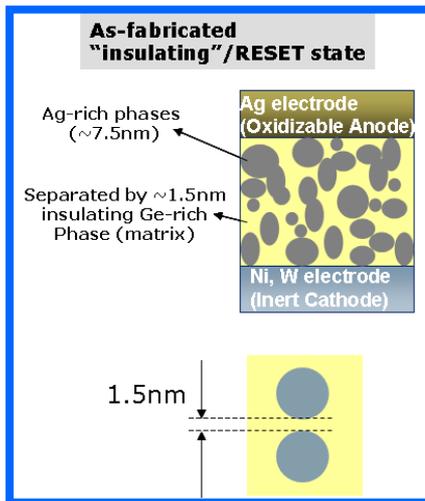
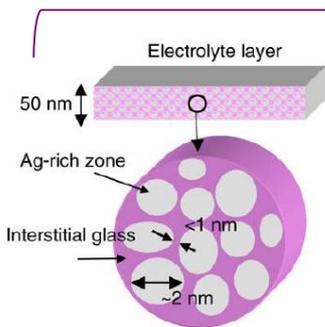
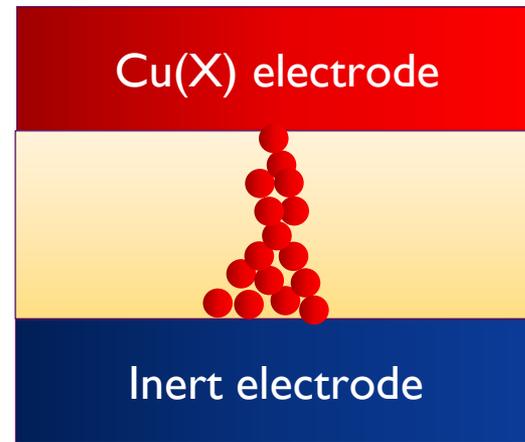
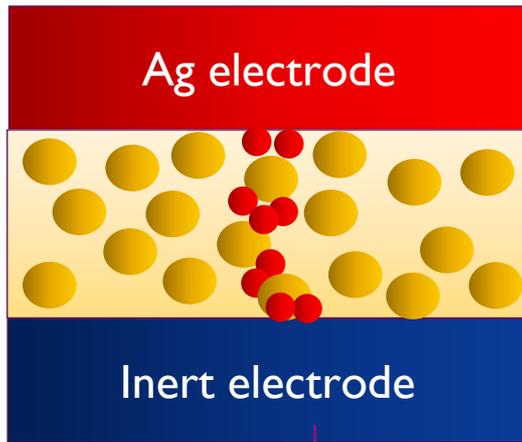


L.Goux et al., *VLSI Technology* 2012

Materials and Structures

1st generation : **Ag-doped chalcogenide**
All-in-one, non-homogeneous material

2nd generation: **Metal-Oxide**
Cu source separated from switching layer

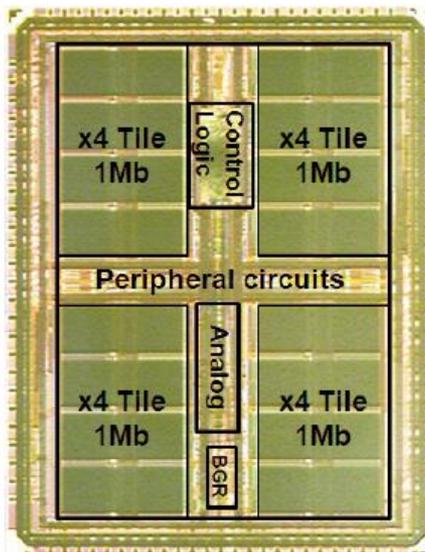


[1] M.Kozicki,
IEEE Trans. On
Nanotechnology
4(3), 331 (2005)

K.Aratani et al., IEDM 2007

SONY ISSCC 2011 CBRAM 1T1R

**A 4Mb Conductive-Bridge Resistive Memory with
2.3GB/s Read-Throughput and 216MB/s
Program-Throughput**



Capacity	4 Mb
Tile	256Kb
Process	180nm CMOS
Chip size	6.8x5.26mm 35.8 mm ²
Cell architecture	1T-1R
Cell size	2.24 μm ²
Power Supply	3.3 V, 1.8 V
Memory / IF clock	125MHz
Read Size, Throughput	128Byte 2.3GB/s
Program Size, Throughput	16Byte 216MB/s

Figure 11.7.1: Die micrograph and features.

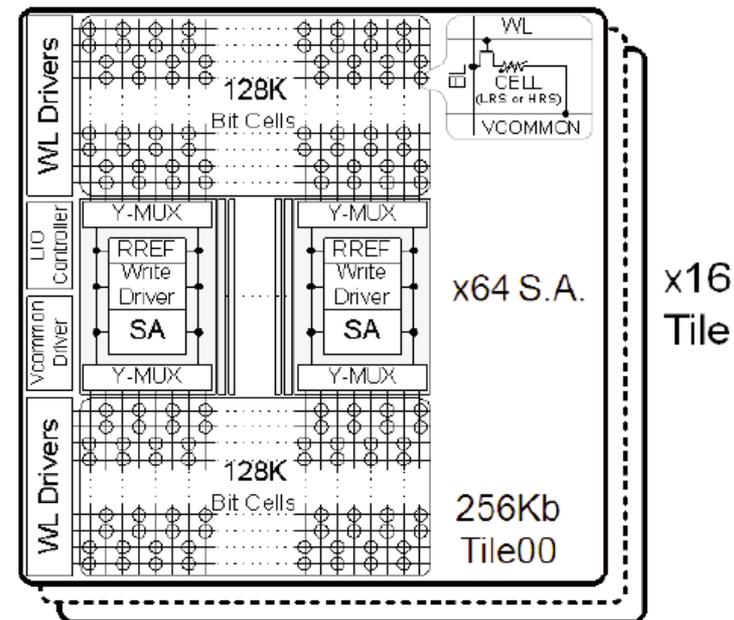


Figure 11.7.2: Array organization.

The Time-Voltage Dilemma

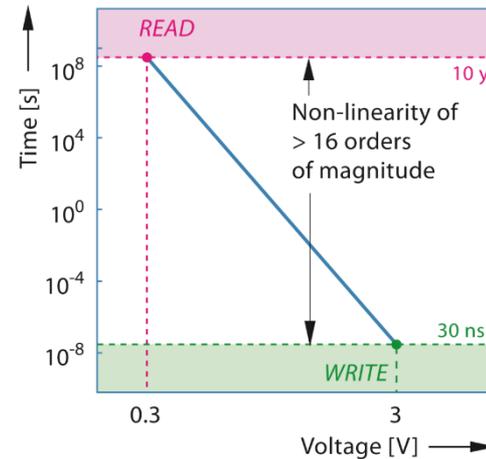
How can we make a 2-terminal NVM ?

Fast programming

- ▶ At $\sim 1\text{V}$, need programming in $\sim 10\text{nsec}$

Good retention

- ▶ At $\sim 0.1\text{V}$, need stable read for $\sim 10\text{ years}$

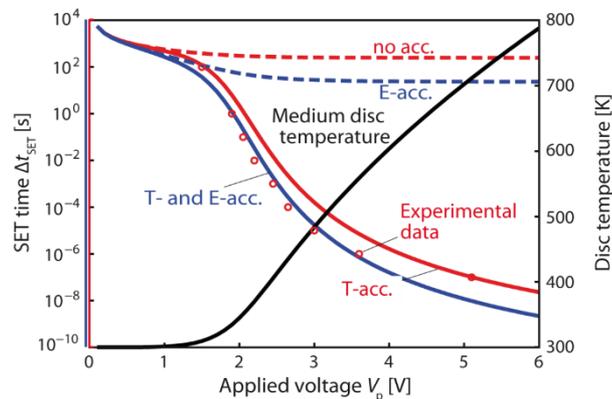


Need operation mechanism with extreme non-linear behavior:

>15 orders of magnitude in time over 1 decade in voltage

Further comparison of 2 types of bipolar switching RRAM : different kinetics

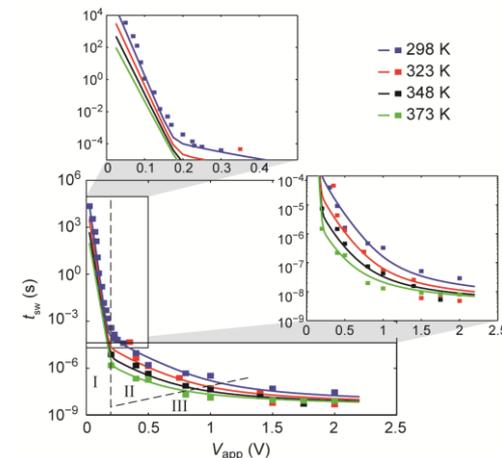
- ▶ Oxygen vacancy defect based cells (also called VMC cells)



Menzel et al., Adv. Funct. Mat 2011

- Drift of oxygen vacancies requires strong **thermal activation**
- Limit of min current (> 1 μ A, typically few 10 of μ A's)
- Limits RESET depth

- ▶ Metal cation based cells (ECM cells)



Switching kinetics are limited by

- I: Nucleation
- II: Electron transfer reactions
- III: Electron transfer reactions and ion hopping transport

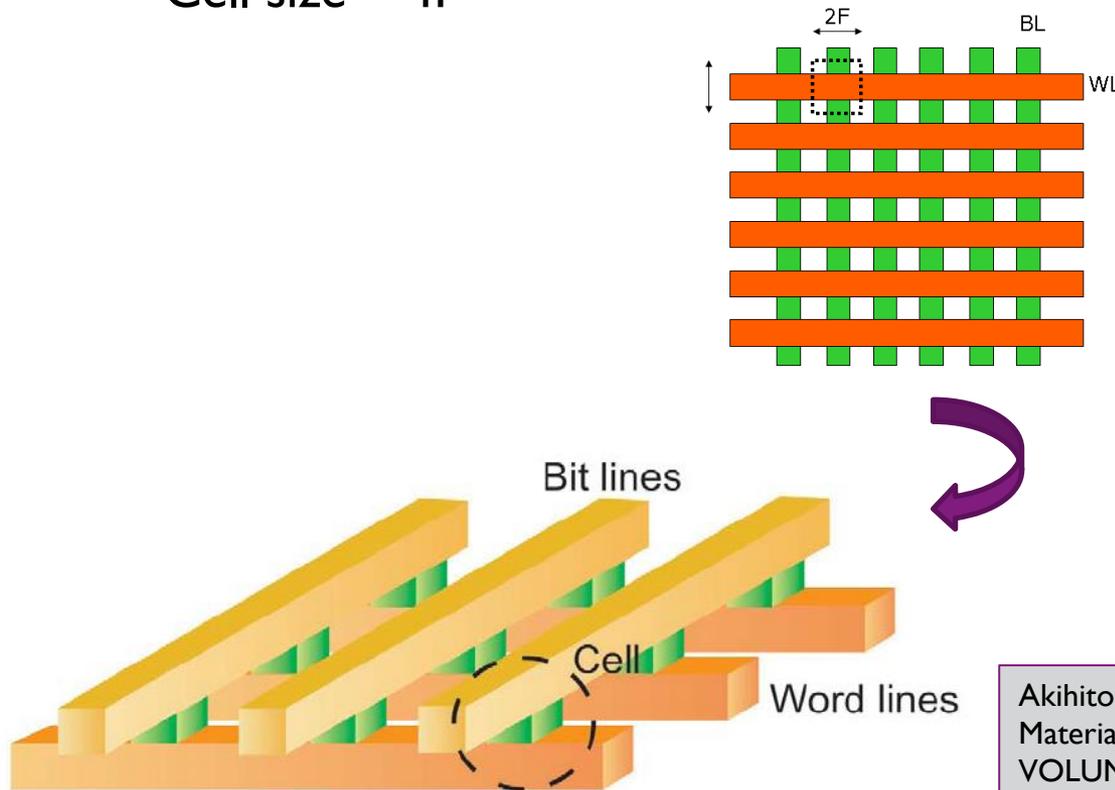
SET kinetics can be modeled by E-activation only

S. Menzel et al., Phys. Chem. Chem. Phys., 15, 18 (2013)

- Drift of metal cations possible **without thermal activation**
- Lower current operation possible
- Strong RESET
- compromised retention

RRAM Cell and Array configurations

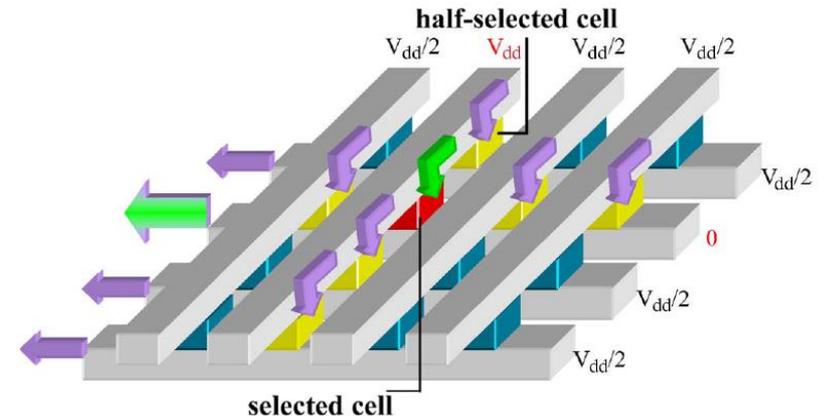
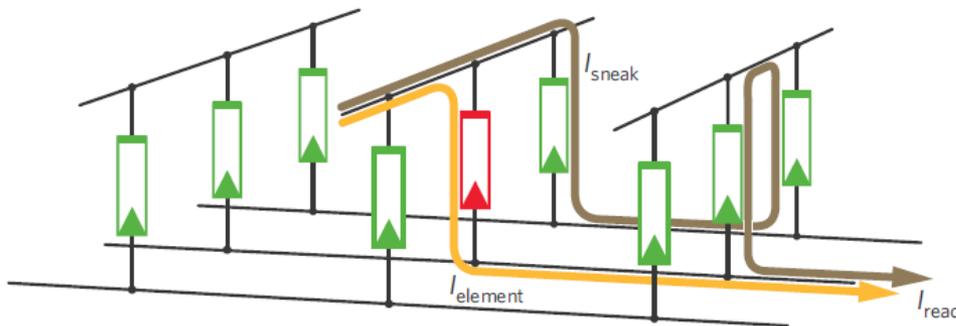
- ▶ RRAM element = RRAM cell ?
 - Raw Cross Point array = highest density configuration
 - Cell size = $4F^2$



Akihito Sawa,
MaterialsTodayJUNE 2008 |
VOLUME 11 | NUMBER 6 p. 28

RAW XP LIMITATIONS

- ▶ Read errors due to sneak current paths
- ▶ Program disturbs on half-select cells (1/2 or 1/3 V scheme)
- ▶ Power dissipation due to current through half-selected cells



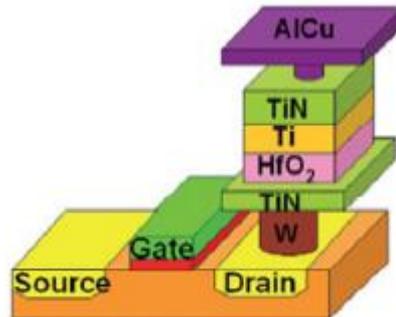
E.Linn en al, NATURE MATERIALS VOL 9 p. 403 MAY 2010

J.Liang et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 57, NO. 10, p.2532 OCTOBER 2010

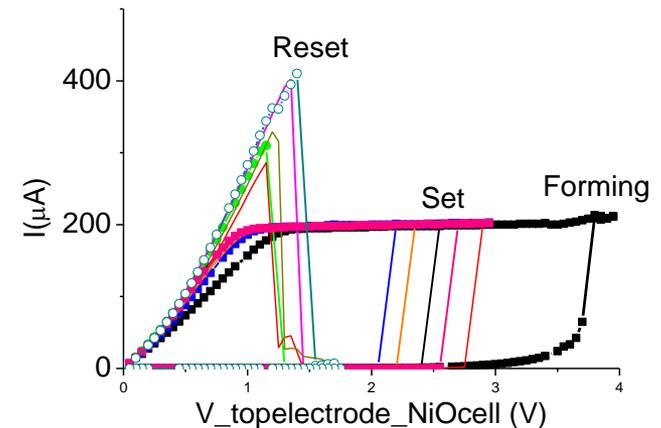
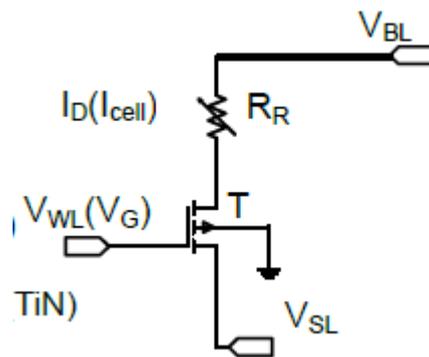
1T1R cell

Transistor is ideal selector

- ▶ Both isolation switch and current limiter (during SET)
- ▶ 3-terminal device : large cell
- ▶ Best suited for embedded RRAM



F,Chen ITRI

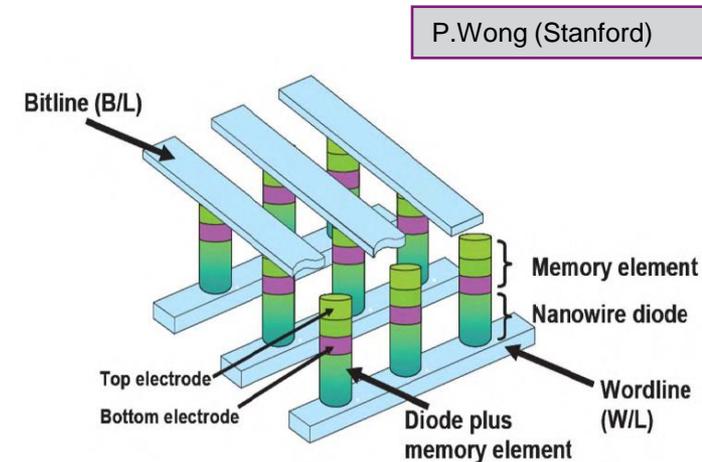


F.Nardi et al, IMW 2010

1D1R -1S1R cell

▶ Diode selector

- Good selector : strong asymmetry (rectification) combined with strong (exponential) non-linearity
- 2 terminal selector on top of RRAM
 - Small cell size possible
- Only for unipolar switching RRAM
- Voltage drop over diode
- Large aspect ratio



▶ For bipolar RRAM

- New 2 terminal selectors :
 - “Symmetric” diode type and Volatile Switching types

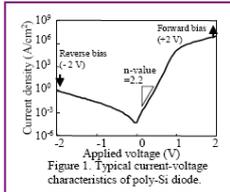
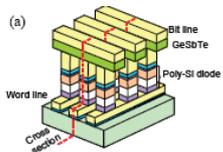
2- Terminal SELECTOR concepts

unipolar

bipolar

Diode types

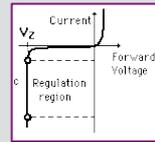
- p(i)n diode
- Schottky diode



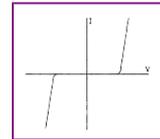
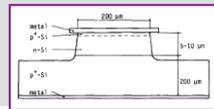
Y.Sasago et al, VLSI Tech.Symp. 2009

Symmetric diode type

-Zener



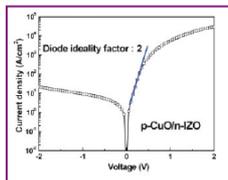
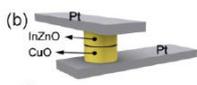
-Punch Through Diode



Using semiconducting material

Diode types

MO_x pn/Schottky diode



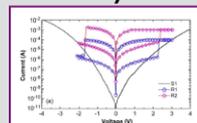
M-J. Lee, Advanced Functional Materials, 2008, 18, p.1

J-J. Huang, IEDM 2011

Symmetric diode type

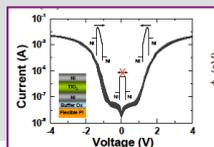
MO_x

- Schottky Diode



J-J. Huang, EDL 11(10) 2011

- Tunnel Diode



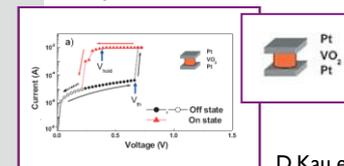
Volatile switching type

-MOTT VO₂

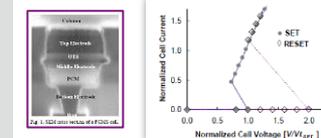
-OTS Chalcogenide

-MIEC Ion Conductor

M-J. Lee, Advanced Materials, 2007, 19, p.3919



D.Kau et al, IEDM 2009

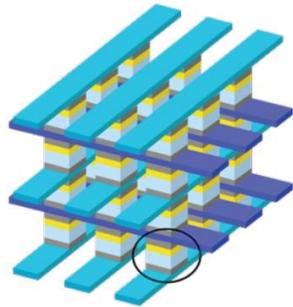


K.Gopalankhrisnan et al. VLSI 2010

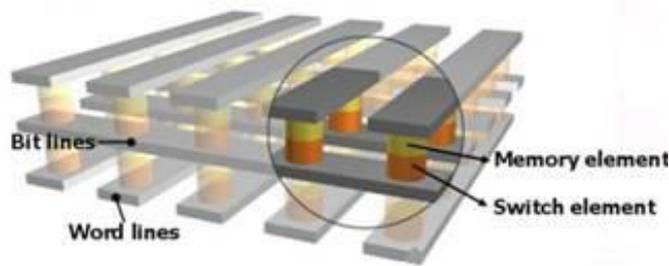
novel materials

3D RRAM ARRAY OPTIONS

3D Stackable RRAM



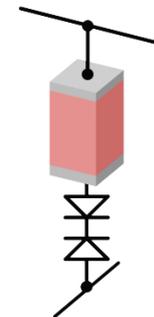
“pseudo 3D” = 2D stacking



M. Lee, et al., IEDM Tech. Dig. 2007



3D Matrix, *Semiconductor International*, 7 Jan. 2005



ISIR

3D RRAM ARRAY OPTIONS

3D Stackable RRAM

3D VRRAM

“true” 3D

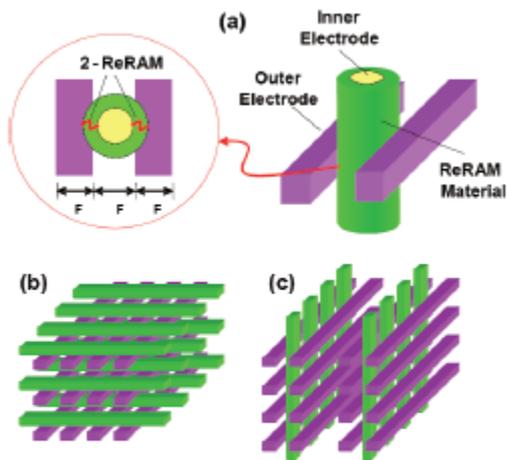
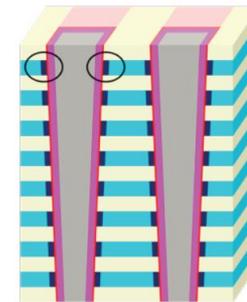


Fig. 1 Schematic diagram of (a) an unit vertically-defined ReRAM cell, (b) horizontal cross-point architecture (HCPA), and (c) vertical cross-point architecture (VCPA).

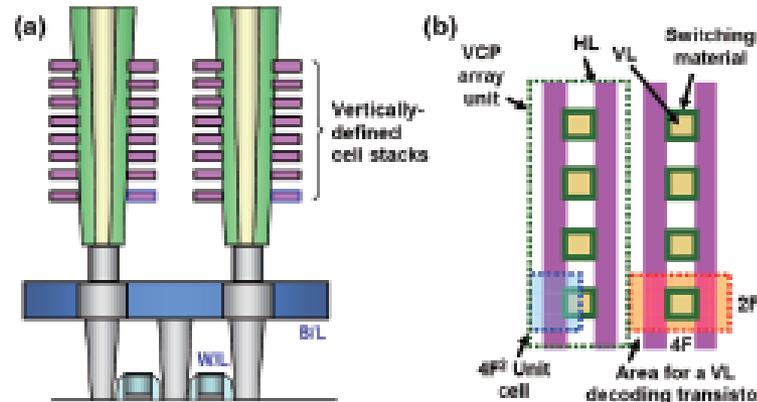
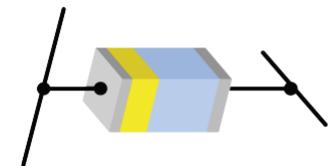


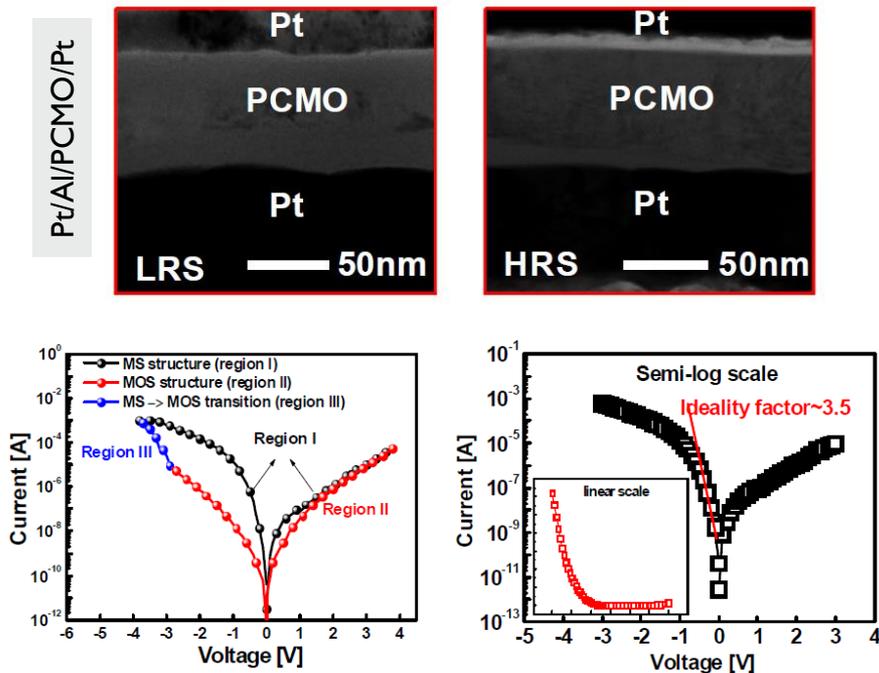
Fig. 10 (a) Vertical view and (b) top view of VCPA ReRAM with $4F^2$ memory cell densities.



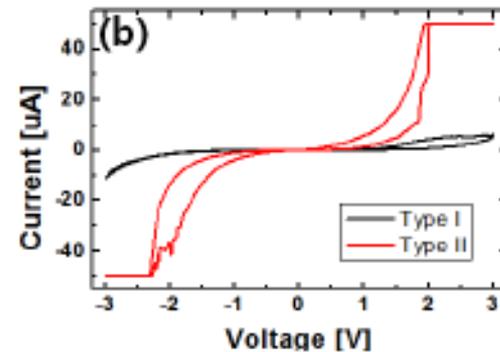
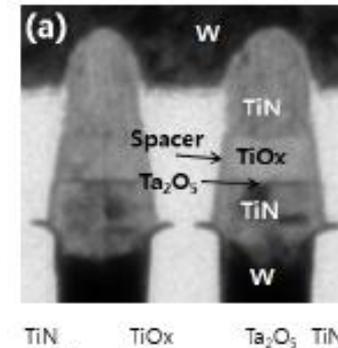
No place for selector !
→ SRC

Self Rectifying Cell

- ▶ Cell with strong nonlinearity (in ON state)
- ▶ Some proposals, but still limited nonlinearity

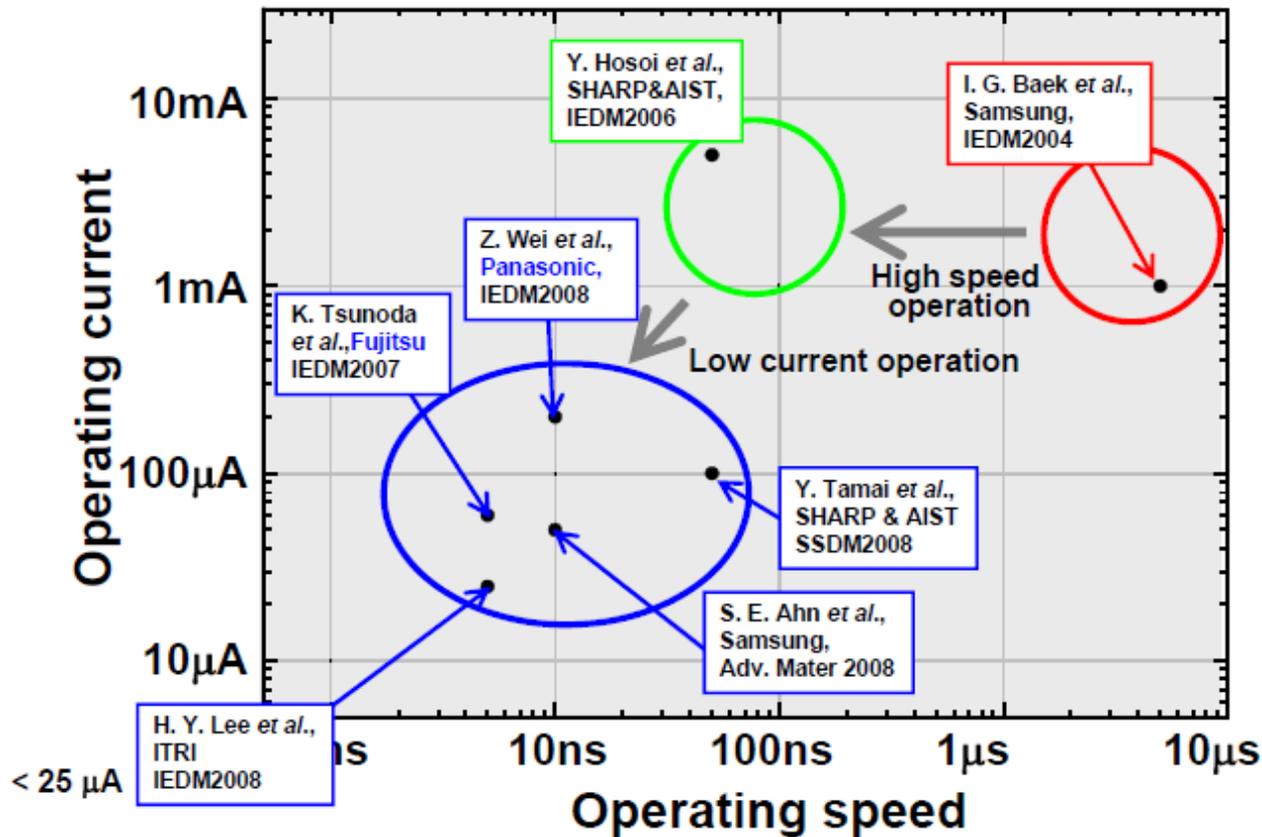


M.Jo et al, VLSI Tech. 2010

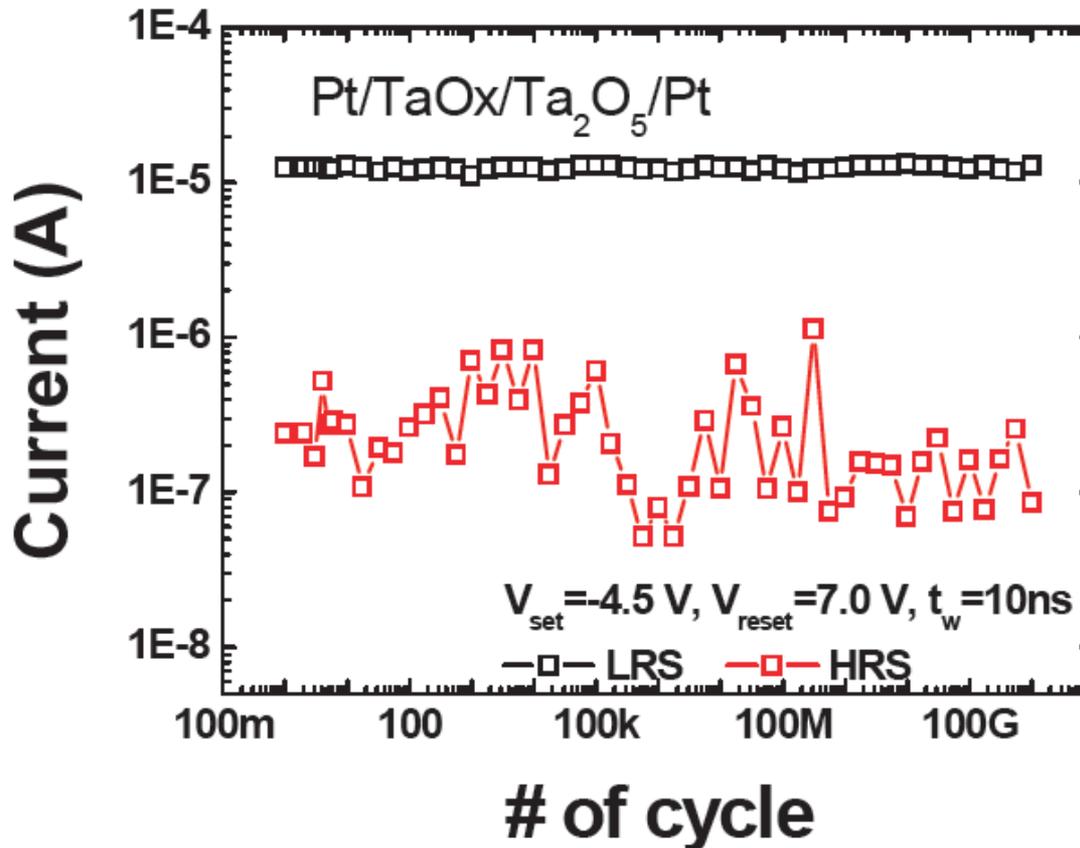


Hynix VLSI Tech. 2012

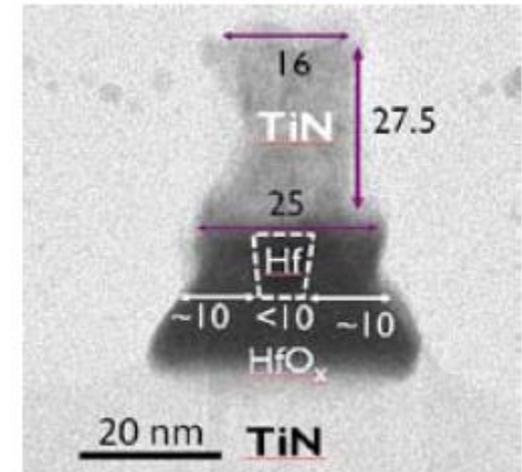
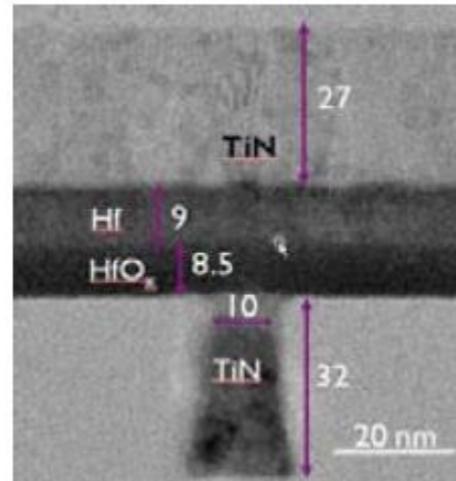
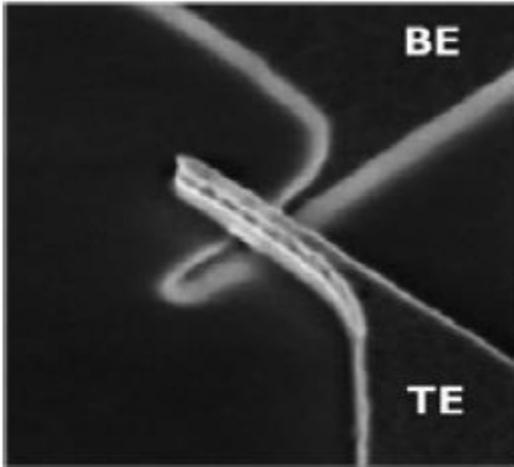
Steady improvement of RRAM operation speed & current



$> 10^{12}$ cyclability in TaOx

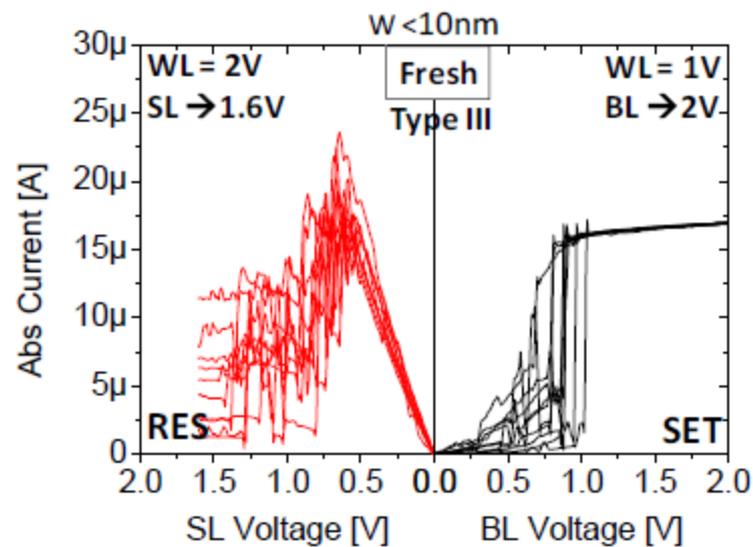


<10nm scalability of HfO₂ RRAM cells

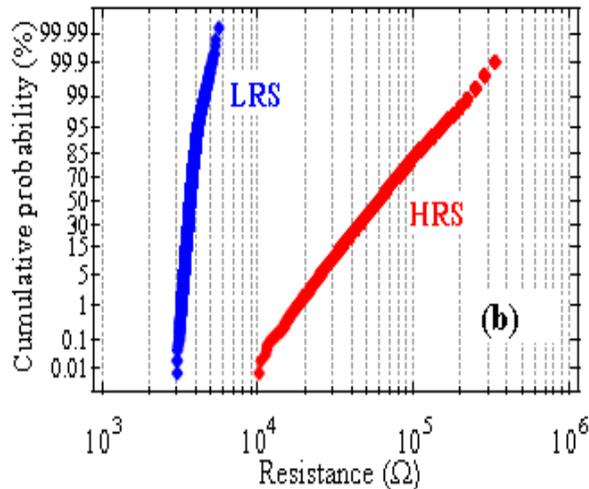
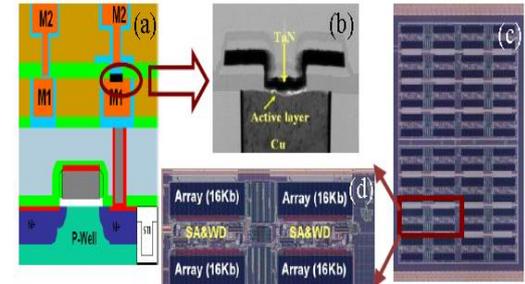
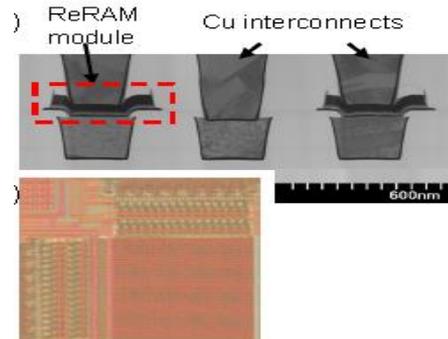
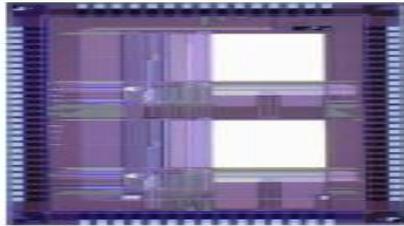


B.Govoreanu et al IEDM 2011

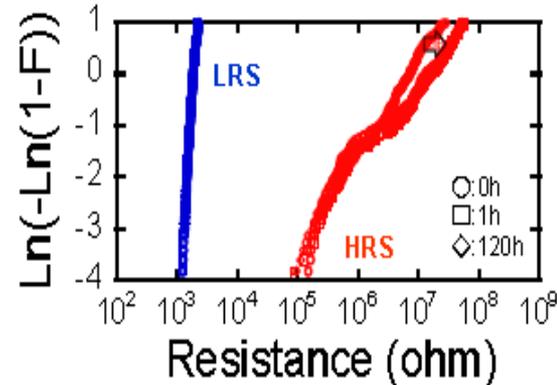
G.Kar et al VLSI 2012



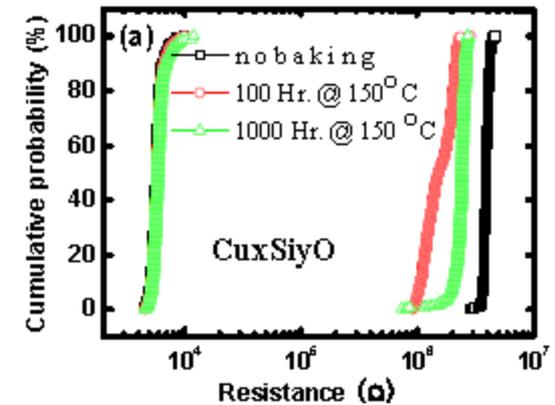
Array Demonstrations of 1T-1R RRAM



Pt/TaO_x/Pt
8kb bipolar array
Panasonic, IEDM 2008



Ru/TiO_x/TaO_x/Ru
1kb unipolar array
NEC, VLSI 2010



TaN/CuSi_xO_y/Cu
1Mb bipolar array
SMIC, VLSI 2010

Array Demonstrations of 1S-1R RRAM

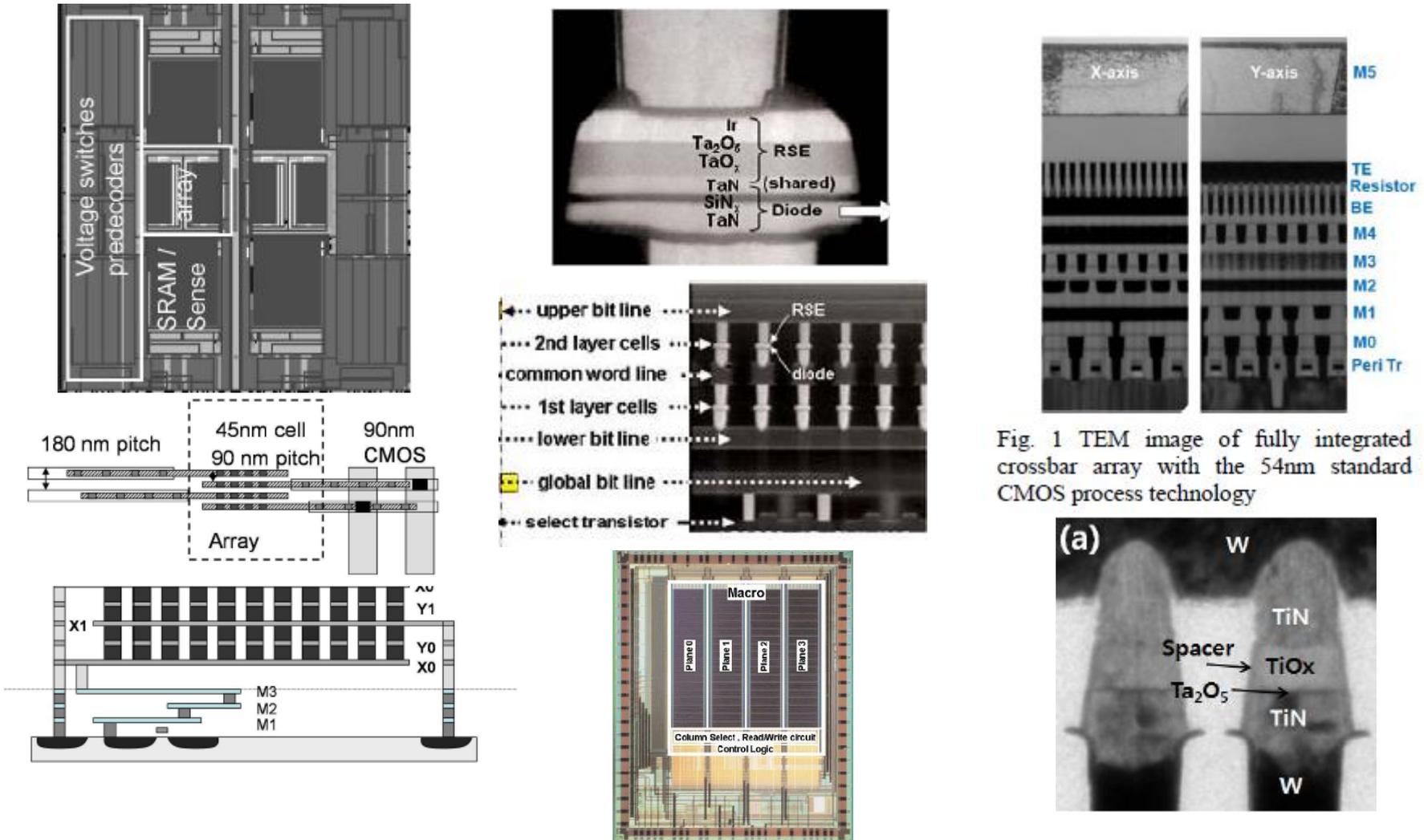


Fig. 1 TEM image of fully integrated crossbar array with the 54nm standard CMOS process technology

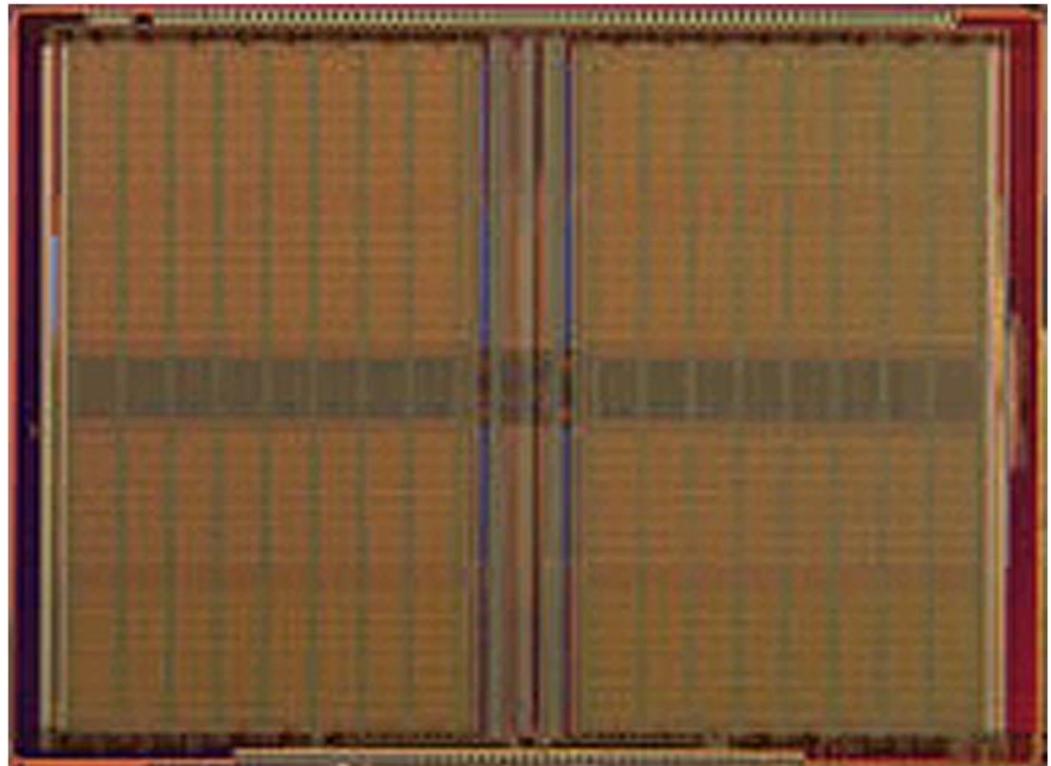
ELPIDA Elpida

Elpida announces ReRAM chip, aims to enter market 2013

Peter Clarke

1/25/2012 3:13 PM EST

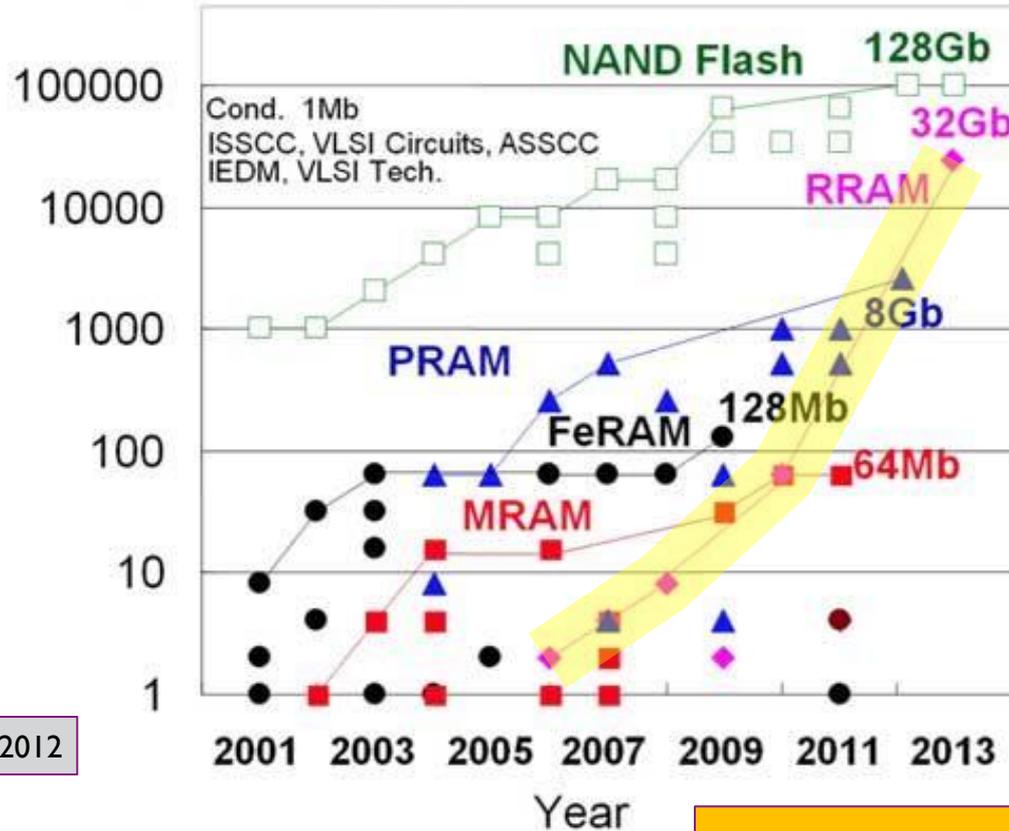
64Mb, 50nm process,
Collaboration with AIST and SHARP



Elpida Memory, Inc. 64 Megabit prototype ReRAM

Toshiba_Sandisk will announce a 32Gb 1D1R RRAM in 24nm @ ISSCC2013

Storage Capacity [Mb].



EETimes Asia 21 Nov. 2012

RRAM is fastly emerging !

Status - outlook

Main issue :

C2C variability, especially for HR/thin filaments
(lack of control of defect positions on atomic scale)
→ LRS/HRS distribution overlap

Application :

- embedded NVM (simple process, no HV)
- NAND Flash replacement (2D -3D): scalability
- Storage Class Memories : performance