Overview of Radiation Test Activities on Memories at ESA

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Outline

- Memories in space applications
  - Different types, usage in space
  - Availability on the market

- Radiation effects
  - Radiation Hardness Assurance
    - Utilisation of COTS in space

  - Typical examples of radiation effects in memories
    - PCRAM
    - NAND flash
    - SDRAM
    - SRAM

- Utilisation of COTS in-flight
    - Example: SRAM

Memories in space applications

- Program / Configuration Storage (BIOS, FPGA configuration, etc.):
  PROM / E²PROM, MRAM, NAND/NOR Flash

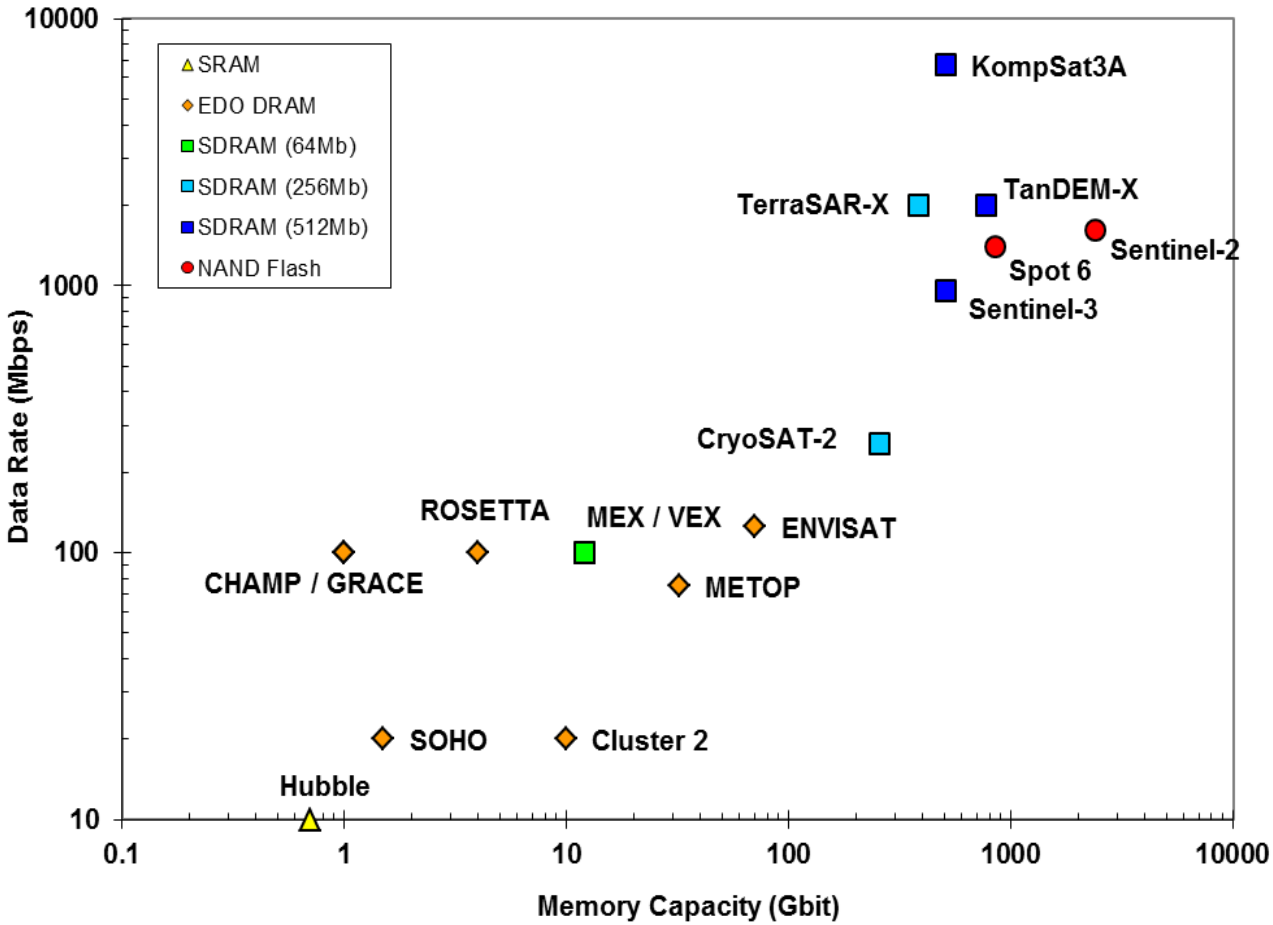
- Data Buffer (TM, HK, Instrument data, etc.):
  SRAM (async., sync., FIFO, DPRAM), SDRAM

- MPU/MCU Memory:
  SRAM (async., sync.), SDRAM

- Mass Memory
  - Platform Data Handling (OBC MM):
    SDRAM
  - Payload Data Handling (PDHU, SSR, Compression MMU):
    SDRAM, NAND Flash

[H. Schmidt, Airbus
under ESA contract, Nov. 2014]

Memories in Space Applications
Payload Data Handling

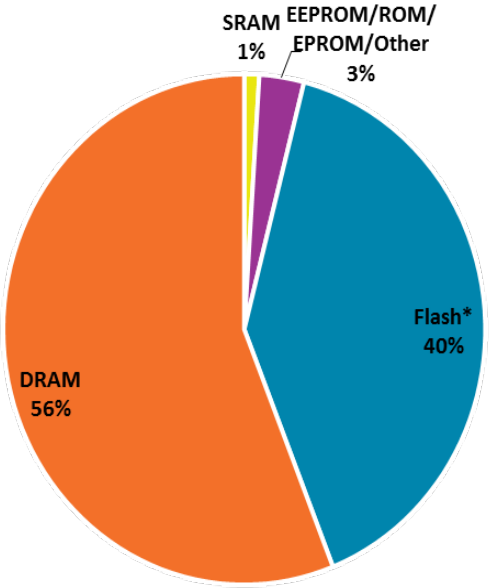


- **Increase of storage size:**
  → 10 Tbit (SAR, new optical instruments)
- **Increase of Data Rate:**
  → 10 Gbps (SAR)
- **Introduce of non-volatile memory to increase storage size at reduced power consumption and weight**

[H. Schmidt, Airbus under ESA contract, Nov. 2014]

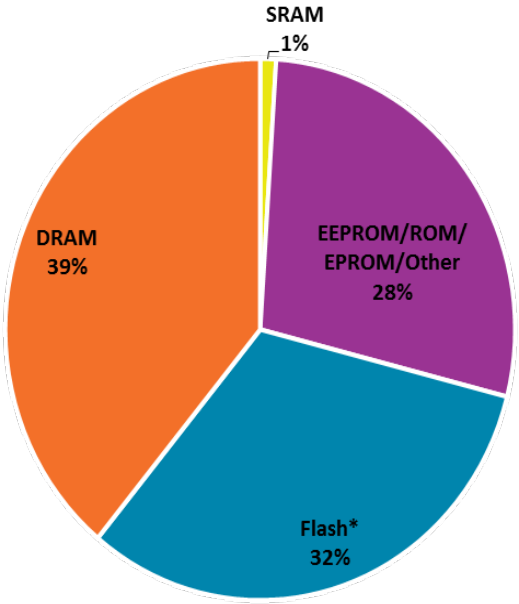
Market Analysis
Overview

2014 Forecast: Memory Market
(US$ 69.9 Billion)



* NAND = 37%
NOR = 3%

2014 Forecast: Memory Units
(33.5 Billion)



* NAND = 19%
NOR = 13%

Source: IC Insights

[H. Schmidt, Airbus under ESA contract, Nov. 2014]

Market Analysis
Overview

Volatile Memory

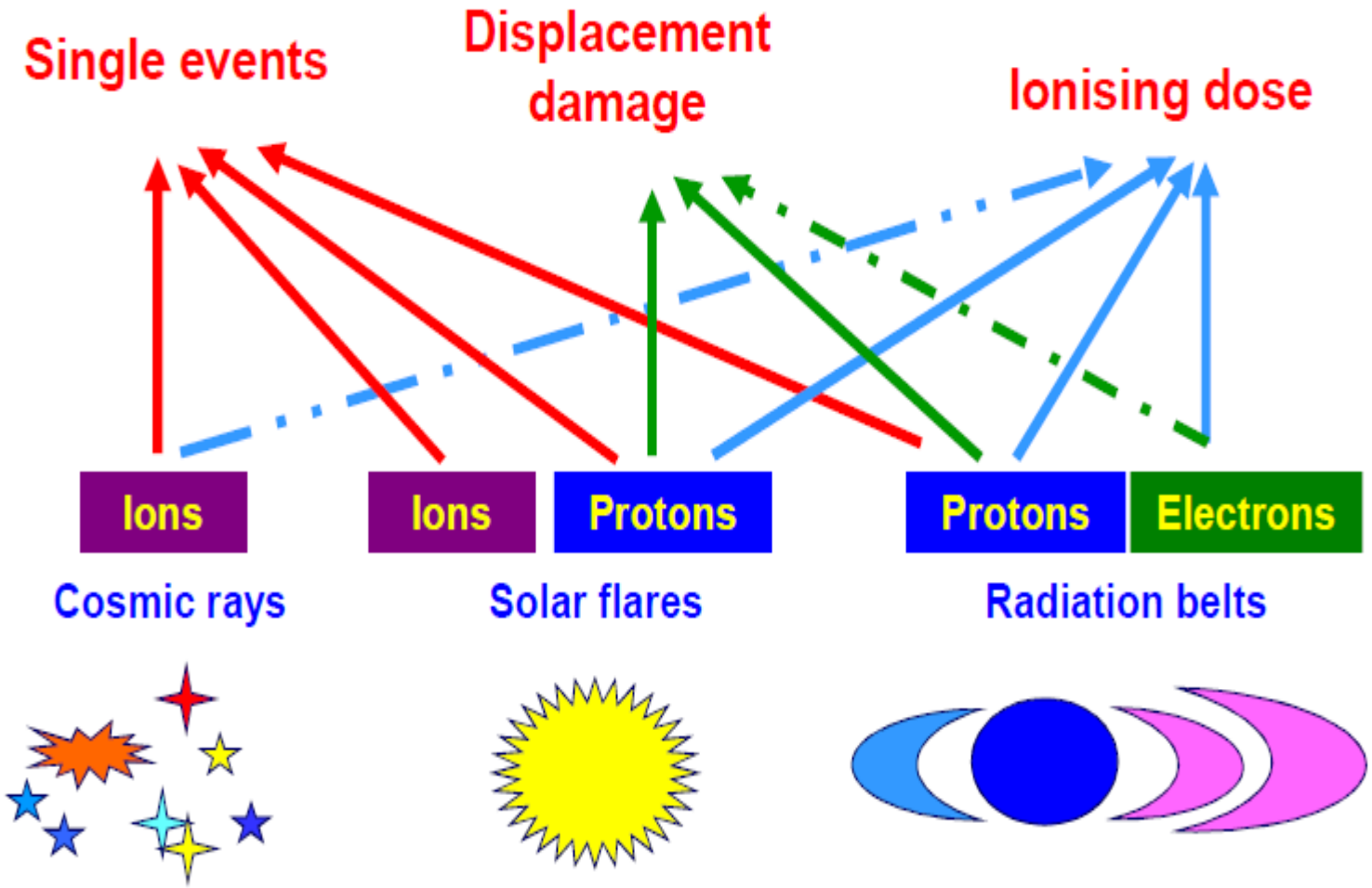
- SRAM
  - async. / sync. I/F
  - FIFO, DPRAM, etc.
- DRAM
  - Computing (SDR, DDRx SDRAM)
  - Mobile (LPDDRx)
  - Graphic (GDDRx,…)

Non-volatile Memory

- ROM / EPROM / E²PROM
- Flash
  - NOR (1 bit, 2 bits)
  - NAND (SLC, MLC, TLC, 3-D)
- MRAM
- PCRAM
- FeRAM
- ReRAM, …

[H. Schmidt, Airbus under ESA contract, Nov. 2014]

Main radiation effects in electronic components



[R. Ecoffet, TNS June 2013]

Radiation Hardness Assurance Application to Memories

ECSS-Q-ST-60-15C
Space product assurance –
Radiation hardness assurance –
EEE components

The flight lot is tested to:

- TID (Co60)
- SEE
  - high and low energy protons
  - Heavy ions
- Comparison to the mission environment and device function

Difficulty when using COTS components

COTS in space

Why use

- Complexity of function
- Performance
- Availability

[L. Adams, Radiation training course May 2003]

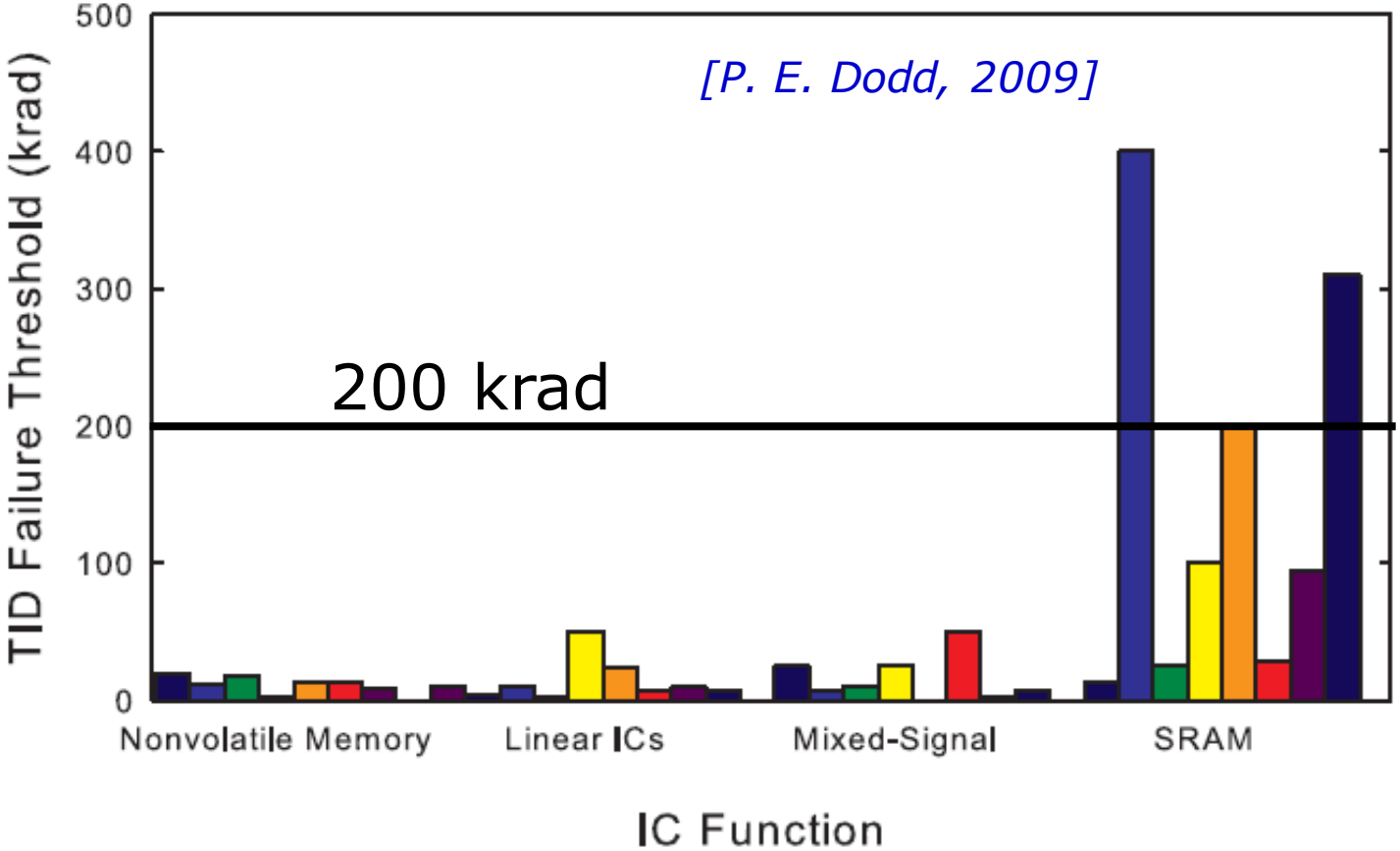
Drawback

- Little or no traceability
- Rapid and un-announced design and process changes
- Rapid obsolescence
- Packaging issues (plastic)
    - Effects of burn-in on radiation effects
    - Deep dielectric charging in space

Use of COTS

- The use of COTS does ***NOT*** necessarily result in cost saving
- Increase of the ***RISK***

Real systems use a large variety of IC technology and generations, Different TID hardness levels



Compilation from data workshops between 2002 and 2004

Examples of radiation effects in memories

PCRAM

- TID
- SEE: functional failures, SEFIs

Other memory types

NAND-Flash memories

- TID
- Destructive events

SDRAM

- Stuck bits
- SEFIs

SRAM

- MBU
- Sensitivity to low energy protons
- In-flight example of Latch-up

PCRAM

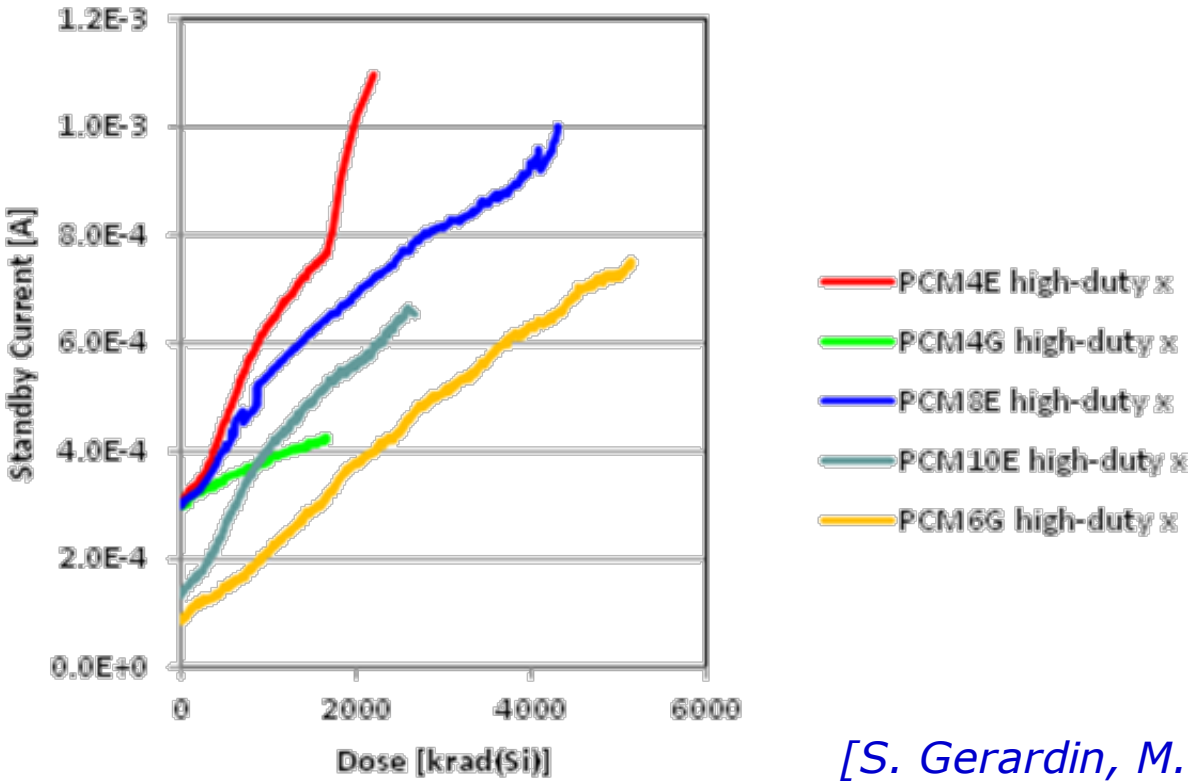
Micron (ex-Numonyx) Omneo P8P NP8P128A13TSM60E phase change memory Radiation test results

1. TID tests
    a. Co60: No functional failure up to 700 krad(Si) (also after annealing following irradiation)
    b. X-rays: No functional failures before 1.6 Mrad(Si), with one still functional above 4 Mrad(Si)
2. SEE tests
    a. Few SEUs under heavy ions at grazing angles
    b. latch-up in all operating conditions,
    c. to a minor extent single event functional interrupts, and bursts of read errors.
    d. Permanent functional failures were also observed in one revision of the chips.
    e. No events observed under high energy protons
3. Despite the very good TID tolerance, SEL may prevent these devices to be used in space.

[S. Gerardin, et al. IEEE TNS 2014]

[S. Gerardin, M. Bagatin, A. Paccagnella, U. Padova, 2013, ESA contract]

TID test of the Omneo P8P NP8P128A13TSM60E phase change memory

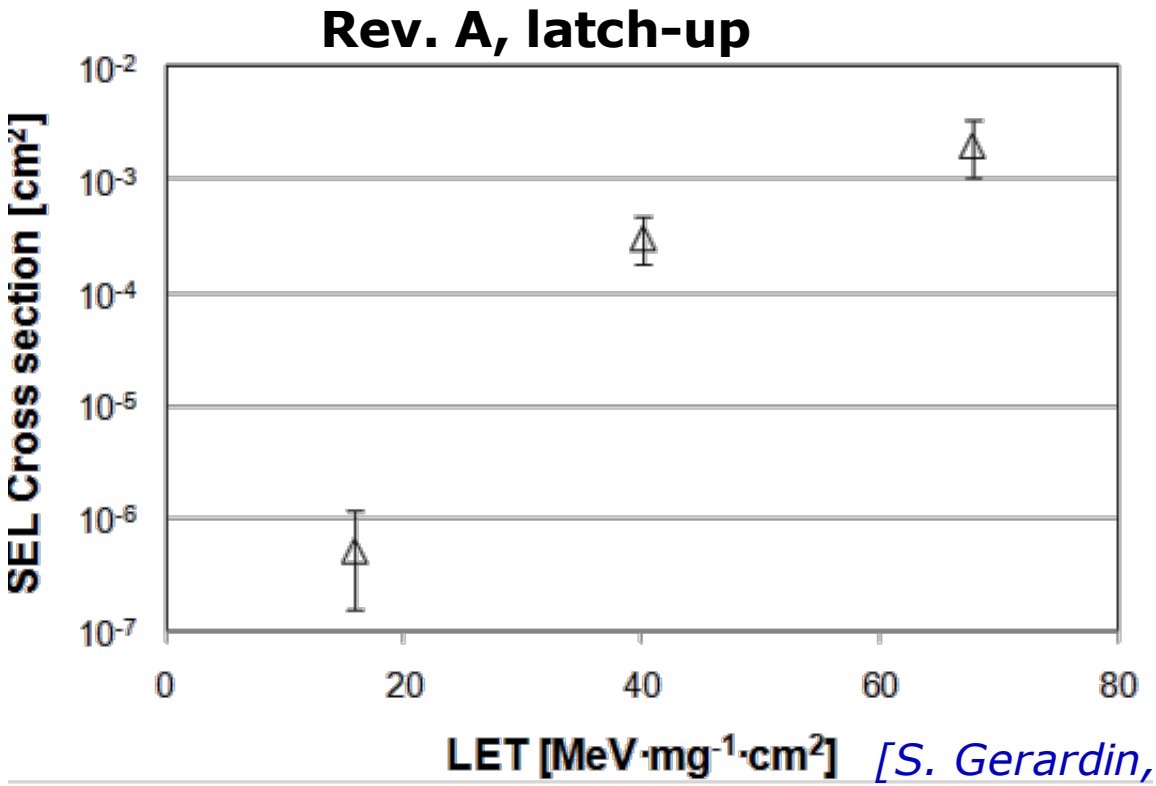


- Increase in the standby current as a function of x-ray received dose

[S. Gerardin, M. Bagatin, A. Paccagnella, U. Padova, 2013, ESA contract]

SEE test of the Omneo P8P NP8P128A13TSM60E phase change memory

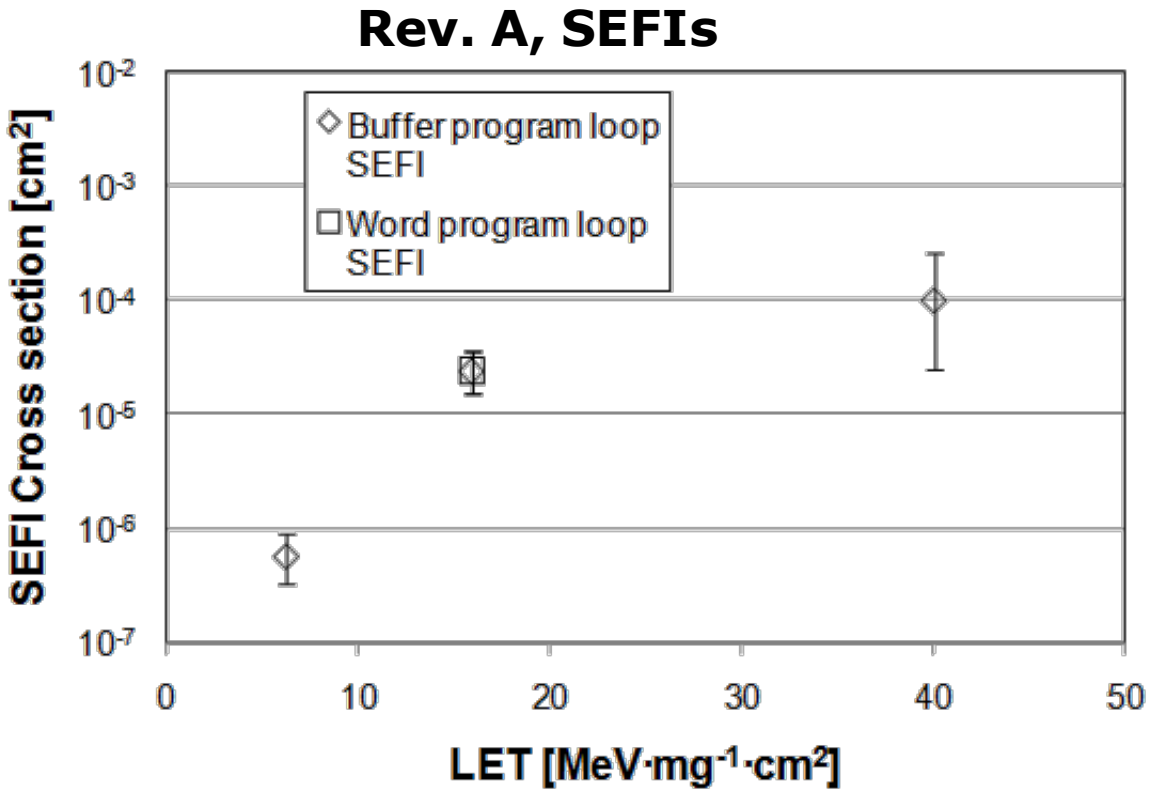
- Revision B of the die exhibited functional failure at low LET (3.3 MeVcm^2/mg)
- Revision A: SEL, SEFI



- In one case, sudden spike in the supply current, which after less than 1 s went back to its normal value, likely due to a logic conflict triggered by an SEU
- A previous report [O'Bryan et al. REDW 2010] indicated a lower SEL LET_{th} than found here, but likely due to different chip revision

[S. Gerardin, M. Bagatin, A. Paccagnella, U. Padova, 2013, ESA contract]

SEE test of the Omneo P8P NP8P128A13TSM60E phase change memory

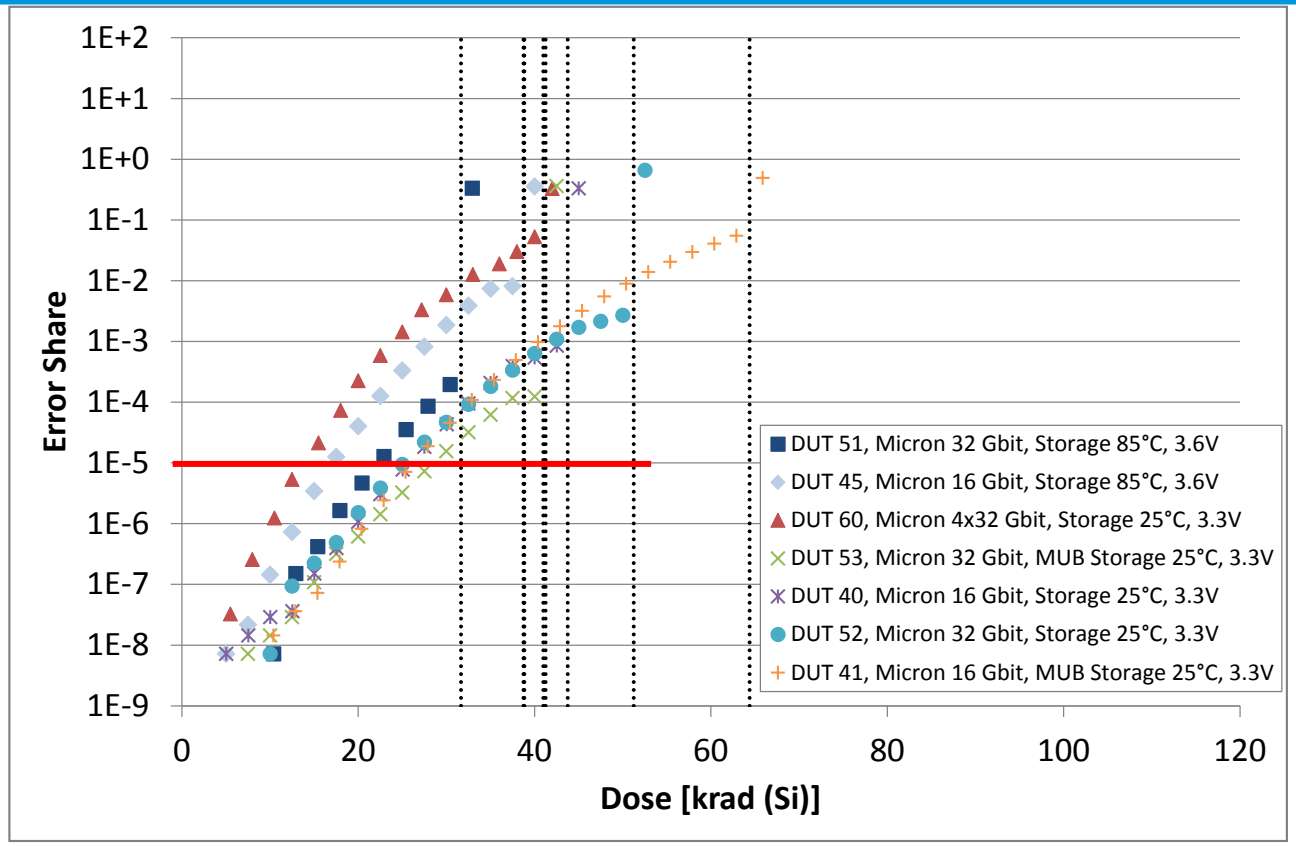


[S. Gerardin, M. Bagatin, A. Paccagnella, U. Padova, 2013, ESA contract]

- Errors signaled by dedicated bits in the status register (SR). Other times, the SR reports a successful operation, but a following read showed that the array had not been properly programmed
- Single Event Functional are likely due to heavy-ion strikes on sensitive regions of the microcontroller (few thousand bits)
- SEFI recovery:
  - At low LET: reset is effective most of the time
  - At high LET: a power-cycle is required in 50% of the cases
  - In few cases, repeating the operation is enough

Radiation effects in different types of memories

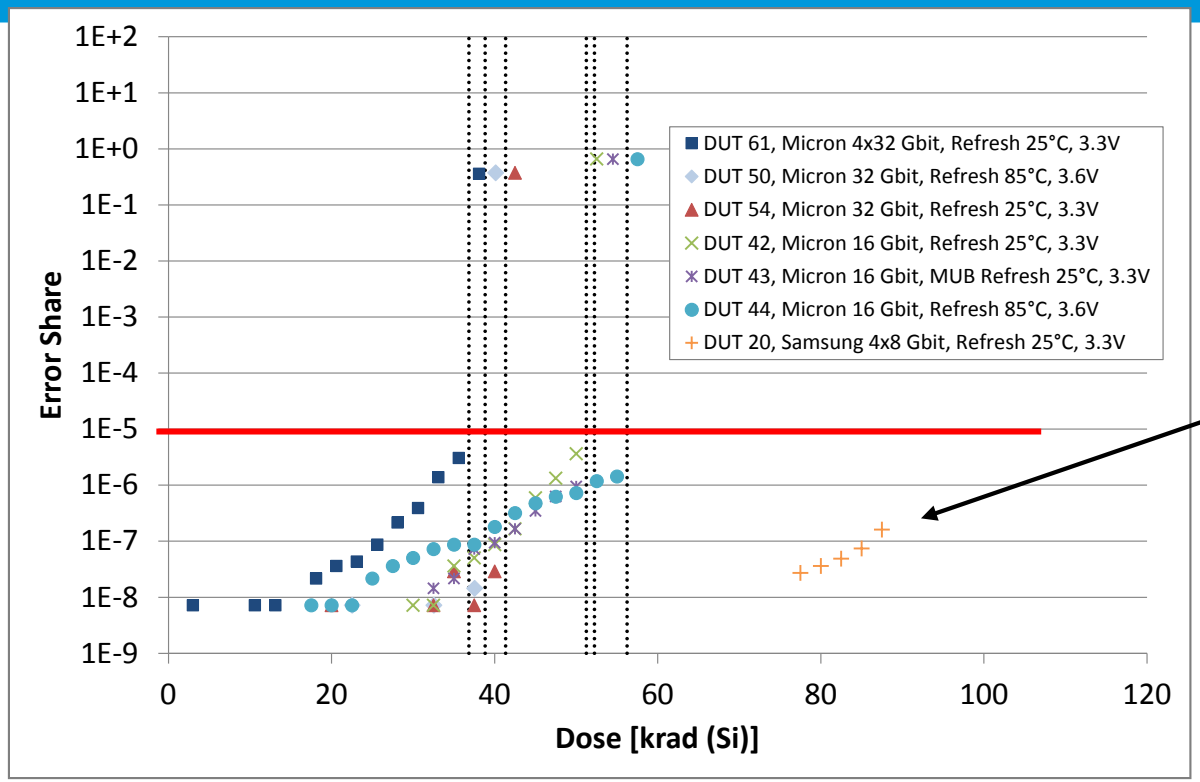
NAND-Flash TID: Errors in Storage Mode



[K. Grürmann, IDA, ESA contract 2012-2014]

- functional breakdown of each DUT is marked with dotted line
- first random data errors already between 5 and 10 krad(Si)
- Destructive Failure between 32 and 64 krad (Si)

NAND-Flash TID: Errors in Refresh Mode



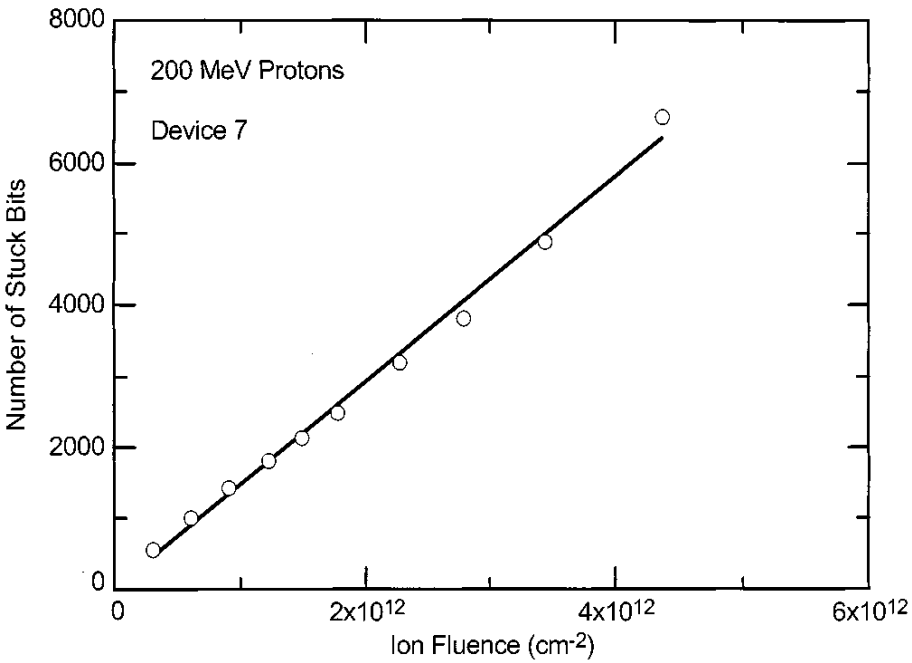
[K. Grürmann, IDA, ESA contract 2012-2014]

Samsung 51nm: first SEUs after 70 krad(Si), no functional breakdown until end of test at 90 krad(Si)

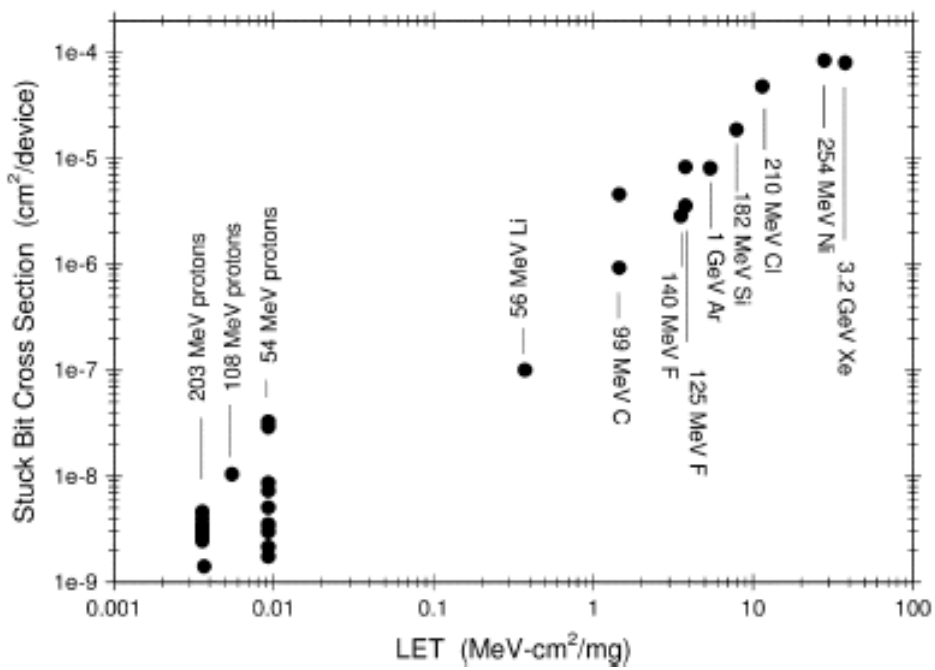
- Refresh every 2.5 krad(Si)
- first random data errors already between 3 and 30 krad(Si)
- periodic refresh keeps the error share below $1 \cdot 10^{-5}$, tolerable before ECC
- Refresh has no influence on the Destructive Failure
- with periodic refresh the Destructive Failure occurrence determines the total dose

Single Event Hard Errors: stuck bits

Samsung 1Gbits DDR1 SDRAM



Hyundai 64-Mb SDRAM



Large part to part variations

[Edmonds 2001]

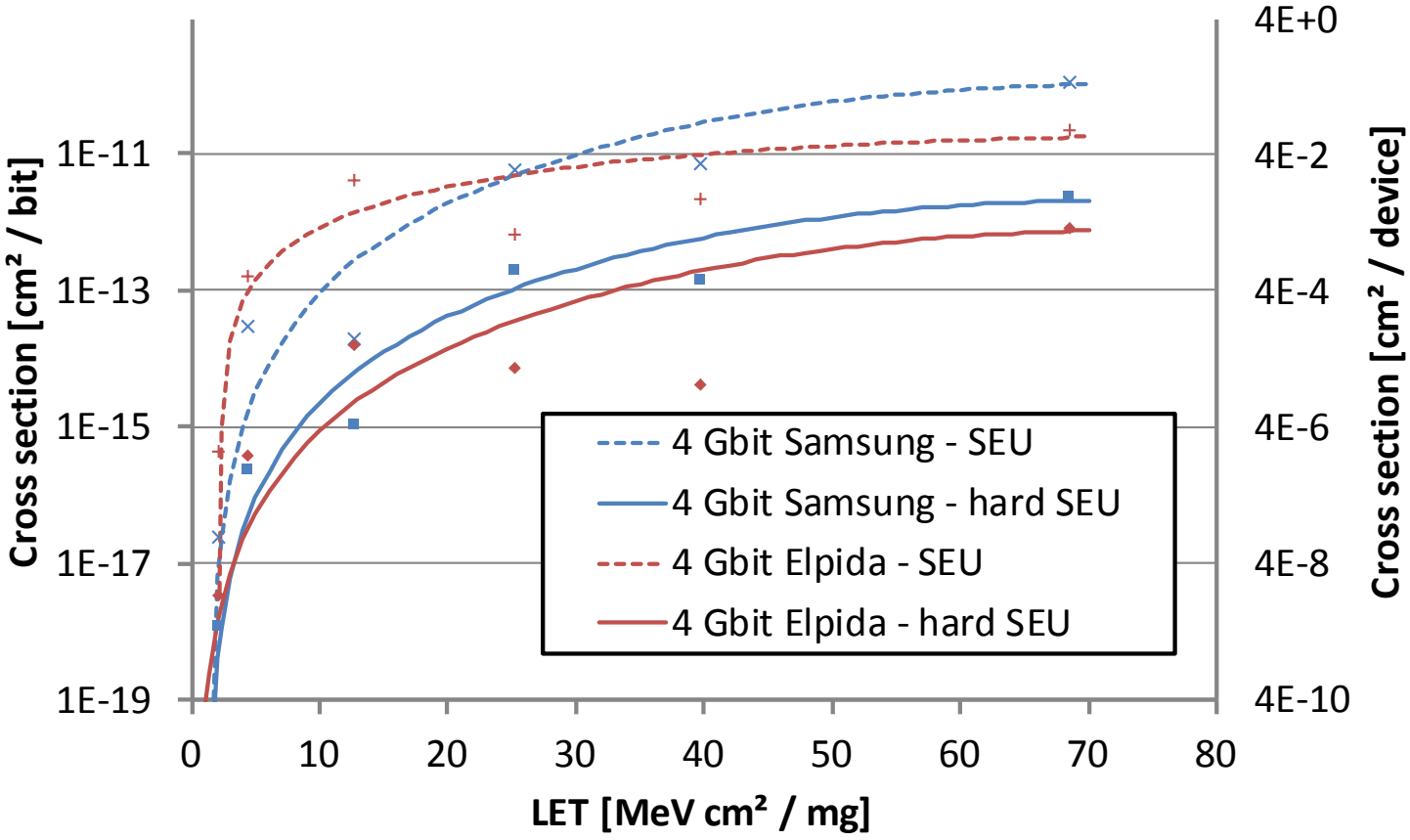
Micro-dose or displacement damage

[Edmonds 2008]

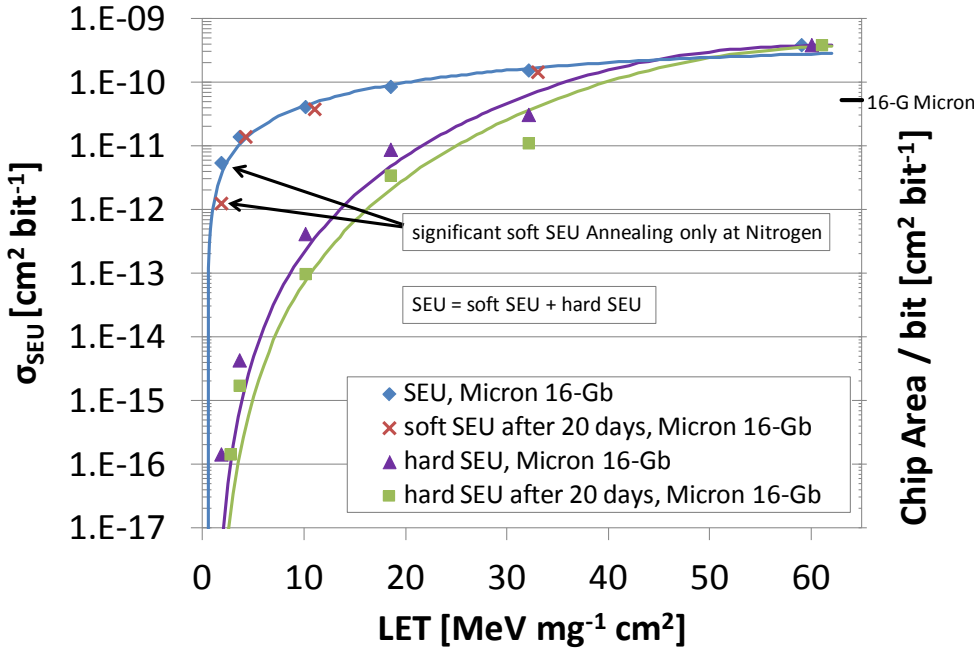
DDR3 results – Stuck bits

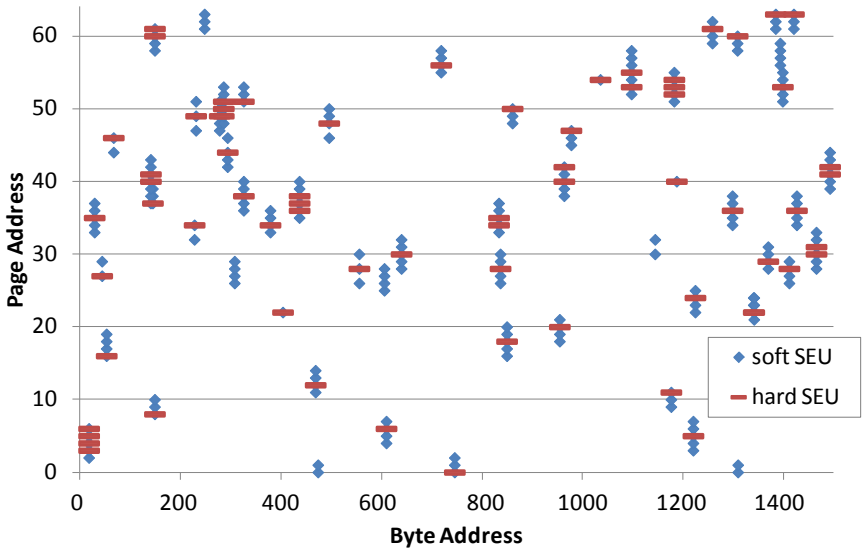
Stuck bits: can not be removed by rewriting

[M. Herrmann, IDA, ESA contract 2012-2014]

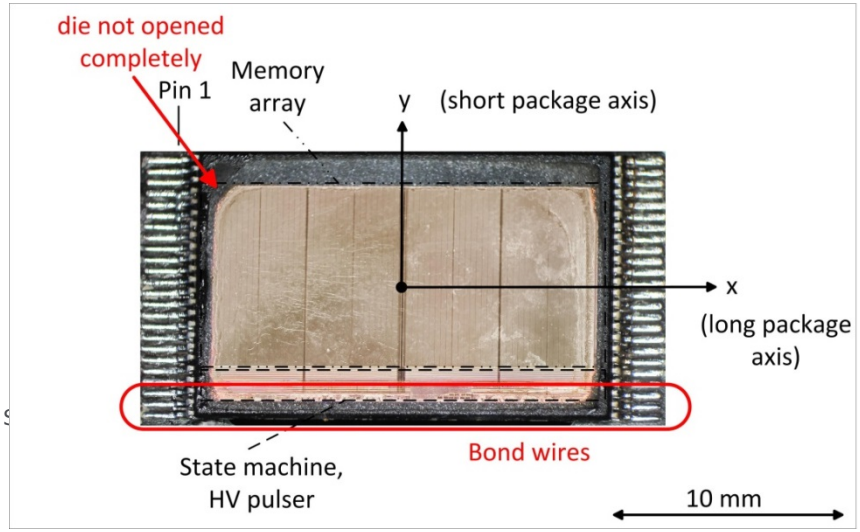


Stuck bits in NAND-flash

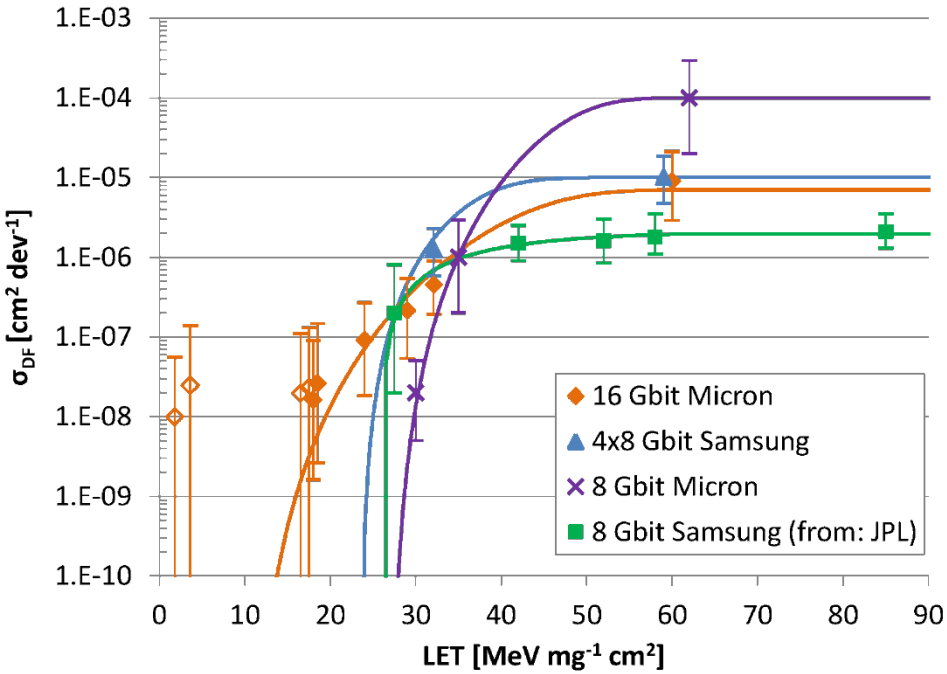




[K. Grürmann, IDA, ESA contract 2012-2014]

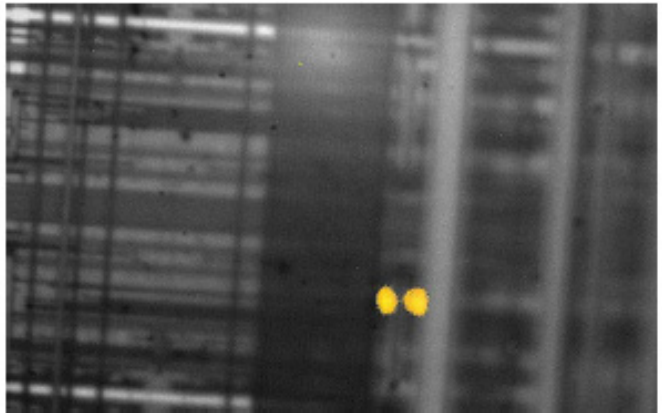


Destructive events in NAND-Flash



[K. Grürmann, IDA, ESA contract 2012-2014]

Samsung 8Gb NAND-Flash

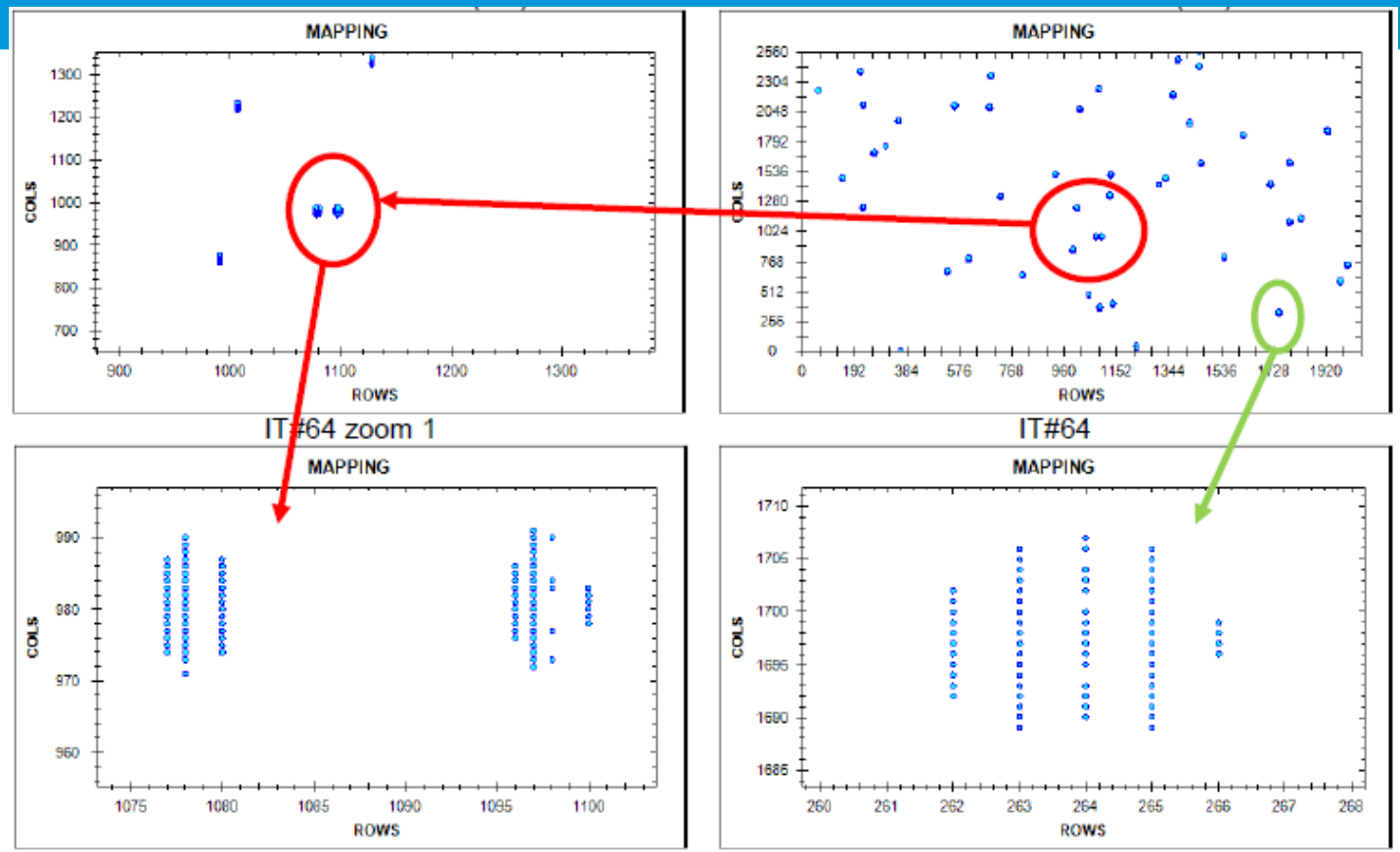


Thermal picture charge pump region

[F. Irom, TNS Feb. 2010]

- Permanent damage with definite data loss
- 16 Gbit Micron shows also other DF types affecting the on-chip microcontroller

Multiple Cell Upset in SRAMs



IT#64 zoom 1

IT#64

IT#64 zoom 2 (2 MCUs)

IT#64 zoom3 Other MCU example

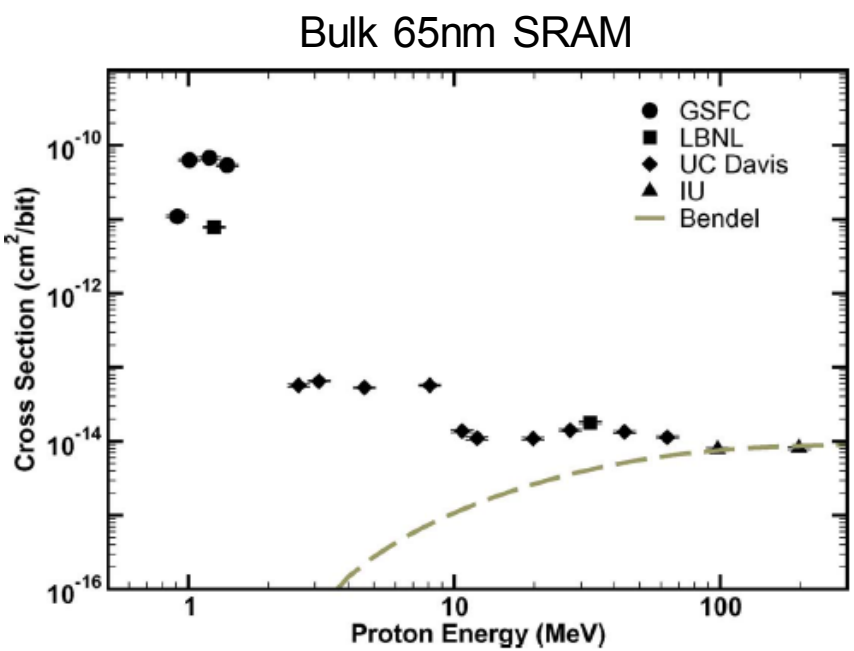
40nm SRAM
Tilt=0, Roll=90,
Xenon, UCL

[ESTEC contract 18799/04/NL/AG
Hirex SEE test report, HRX/SEE/0288
STMicroelectronics 40nm SRAM test vehicle]

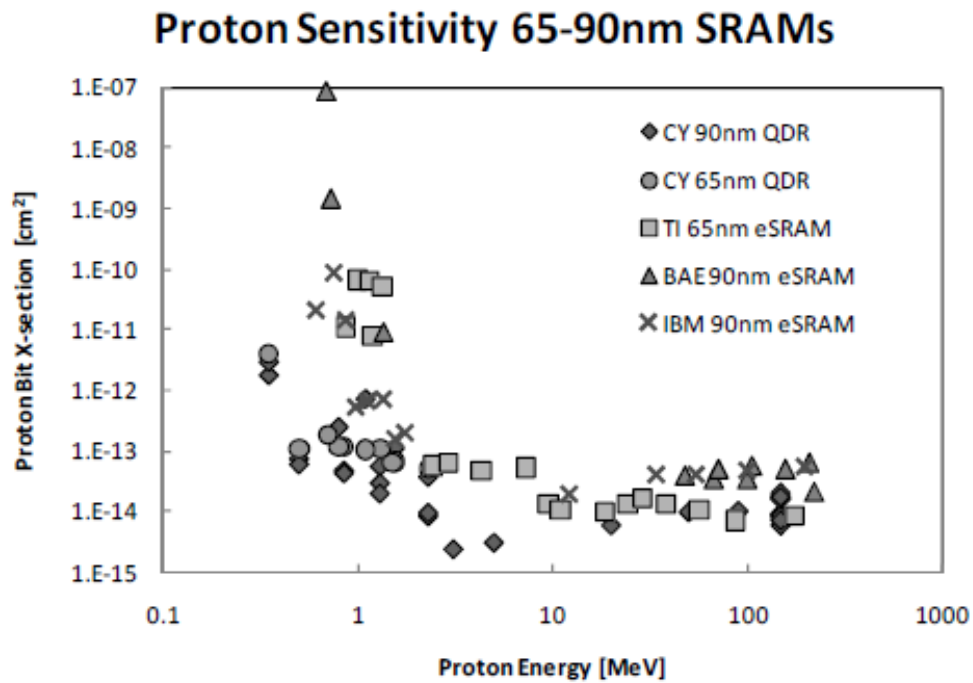
One ion strike can induce more than 100 cell upsets

SEU sensitivity for low energy proton in SRAM from 90nm and beyond

Devices with very low LET thresholds are sensitive to proton-induced upset by **direct ionization**.

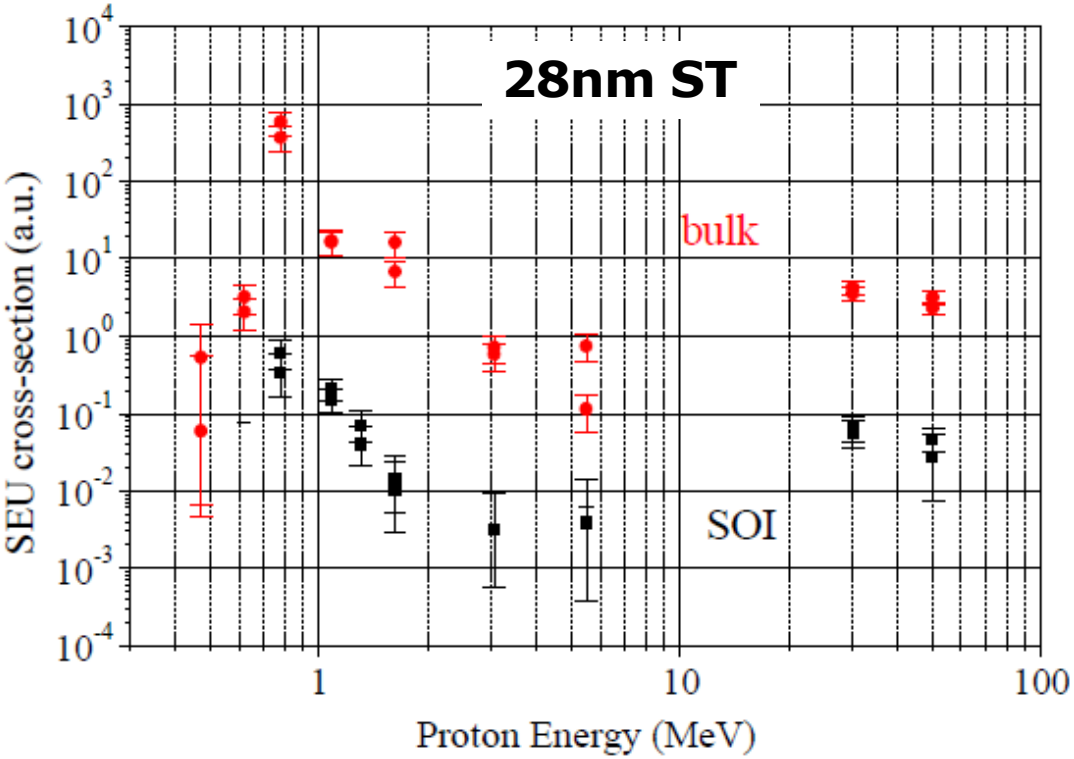


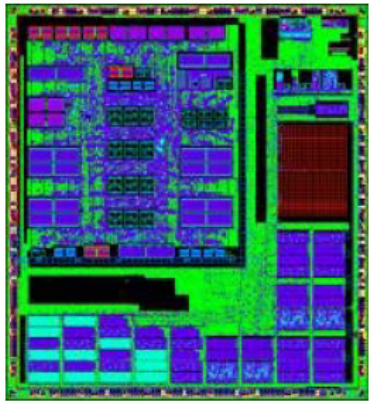
[B. Sierawski, TNS 2009]

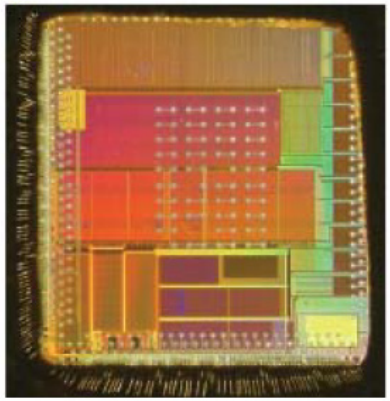


[H. Puchner, REDW 2011]

Low energy protons sensitivity in 28nm SRAMs STMicroelectronics







Low energy protons

High energy beam

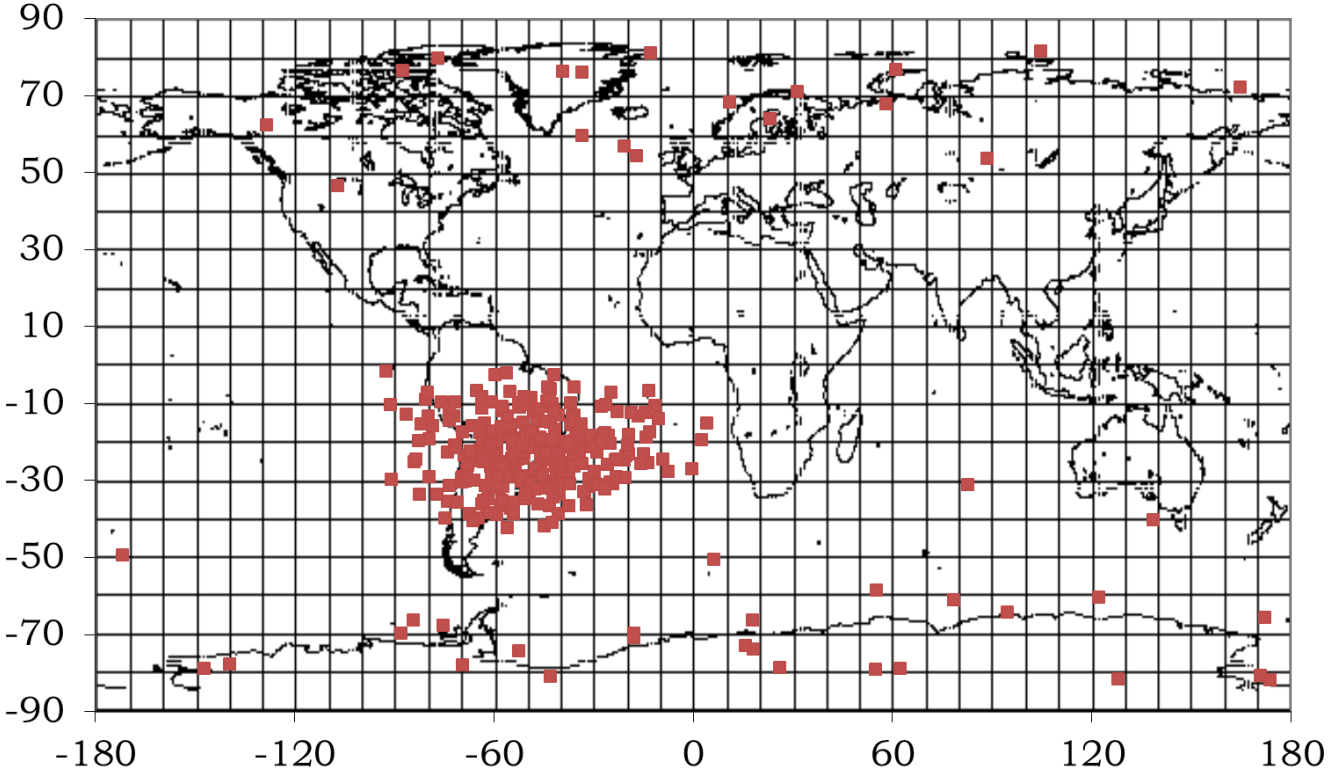
Method needed to calculate the SEE rate due to low energy protons in space

[H. Kettunen, et. al. IEEE REDW 2014]
ESA contract

In-flight example SRAM Aboard Proba-2

GPS receiver: latch-up events in 512kx8 SRAM Samsung K6R4016V1D-TC10

The GPS counts two redundant receiver units and a current limiter; in cold redundancy logic



Proba-2: polar LEO

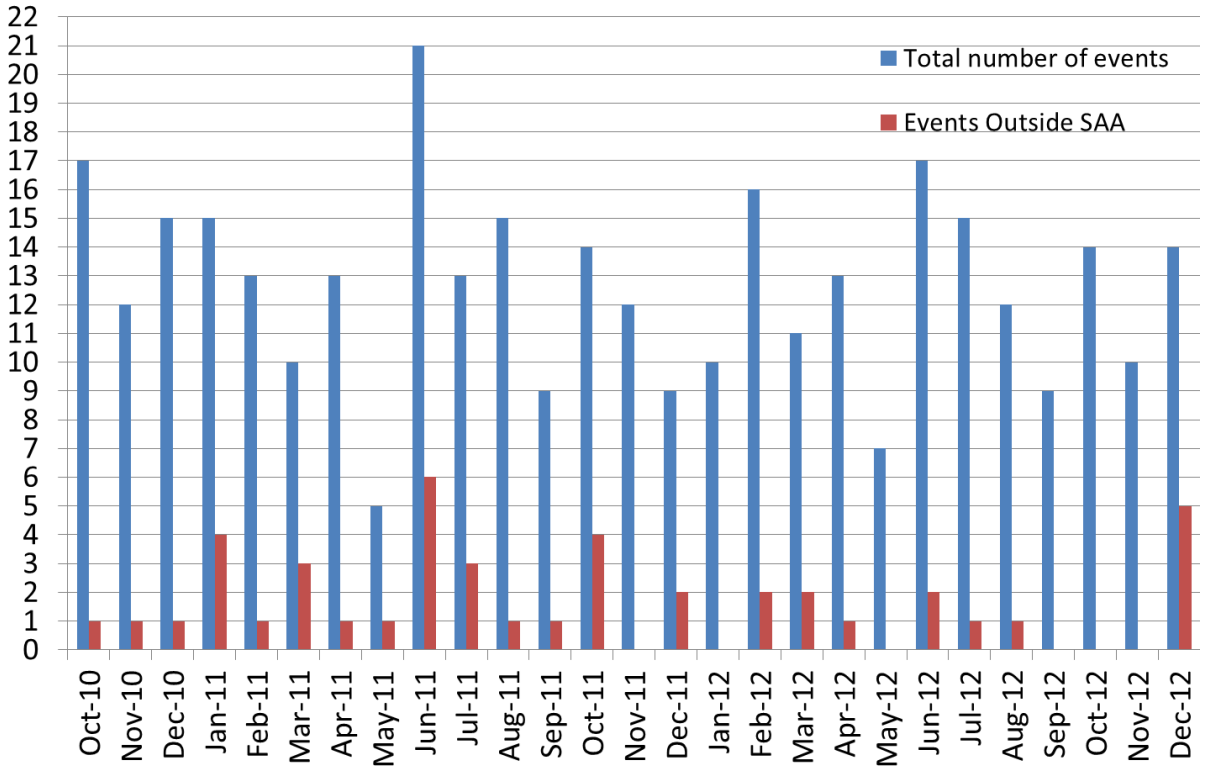
Samsung K6R4016V1D-TC10 DC 220 TANO6EE KOREA

The devices were unsufficiently tested before flight

[M. D'Alessio, et al. ESA at RADECS 2013]

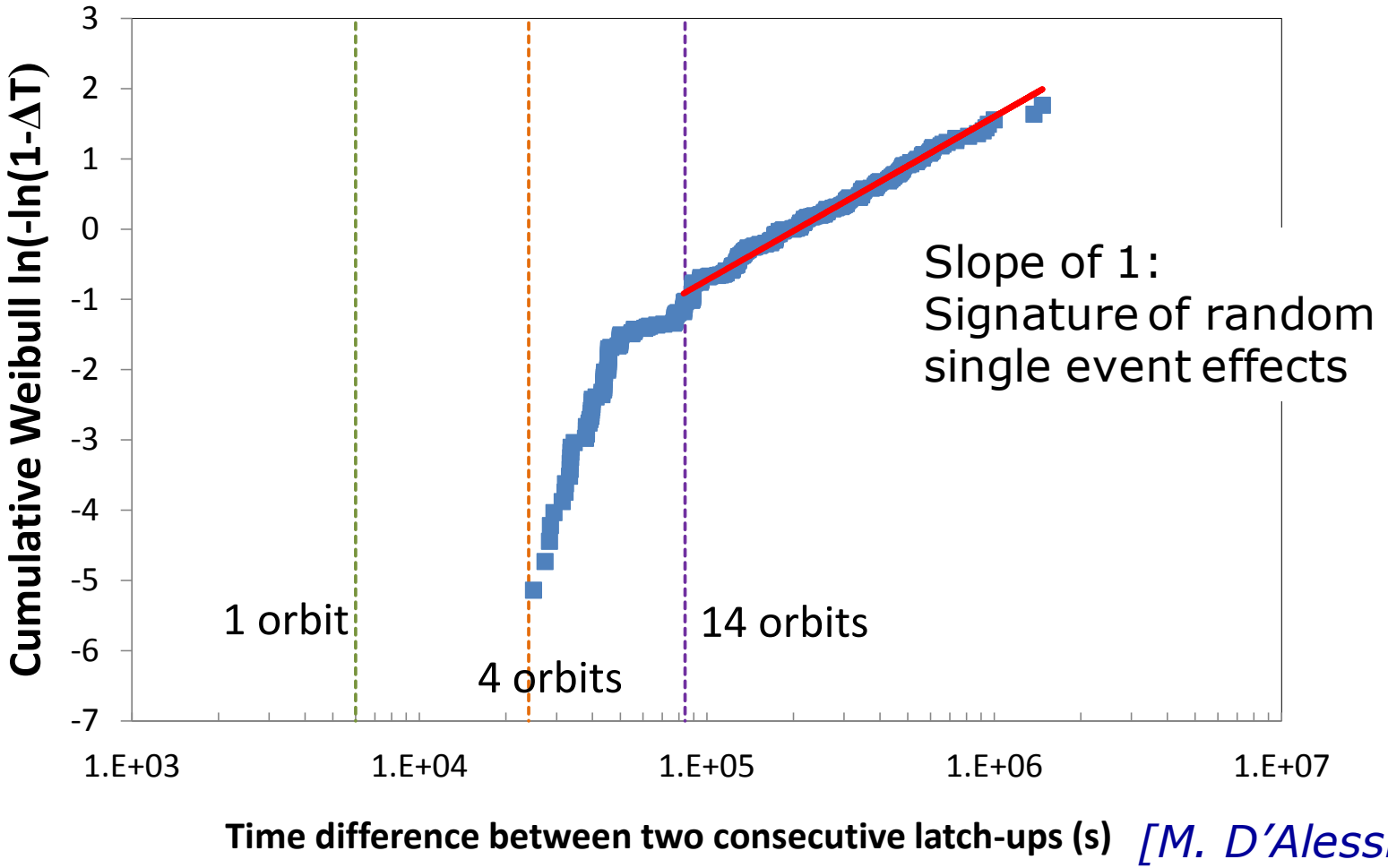
Statistical analysis of the GPS latch-up events from Oct-10 to Dec-12

- Average upset rate of 12 SELs/month (0.4 SEL/day)
- Large variability, from 6 to 27 SELs/months
- 87% SELs are in the SAA



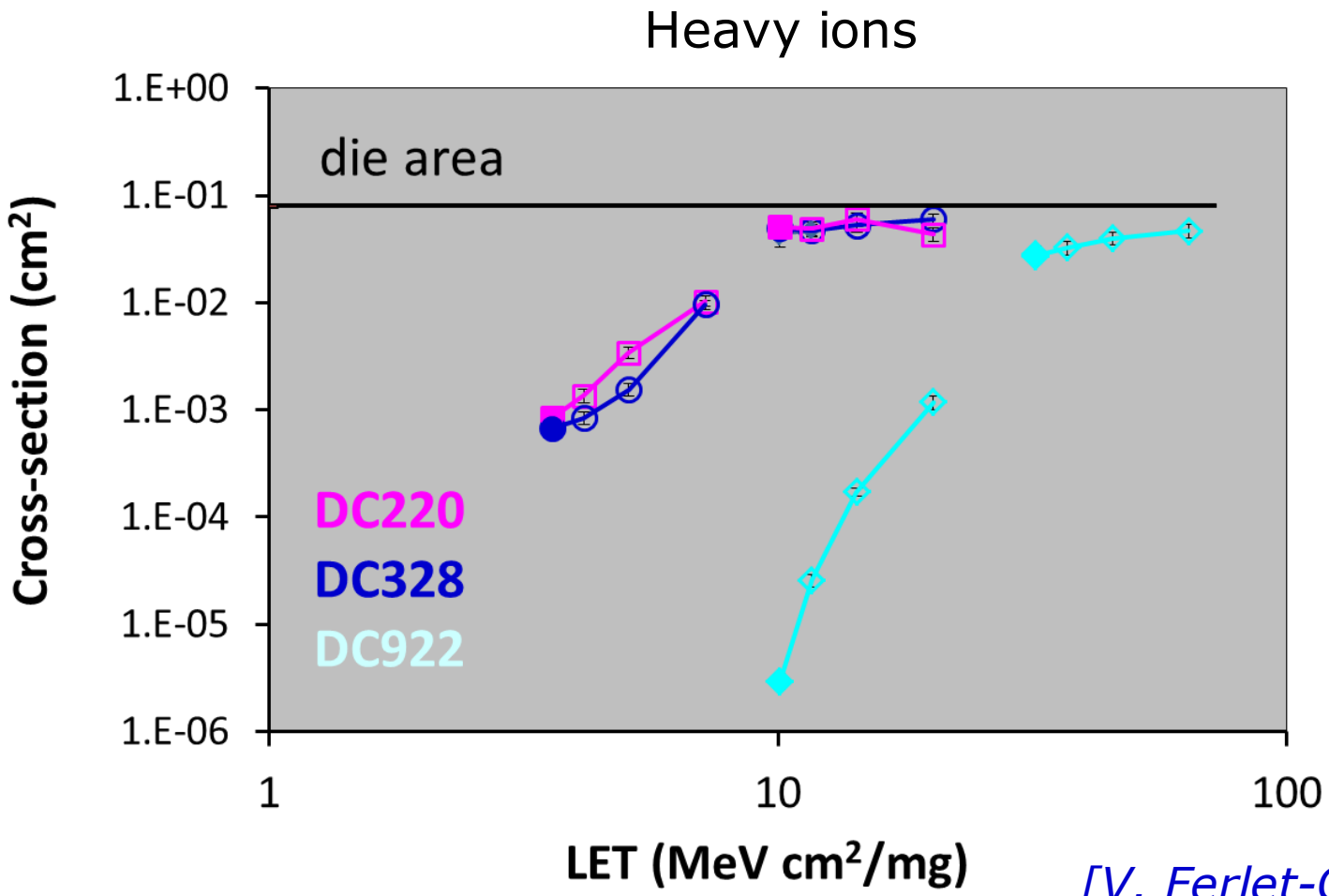
[M. D'Alessio, et al. ESA at RADECS 2013]

Statistical analysis of the GPS latch-up events (cont.)



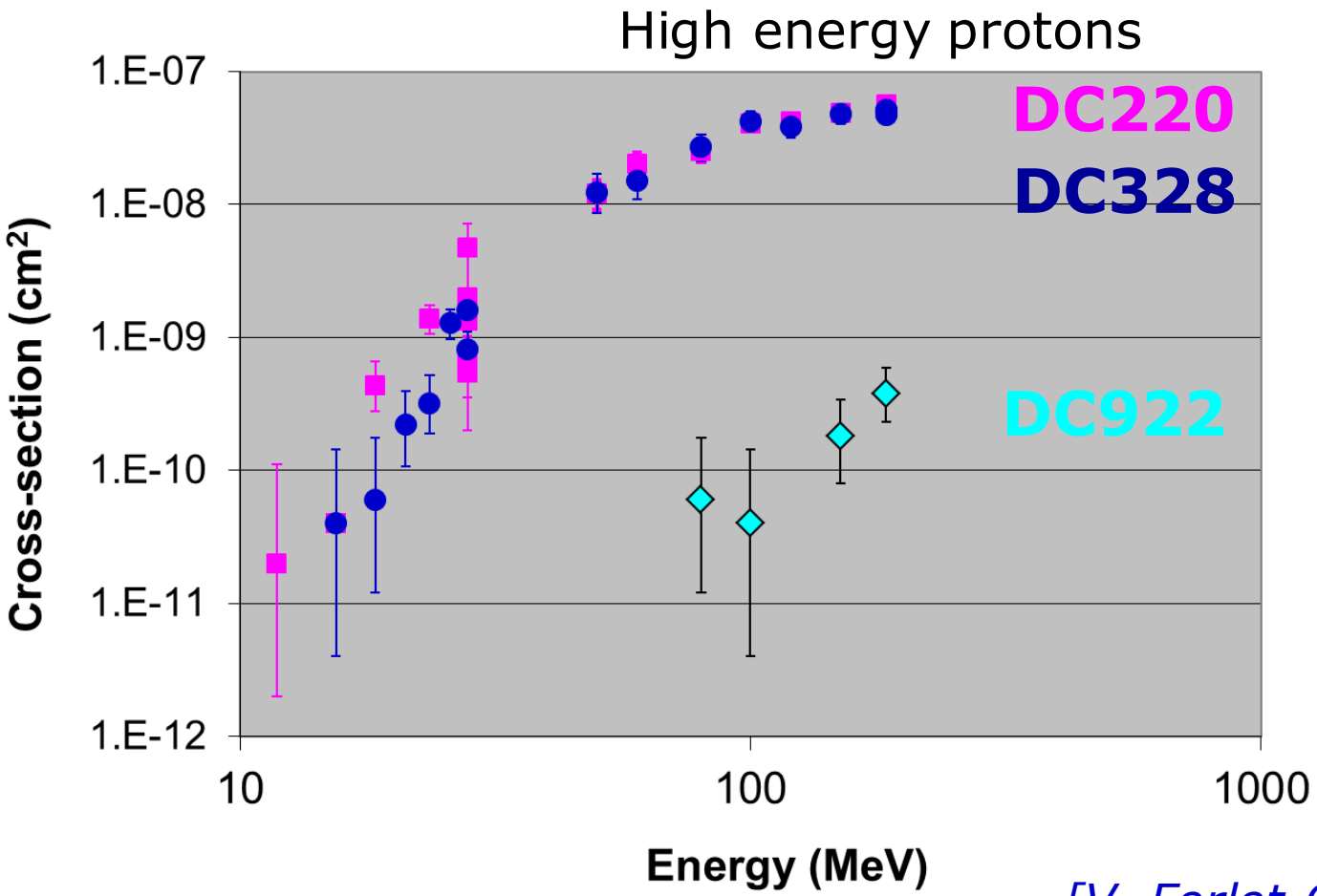
[M. D'Alessio, et al. ESA at RADECS 2013]

The ground tests of the Samsung K6R4016V1D-TC10 shows large differences vs. Date Code – Heavy ion test



[V. Ferlet-Cavrois, ESA test report 2012]

The ground tests of the Samsung K6R4016V1D-TC10 shows large differences vs. Date Code – Proton test



[V. Ferlet-Cavrois, ESA test report 2012]

Conclusion

- Test the flight lots
- Test in the application conditions
- Test to the environment specifications

Test standards:
ESCC22900 TID
ESCC25100 SEE

RHA
ECSS-Q-ST-15C

Find information in: www.escies.org