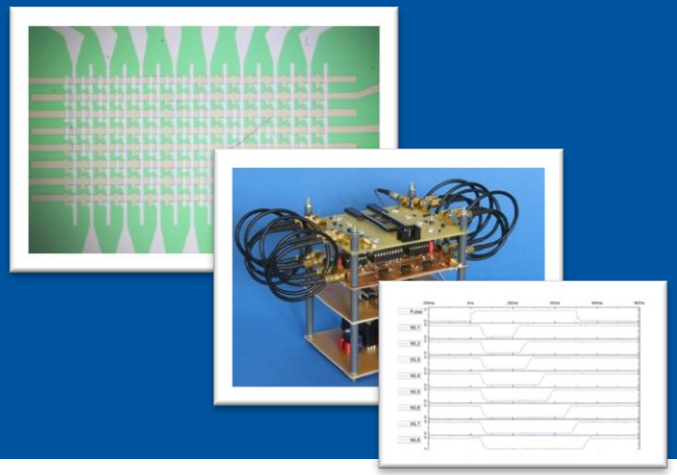


Complementary Resistive Switch based Neuromorphic Associative Capacitive Network

L. Nielen [1,2], A. Siemon [1,2], S. Tappertzhofen [1,2,3], R. Waser [1,2,4], S. Menzel [2,4], E. Linn [1,2]

[1] Institut für Werkstoffe der Elektrotechnik II, RWTH Aachen University, Germany

[2] JARA – Fundamentals of Future Information Technology

[3] Department of Engineering, University of Cambridge, United Kingdom

[4] Peter Grünberg Institut 7, Forschungszentrum Jülich GmbH, Jülich, Germany

21.01.2015

IWE2 Institut für Werkstoffe der Elektrotechnik 2 | RWTH AACHEN UNIVERSITY

Outline

- Associative Capacitive Networks

  a Neuronal application for non-volatile memories

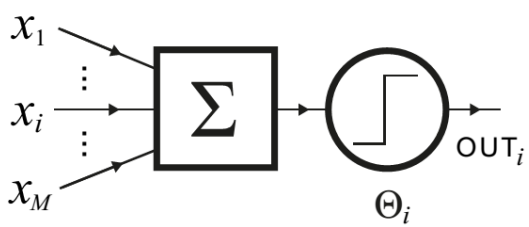
- Complementary Resistive Switches (CRS)

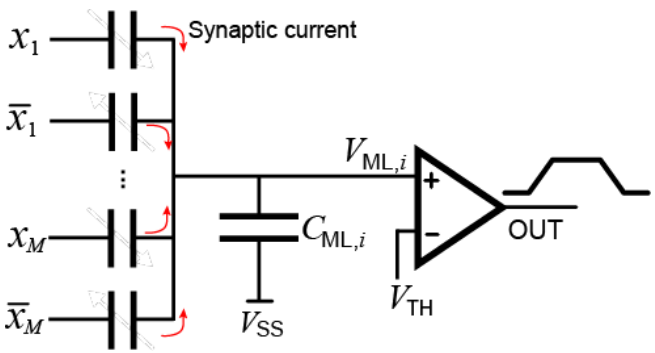
  a solution of the sneak path problem in passive ReRAM arrays

- Capacitive Readout of CRS cells
- CRS-based Associative Capacitive Network (ACN)
- Experimental ACN circuitry
- Simulative evaluation
- Summary

Associative Capacitive Network - Motivation

Artificial neuron model





O. Kavehei, E. Linn et al., *Nanoscale*, 5, 5119 (2013)

- Information stored via capacitance value
- Simultaneous activation function on all lines
- Summarized output

→ Content Addressable Memory

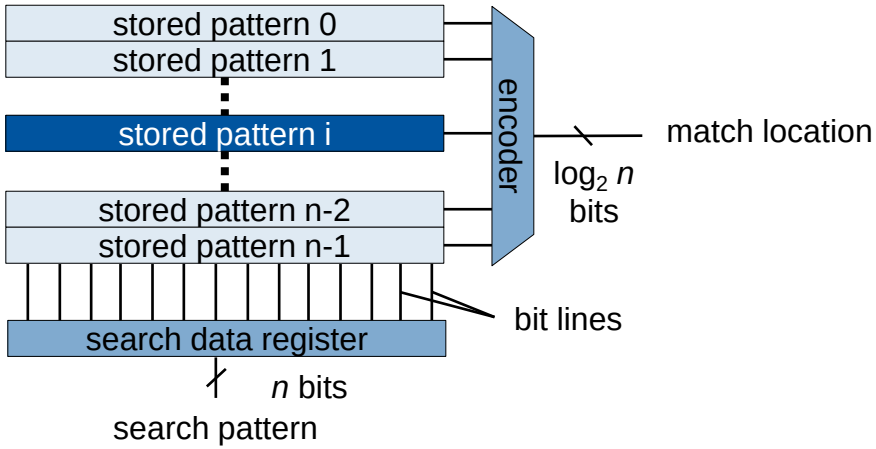
Problem with conventional ACNs:
Capacitances charge is volatile

CRS based solution:
non-volatile memory

Applications area:
- Pattern recognition
- Fast routing (reprogrammable lookup-tables)

Content Addressable Memories (CAM)

- Rewritable memory with lookup-table functionality
- Pattern matching in a single cycle

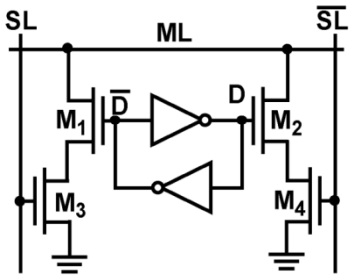


- Conventional CAMs are implemented by SRAM core cells

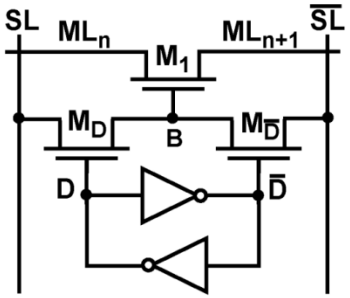
→ drawbacks:

  - static currents → high energy consumption
  - large area demand

Classical SRAM based CAM cell



10-T NOR-type CAM

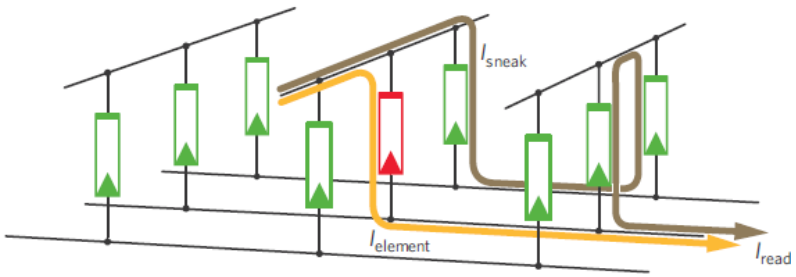


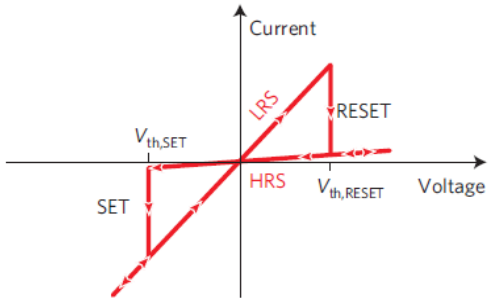
9-T NAND-type CAM

K. Pagiamtzis; A. Sheikholeslami, *IEEE J. Solid-State Circuits, 41*, p. 712 (2006)

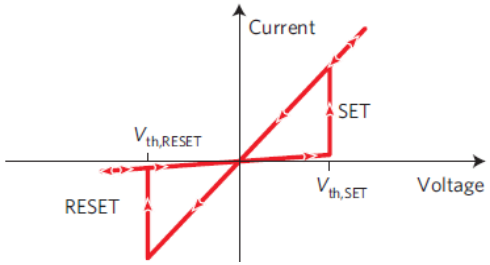
Complementary Resistive Switches (CRS)

Overcoming the Sneak Path Obstacle in passive resistive arrays





Element A



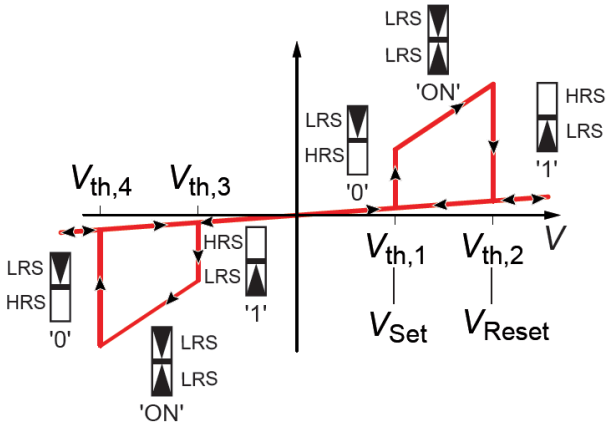
Element B

CRS

Two anti-serially connected elements

- Overall high cell resistance
- No pattern dependency
- Low static power losses

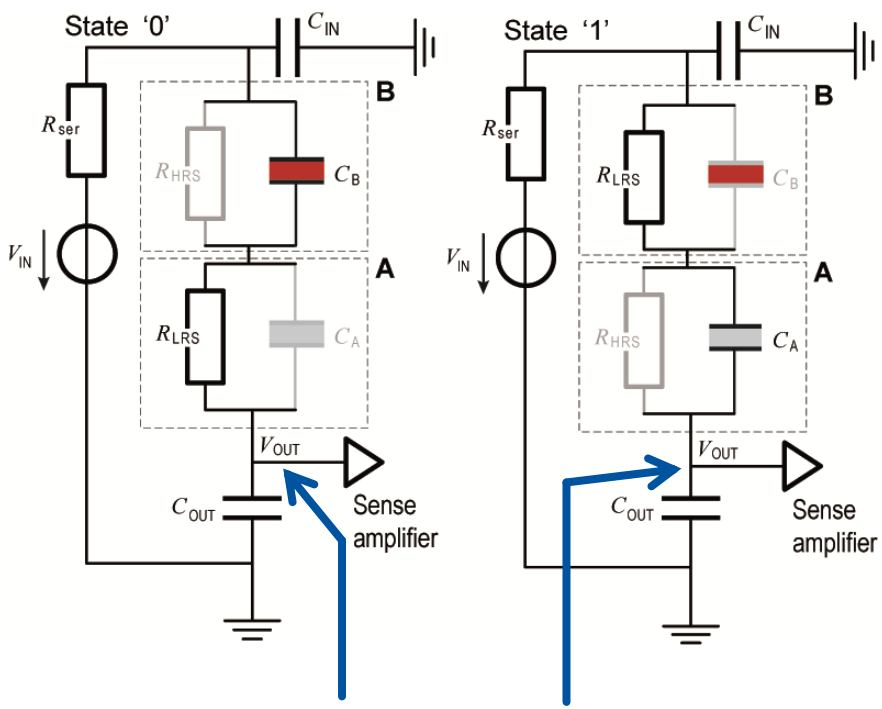
→ No sneak paths



CRS state	Element A	Element B	resistance CRS
0	LRS	HRS	≈ HRS
1	HRS	LRS	≈ HRS
ON	LRS	LRS	LRS+LRS
OFF	HRS	HRS	>> HRS

E. Linn, R. Rosezin et al., *Nat. Mater.*, 9, p. 403 (2010)

Capacitive Read-out

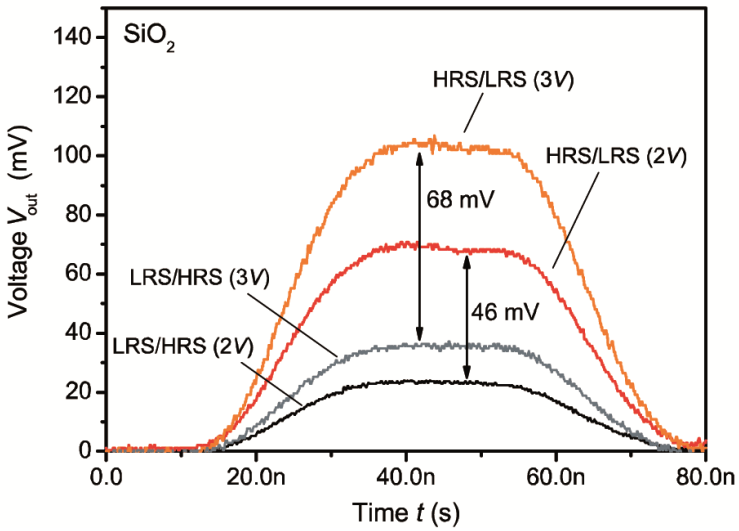


Capacitive voltage divider

NDRO

CRS cells offer a capacitive voltage divider property

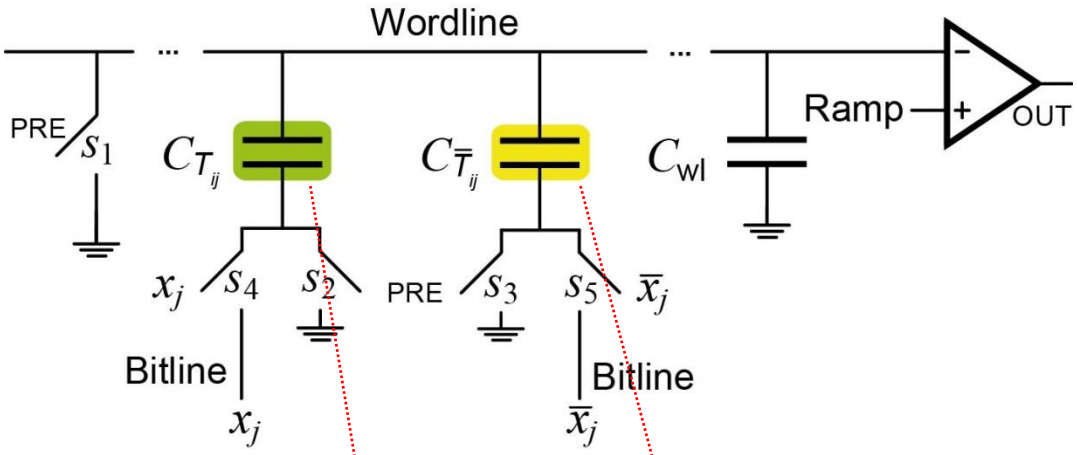
- Both elements A and B are equal in terms of resistive switching
- But: capacitances differ (e.g. different areas)
- Capacitive read-out of the stored state



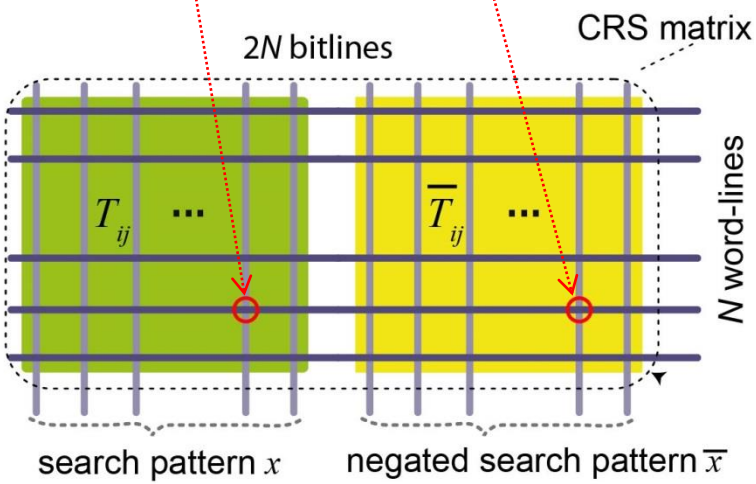
S. Tappertzhofen, E. Linn et al., *Nanotechnology*, 22, p. 395203 (2011)

CRS-based Associative Capacitive Network

Single ACN cell



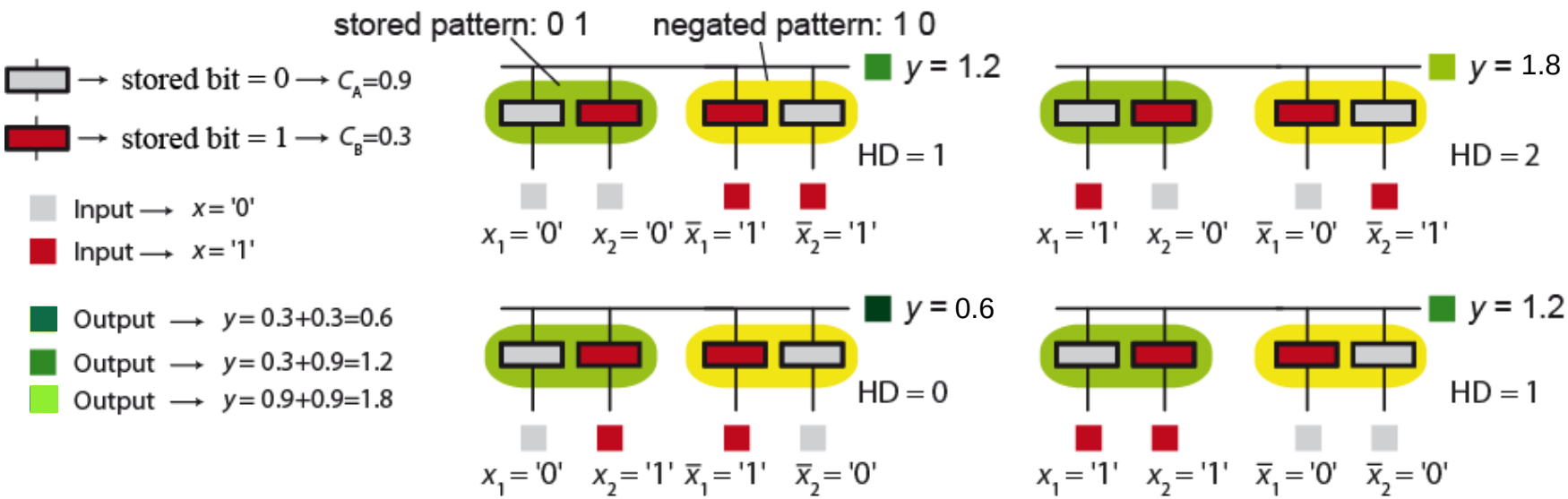
***N*×2*N*-ACN array**



O. Kavehei, E. Linn et al., *Nanoscale*, 5, 5119 (2013)

ACN – 2-bit Example

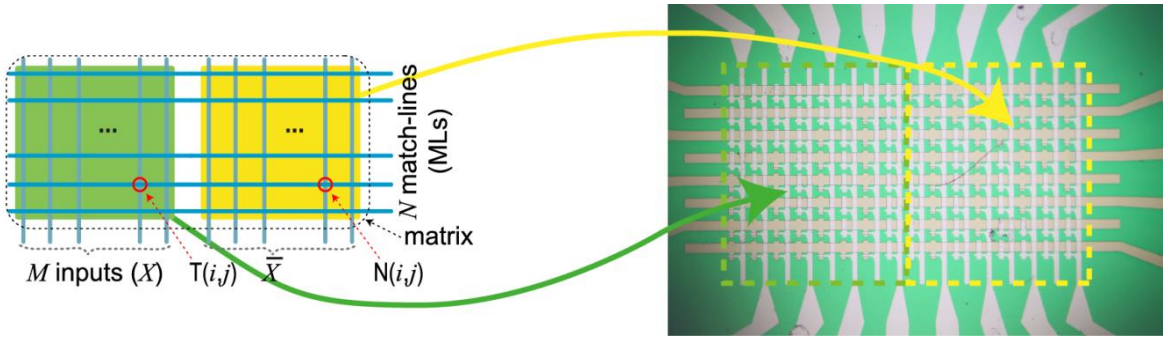
Stored pattern: 0 1 and negated pattern 1 0
HD=2: maximum output (x_1= ‘1’ x_2= ‘0’) [mismatch]
HD=1: equal output for x_1= ‘0’ x_2= ‘0’ and x_1= ‘1’ x_2= ‘1’ [50 % match]
HD=0: minimum output (x_1= ‘0’ x_2= ‘1’) [match]



Output voltage reflects Hamming Distance (HD)
→ Pattern matching

O. Kavehei, E. Linn et al., *Nanoscale*, 5, 5119 (2013)

Fabrication of ACN Cells



Fabrication of a µ-structure array

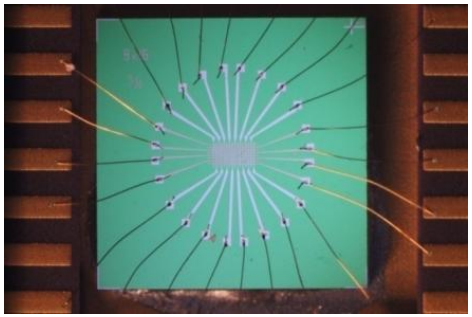
- Silicon wafer
- Platinum, Titanium and TiO_2 sputter deposition
- UV-lithography

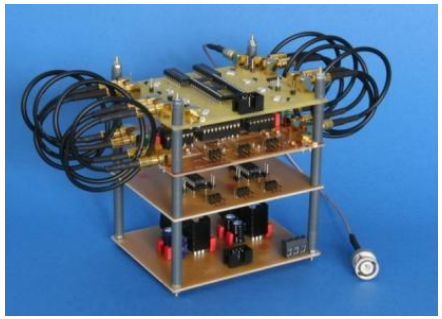
Cell A: 24×10 µm²

Cell B: 20×20 µm²

Associative Capacitive Network

- $N \times 2M$ array of CRS devices
- green: stored template (T)
- yellow: stored negates of T ($\underline{T}$)
- input: vector X and $\underline{X}$



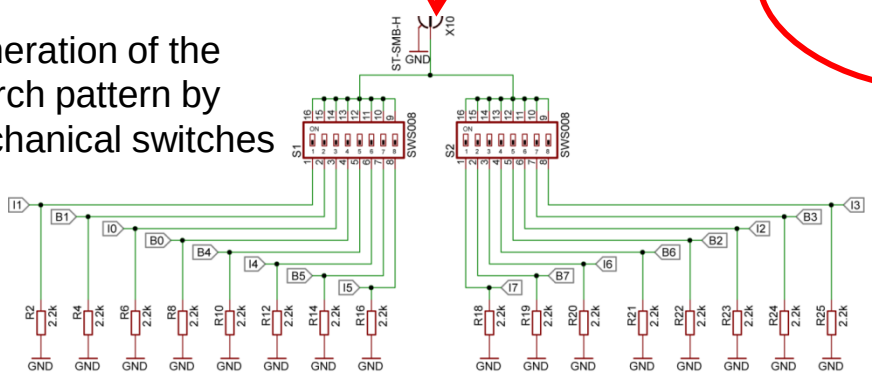


- Die mounting in a 28 pin carrier
- Contacting via wedge-wedge bonding with gold wires
- Evaluation with an experimental circuitry

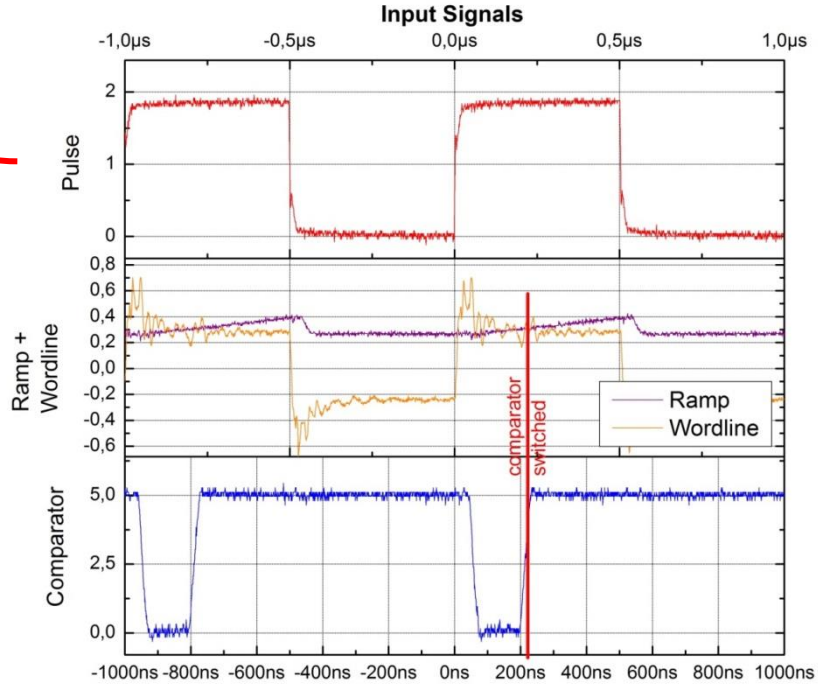
Experimental Setup for ACN Read-Out

Appling the search pattern

Generation of the search pattern by mechanical switches

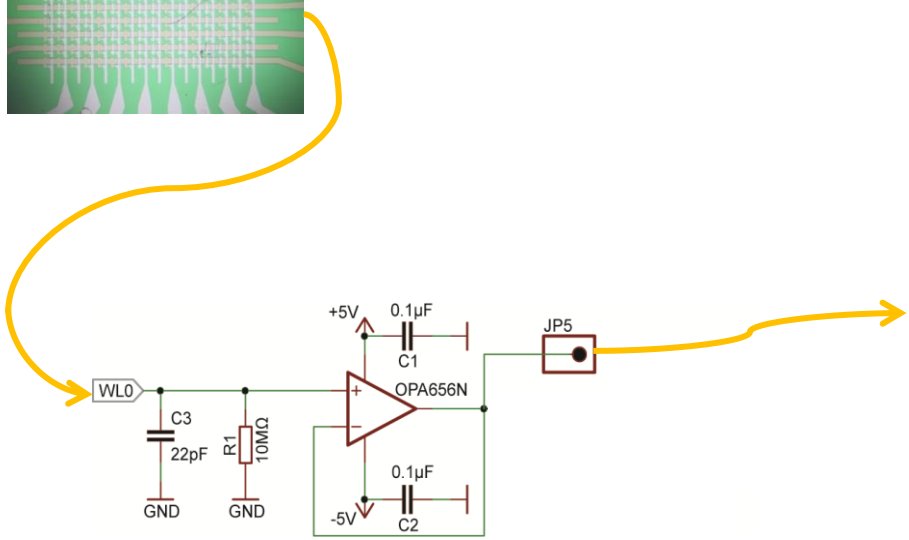


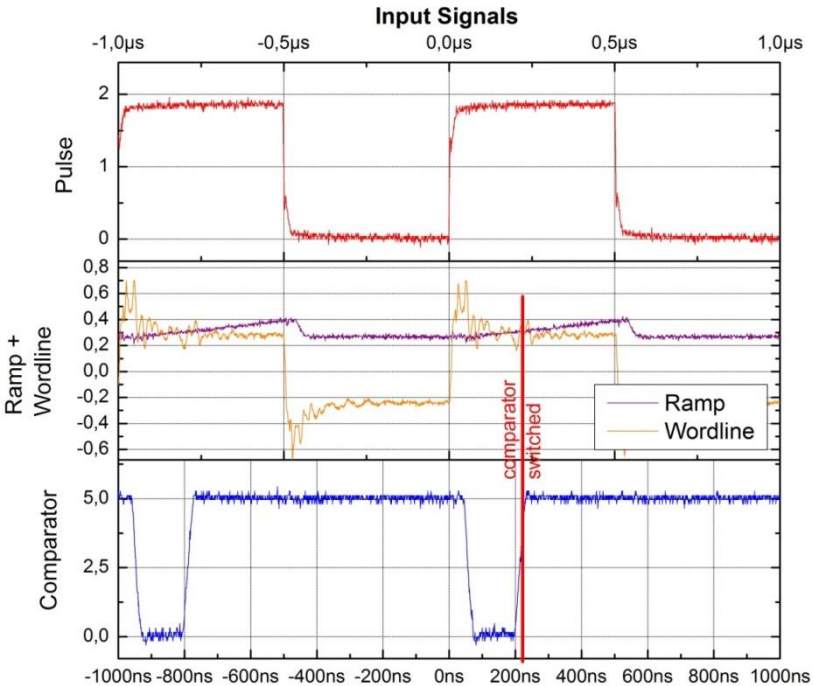
all bit lines



L. Nielen; S. Tappertzhofen et al., IEEE SNW, p. 61 (2014)

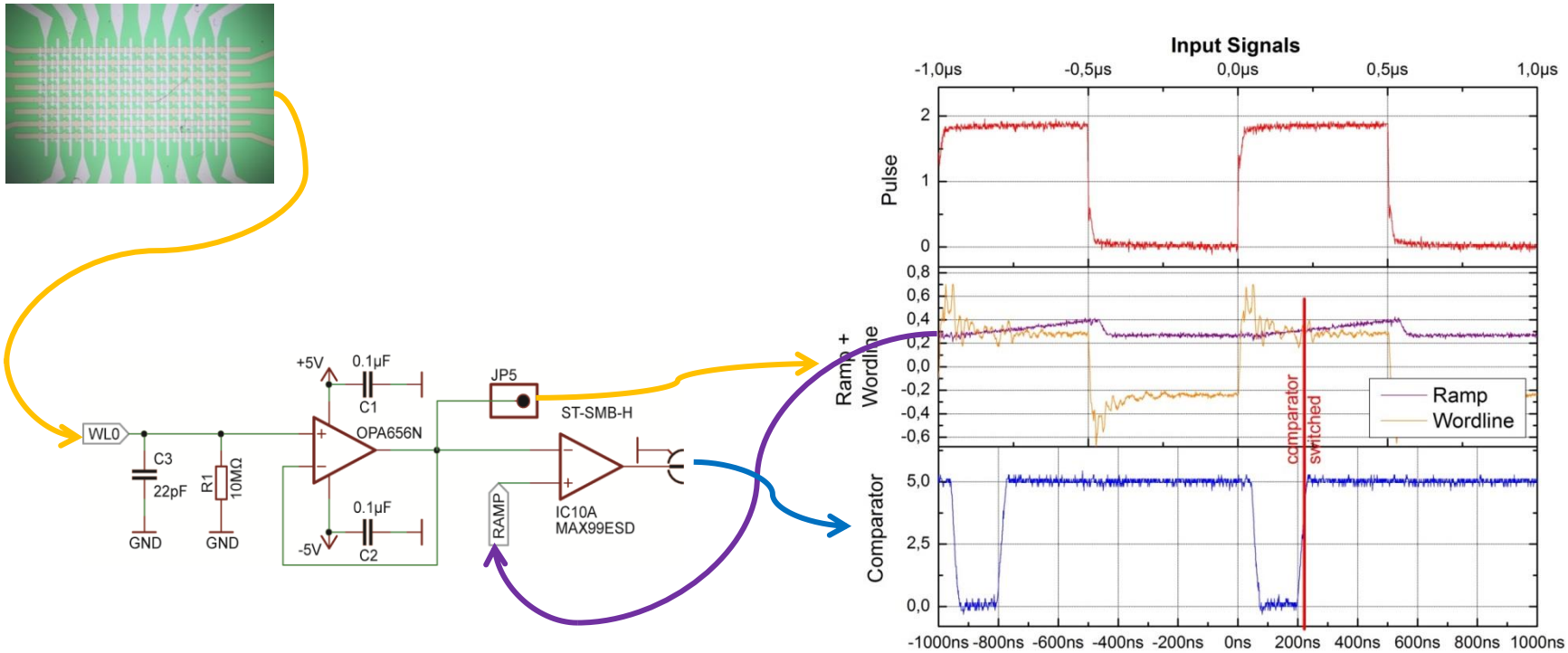
Experimental Setup for ACN Read-Out





Impedance conversion on each word line

Experimental Setup for ACN Read-Out



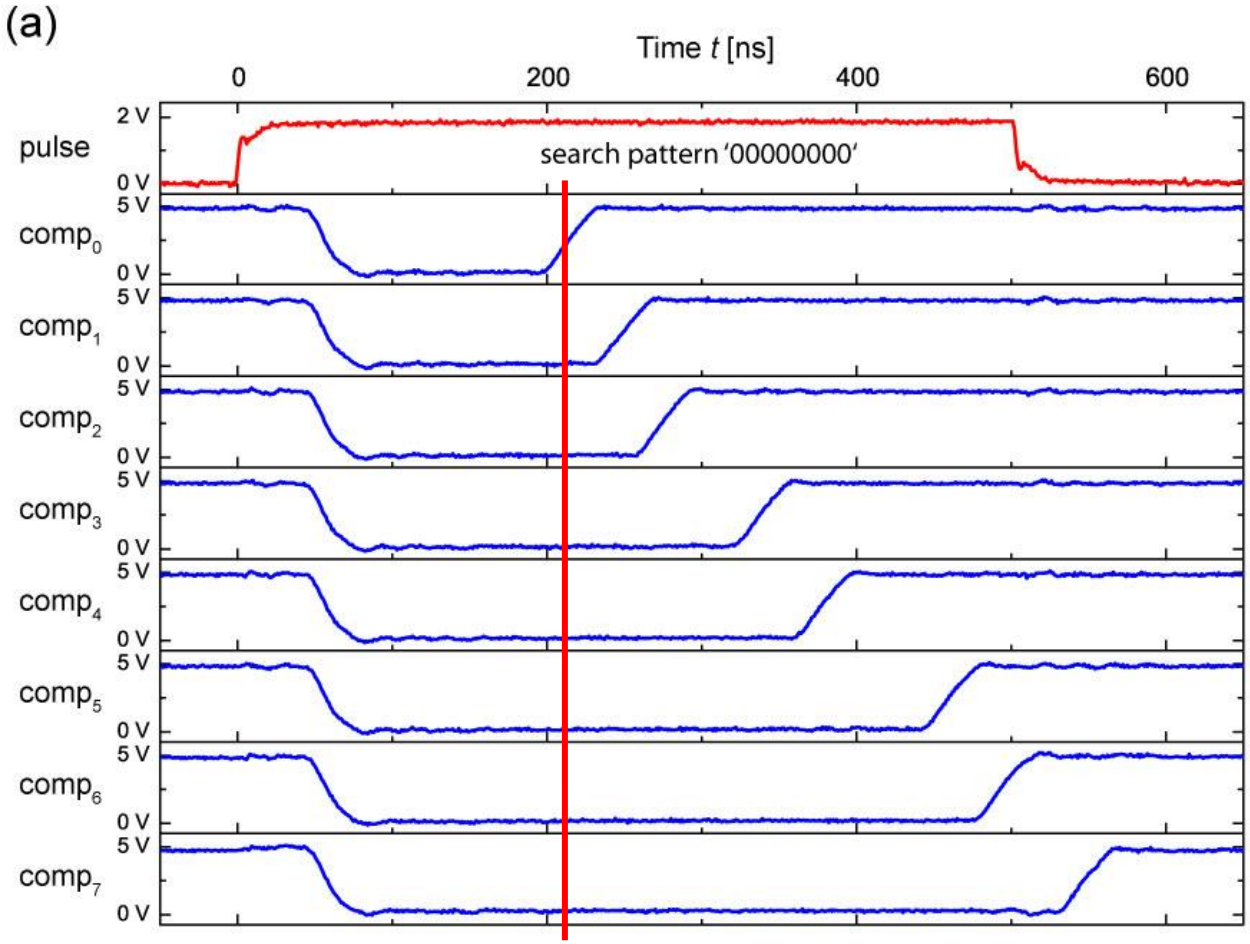
Voltage-to-time conversion

→ HD detection via switching event

Experimental Results

Stored patterns:

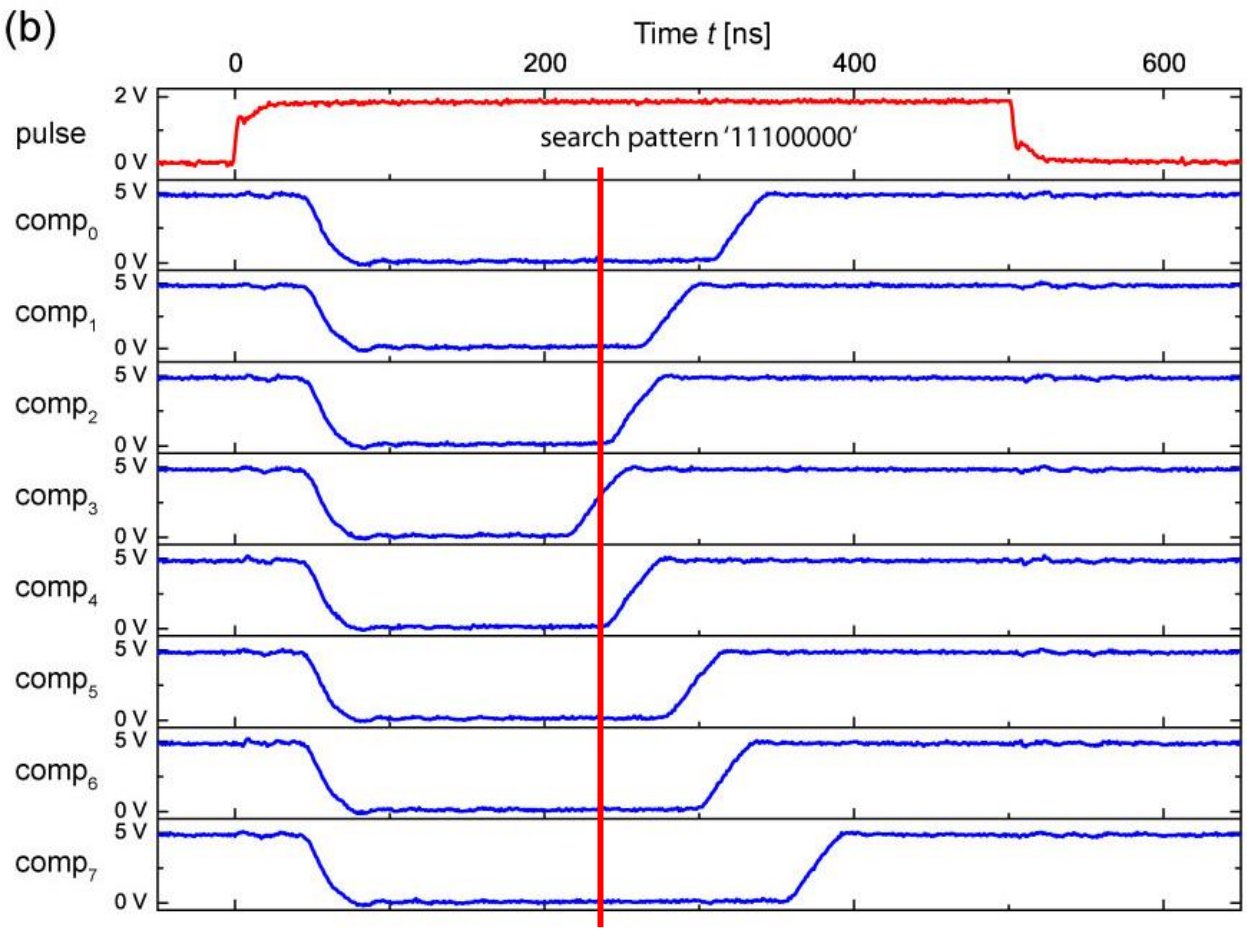
	A	B	C	D	E	F	G	H
A	0	0	0	0	0	0	0	0
B	1	0	0	0	0	0	0	0
C	1	1	0	0	0	0	0	0
D	1	1	1	0	0	0	0	0
E	1	1	1	1	0	0	0	0
F	1	1	1	1	1	0	0	0
G	1	1	1	1	1	1	0	0
H	1	1	1	1	1	1	1	0



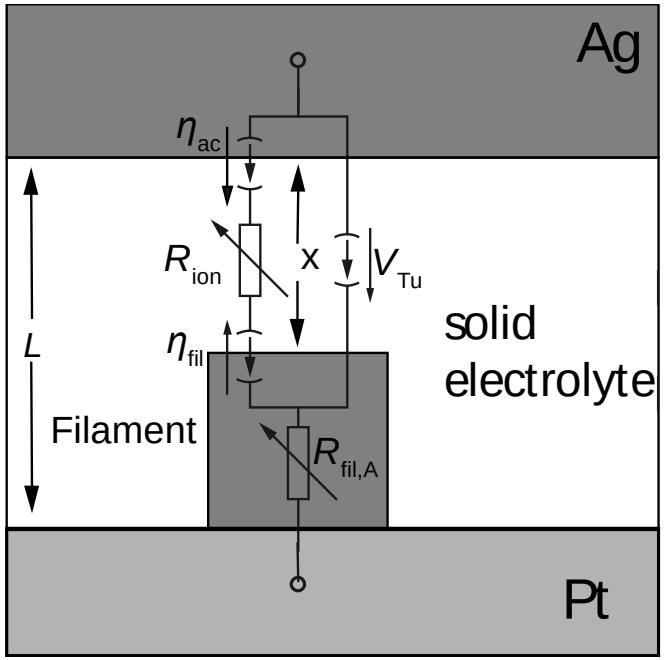
Experimental Results

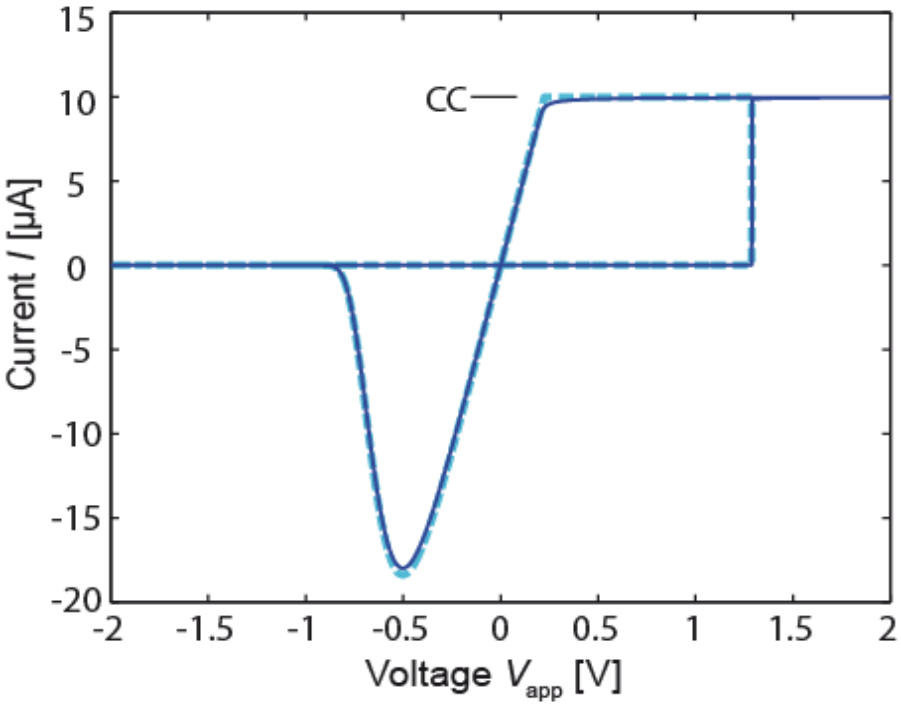
Stored patterns:

	A	B	C	D	E	F	G	H
A	0	0	0	0	0	0	0	0
B	1	0	0	0	0	0	0	0
C	1	1	0	0	0	0	0	0
D	1	1	1	0	0	0	0	0
E	1	1	1	1	0	0	0	0
F	1	1	1	1	1	0	0	0
G	1	1	1	1	1	1	0	0
H	1	1	1	1	1	1	1	0



Memristive ECM model



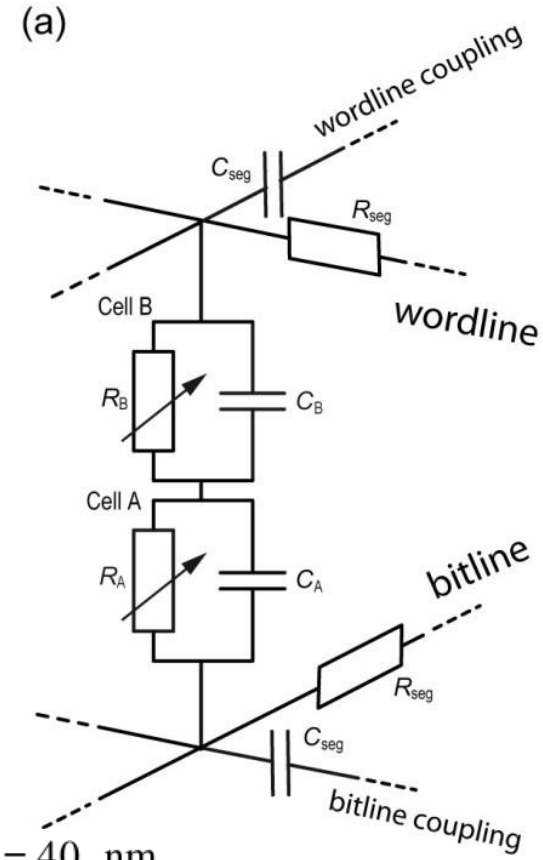


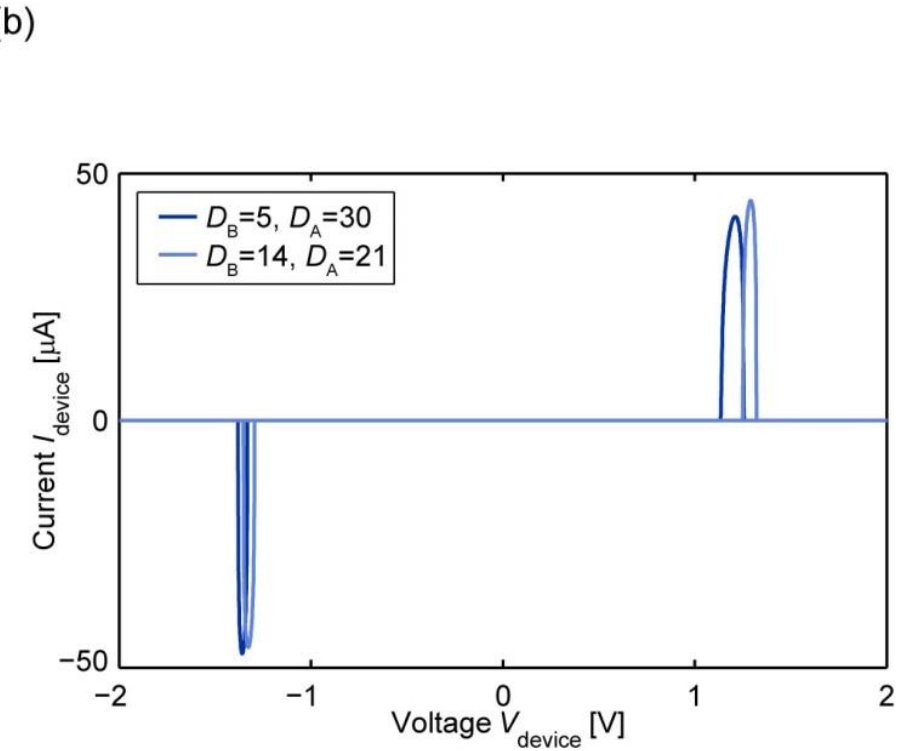
$$I = I_{ion}(V, w) + I_{Tu}(V, w)$$

$$\dot{w} = C_1 \cdot I_{ion}$$

S. Menzel, U. Böttger, et al., *J. Appl. Phys.*, vol. 111, pp. 14501 (2012)
E. Linn, S. Menzel, et al., *Nanotechnology* **24**, 384008 (2013)

VerilogA core cell





$F = 40$ nm

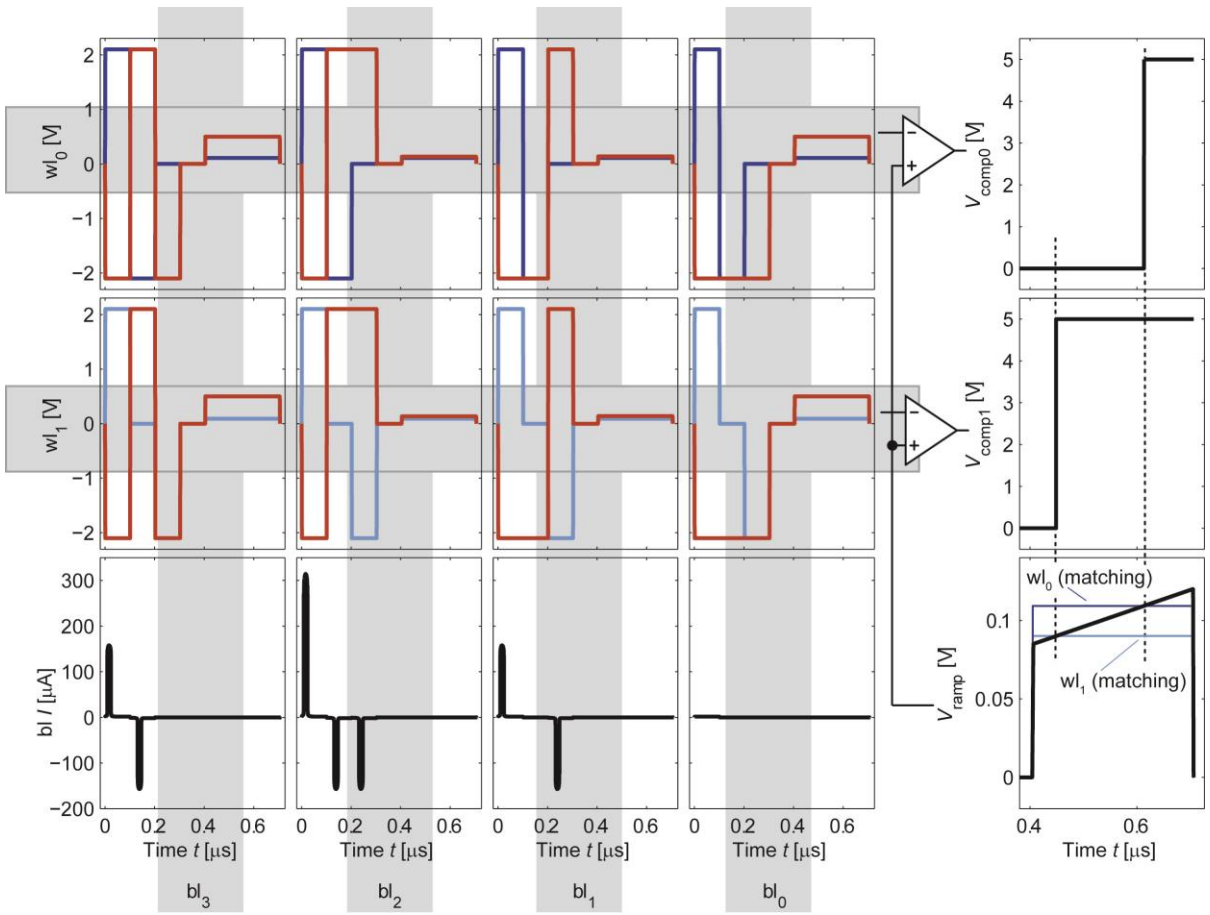
$C_{seg} = 2.76$ aF SiO_2 as interline material ($\varepsilon_r = 3.9$)

$R_{seg} = 0.86\ \Omega$

$D_A / D_B = 21$ nm / 14 nm = 1.5 ($C_A/C_B = 1/1.5$)
$D_A / D_B = 24$ nm / 12 nm = 2 ($C_A/C_B = 1/2$)
$D_A / D_B = 28$ nm / 7 nm = 4 ($C_A/C_B = 1/4$)
$D_A / D_B = 30$ nm / 5 nm = 6 ($C_A/C_B = 1/6$)

L. Nielen, A. Siemon et al., accepted *Jetcas*, (2015)

ACN Array Simulations



- Memristive ECM model implementation with VerilogA (SPICE)
- Array simulations performed by Cadence Spectre

Features

- Complete write and search operation feasible
- Implementation of coupling capacitances
- Different device capacitance ratios

L. Nielen, A. Siemon et al., accepted *Jetcas*, (2015)

Size Effects & Power Consumption

Minimum voltage margin *ΔV*

- Increasing array size (i.e. pattern length)

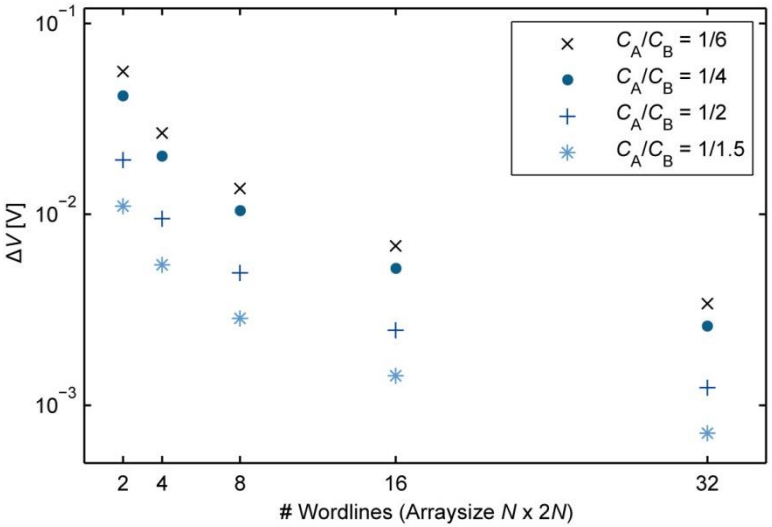
  → voltage interval corresponding to HD decreases

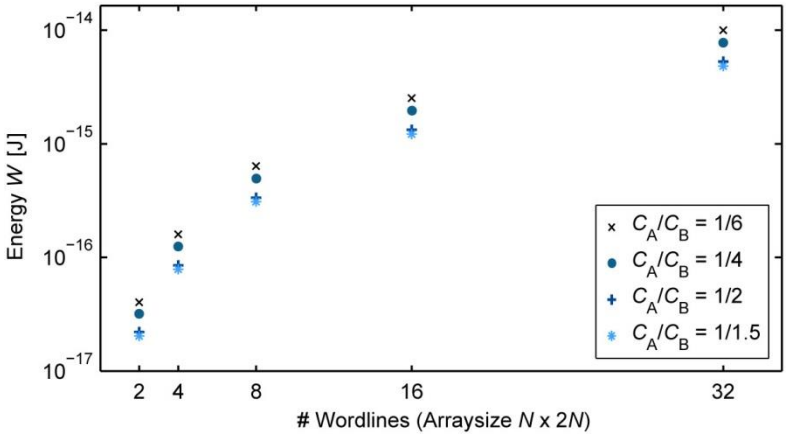
Search energy demand

Only caused by charging currents in:

- cells
- parasitic capacitances

→ Power consumption scales with array size





ACN (C_A/C_B = 1.5)		**SRAM-based**	
32×64		256…1024×144	
8 F^2	40nm	120–1500 F^2	32–65 nm
4.69 aJ/bit/search		> 0.1 fJ/bit/search	

P. T. Huang; W. Hwang, *IEEE J. Solid-State Circuits,* 46, p. 507, (2011)
A. T. Do, C. Yin et al, *IEEE J. Solid-State Circuits, 49*, p. 1487 (2014)

L. Nielen, A. Siemon et al., accepted *Jetcas*, (2015)

Summary

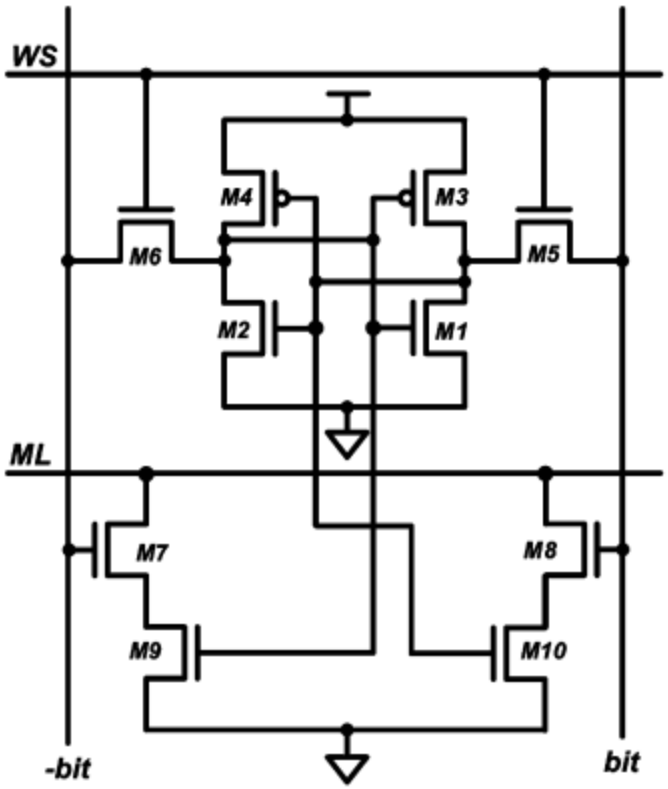
- **Neuromorphic** application for Memristive Random Access Memories was demonstrated
- An **Associative Capacitive Network** was fabricated
- Development of an **Experimental Setup** for ACN Evaluation
- **Proof-of-Concept:** The ACN shows the predicted behavior
- Study of arrays promises **Low Power Consumption**
- Fully parallel search within the range of **Nanoseconds** was demonstrated using a simple measurement setup

Advantages of CRS based ACN concept:

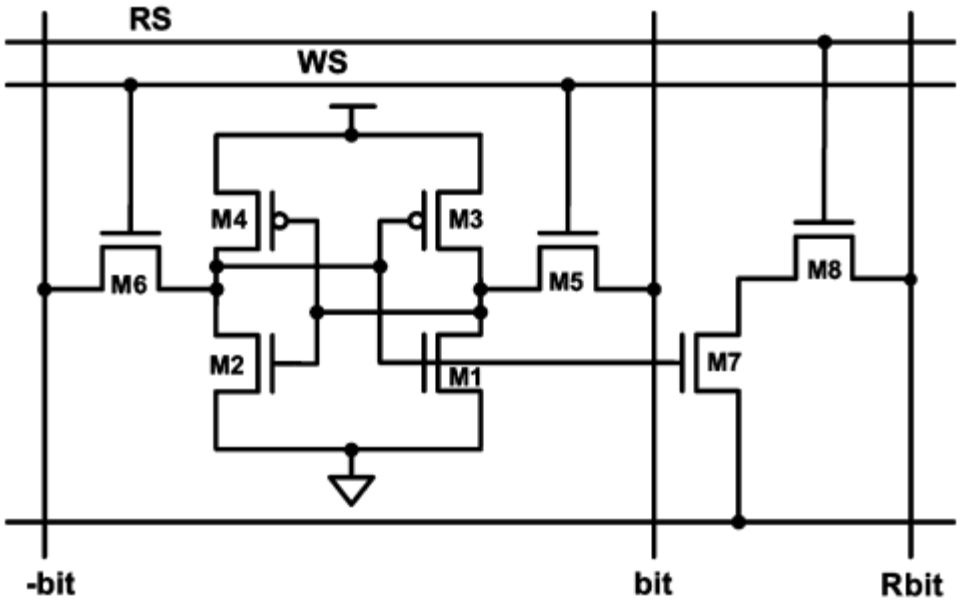
- Hamming Distance detection (similarity)
- Fully passive 2-CRS cell implementation – small area demand
- Non-volatile → No Refresh → Low Power Consumption
- No reprogramming → fast read access
- No requirement of constant voltage supply

THANK YOU
FOR YOUR ATTENTION

Content Addressable Memories (CAM)



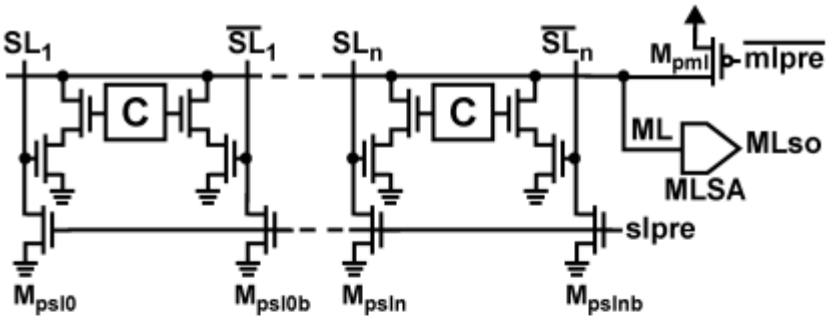
10-T NOR-type CAM



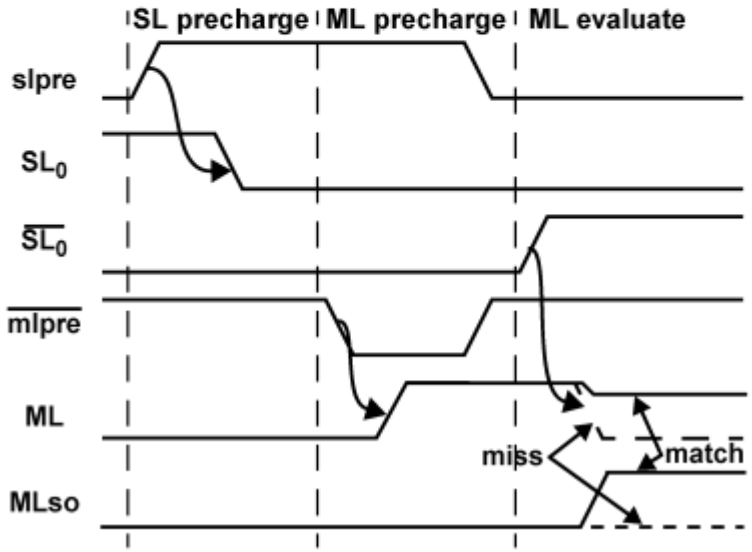
9-T NAND-type CAM

K. Eshraghian; K. R. Cho et al., *IEEE Trans. VLSI,* 19, p. 1407 (2011)

Content Addressable Memories (CAM)



(a)



(b)

K. Pagiamtzis; A. Sheikholeslami, *IEEE J. Solid-State Circuits, 41*, p. 712 (2006)

Content Addressable Memories (CAM)

TABLE I
PERFORMANCE COMPARISON OF PRIOR WORKS

	This work	[25]	[10]	[3]	[19]	[20]
Technology /Supply	65 nm /1.2V	130nm /1V	32nm/1V	65 nm/ 1V	65 nm/ 1V	130nm /1.2V
Search delay (ns)	1.07	0.9	0.145	1.92	0.6 (72 bits) 2.2 (240 bits)	3.5 ns
FOM (fJ/bit/search)	0.77	1.827	1.07	1.98	0.99	1.3
Normalized FOM*	1	1.09	2.48	2.37	1.2	0.65
Frequency	500 MHz	250 MHz	N.A	250 MHz	450	N.A
Chip area(mm^2)	0.125	1.4	N.A	99	0.078	N.A
Capacity	128×128	128×32	128×128	18 Mb	64x72	256x144

* Normalized FOM = FOM × (65 nm/technology node)×(1.2 V/VDD).

A. T. Do, C. Yin et al, *IEEE J. Solid-State Circuits, 49*, p. 1487 (2014)

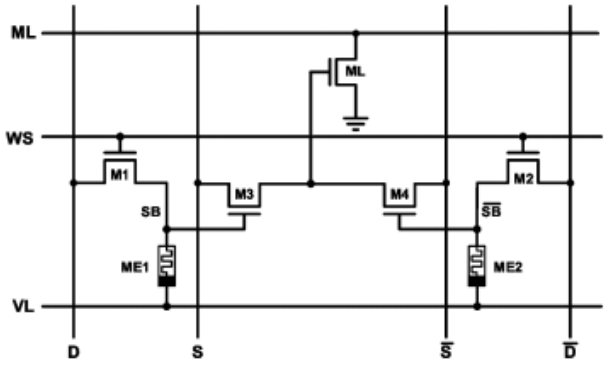
Content Addressable Memories (CAM)

TABLE I
FEATURES SUMMARY AND COMPARISONS

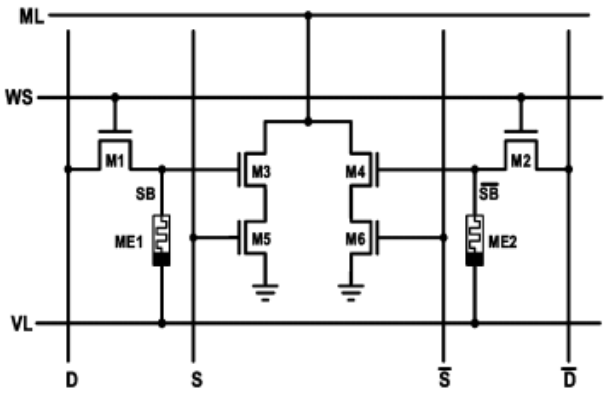
	Hybrid [19] (JSSC 2005)	PF-CDPD [15] (JSSC 2006)	Range Match [16] (ISSCC 2006)	Tree-style [17, 21] (JSSC 2008)	Charge Recycling [22] (ASSCC 2008)	This Work	
						Simulation	Test Chip Measurement
configuration	1024x144	256x128	512x144	256x128	1024x144	256x144	
Technology	100 nm	0.18 μm	0.13 μm	0.18 μm	0.18 μm	65 nm	
Area (mm^2)	2.8x4.2 (chip)	1.21x0.56 (core)	1.5x1.7 (core)	0.84x0.92 (core)	3.67x0.98 (core)	1.01x0.43 (core)	
Supply voltage (V)	1.2 V	1.8 V	1.2 V	1.8 V	1.8V	1.0 V	
Search time (ns)	2.20 ns	2.10 ns	4.80 ns	1.56 ns	100MHz	0.38ns	400MHz
Energy metric (fJ/bit/search)	0.700	2.330	0.590	1.420	6.300	0.113	0.165
Normalized Search time T* (ns)	1.716	1.365	2.880	1.014	N.A.	0.380	N.A.
Normalized Energy metric E* (fJ/bit/search)	0.316	0.260	0.205	0.158	0.702	0.113	0.165

P. T. Huang, W. Hwang, *IEEE J. Solid-State Circuits, 46*, p. 507 (2011)

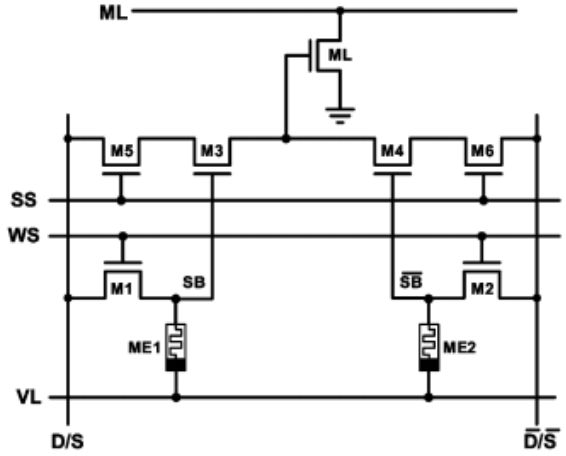
Content Addressable Memories (CAM)



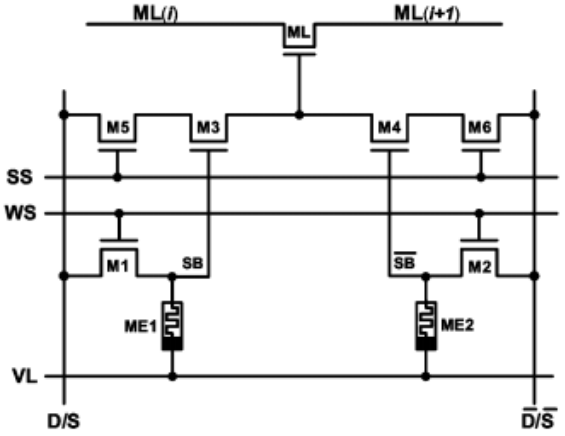
5T-2R NOR-type CAM



6T-2R NOR-type CAM



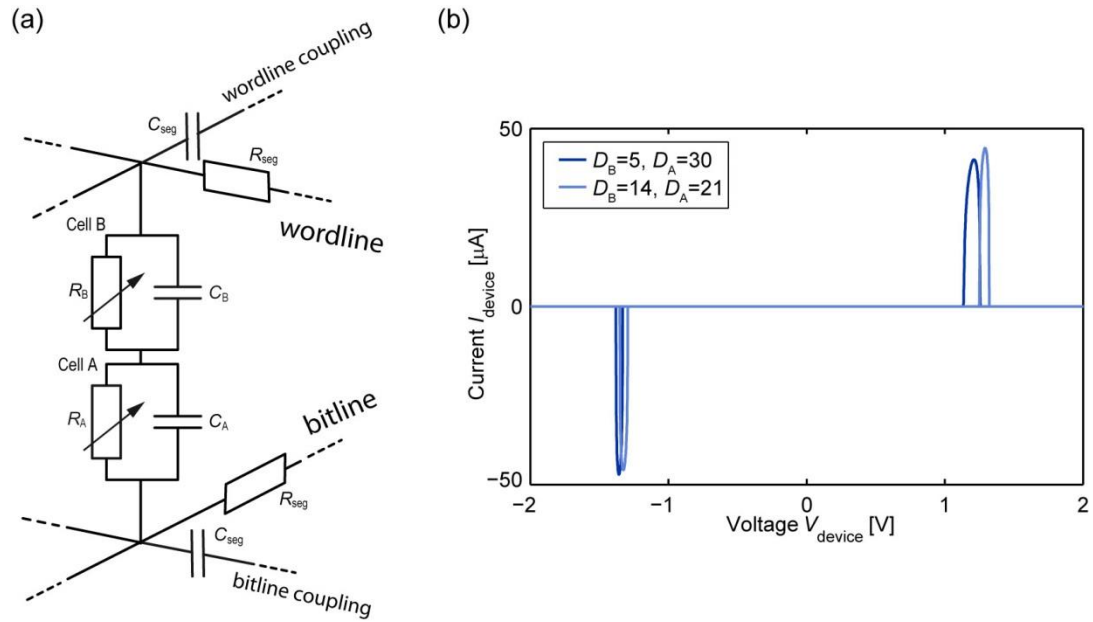
7T-2R NOR-type CAM



7T-2R NAND-type CAM

K. Eshraghian; K. R. Cho et al., *IEEE Trans. VLSI,* 19, p. 1407 (2011)

VerilogA core cell



$F = 40$ nm

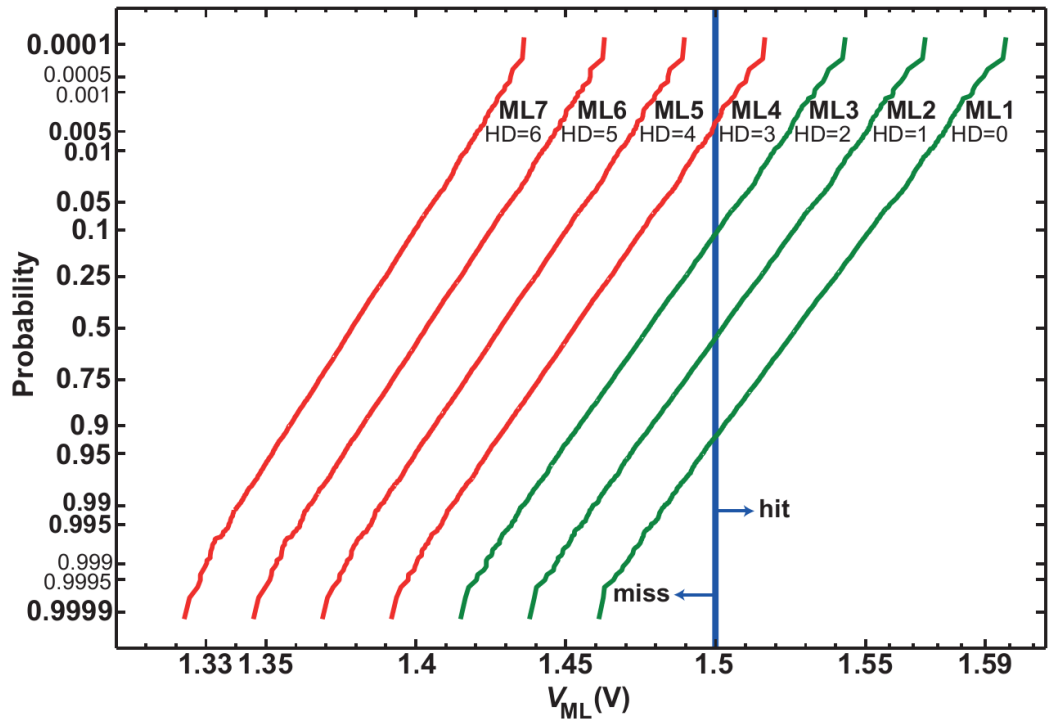
$C_{seg} = 2.76$ aF

$R_{seg} = 0.86\ \Omega$

SiO_2 as interline material ($\varepsilon_r = 3.9$)

$D_A / D_B = 21$ nm / 14 nm = 1.5 ($C_A/C_B = 1/1.5$)
$D_A / D_B = 24$ nm / 12 nm = 2 ($C_A/C_B = 1/2$)
$D_A / D_B = 28$ nm / 7 nm = 4 ($C_A/C_B = 1/4$)
$D_A / D_B = 30$ nm / 5 nm = 6 ($C_A/C_B = 1/6$)

Monte Carlo Simulations



Probability function (p) of seven top match-lines with minimum HDs versus V_{ML}. The detection probability can be interpreted as *p*. In order to detect HD=0, (ML1), with p=95% chance, V_{TH} has to be around 1.5 V. Under these circumstances a successful detection over a range of outputs is achieved. If HD=0, the output is 1 with 95% probability. For HD=1, the output is 1 with 50% probability, while for HD=2 the probability for an output 1 is 10%. For HD=3, only a probability of 0.5% for observing an output 1 is given. The probability that output is 1 for HD > 3 tends to have negligible small values. Thus, HD < 4 are detect-able with high probability.

Variable	Mean (μ)	Relative 3σ
Supply and input voltages	3 V	10%
Series resistors on each ML	100 Ω	10%
Device thickness	20 nm	10%
Top electrode width	5 μm	10%
Middle electrode width	10 μm	10%
Bottom electrode width	15 μm	10%
Load capacitor (C_{ML})	22 pF	10%
RRAM ON resistance (R_{ON})	1 kΩ	20%
RRAM OFF resistance (R_{OFF})	1 MΩ	20%

Probability–voltage distribution for seven outputs with HD=0 to 6 that correspond to $ML_1$to ML_7. The solid blue line indicates VTH in our test-bench circuit. Outputs with a voltage amplitude above the threshold voltage are treated as ‘hit’ and below that are treated as ‘miss’

O. Kavehei, E. Linn et al., *Nanoscale*, 5, 5119 (2013)