R2RAM 640073 H2020 Project

Cristiano Calligaro

RedCat Devices - c.calligaro@redcatdevices.it

Outline

- R2RAM Consortium
- R2RAM Goals
- R2RAM Technology
- R2RAM Test Vehicle
- R2RAM Testing approach

R2RAM Consortium

The IHP is an institute of the Leibniz Association and conducts research and development of silicon-based systems and ultra high-frequency circuits and technologies including new materials. It develops innovative solutions for application areas such as wireless and broadband communication, aerospace, biotechnology and medicine, automotive industry, security technology and industrial automation.
Key Person and Project Coordinator: Christian Wenger

IUNET (Italian Universities Nano-Electronics Team), is a non-profit Organization, aimed to lead and coordinate the effort of the major Italian university teams in the field of silicon-based nanoelectronic device modelling and characterization. Current members of IUNET are the Universities of Bologna, Calabria, Ferrara, Modena e Reggio Emilia, Padova, Pisa, Udine, Roma “La Sapienza” and the Politecnico of Milano. **Key Person: Prof. Piero Olivo**

The University of Jyväskylä (JYU) is one of the largest universities in Finland. Department of Physics (JYFL) of the university belongs to the Faculty of Mathematics and Science. Accelerator laboratory of JYFL has operated very successfully as one of the Large Research Access Infrastructures in the FP4 - FP7 programmes of the EU since 1996 (ENSAR for 2013-2014) and acted as a FP5 Marie Curie Training Site. Since 2005 laboratory’s RADiation Effects Facility, RADEF has been qualified to one of the External European Component Irradiation Facilities of European Space Agency, ESA. **Key Person: Prof. Ari Virtanen**

UNIVERSITY OF JYVÄSKYLÄ

RedCat Devices (RCD) is a privately held fabless semiconductor company involved in several fields of research concerning memories (volatile and non volatile), analog components (ADCs, DACs) and standard digital libraries for special applications. In the last eight years RCD has been involved in several R&D projects including FP7 262890 SkyFlash in the role of coordinator. **Key Person: Cristiano Calligaro**

RedCat Devices

R2RAM Goals

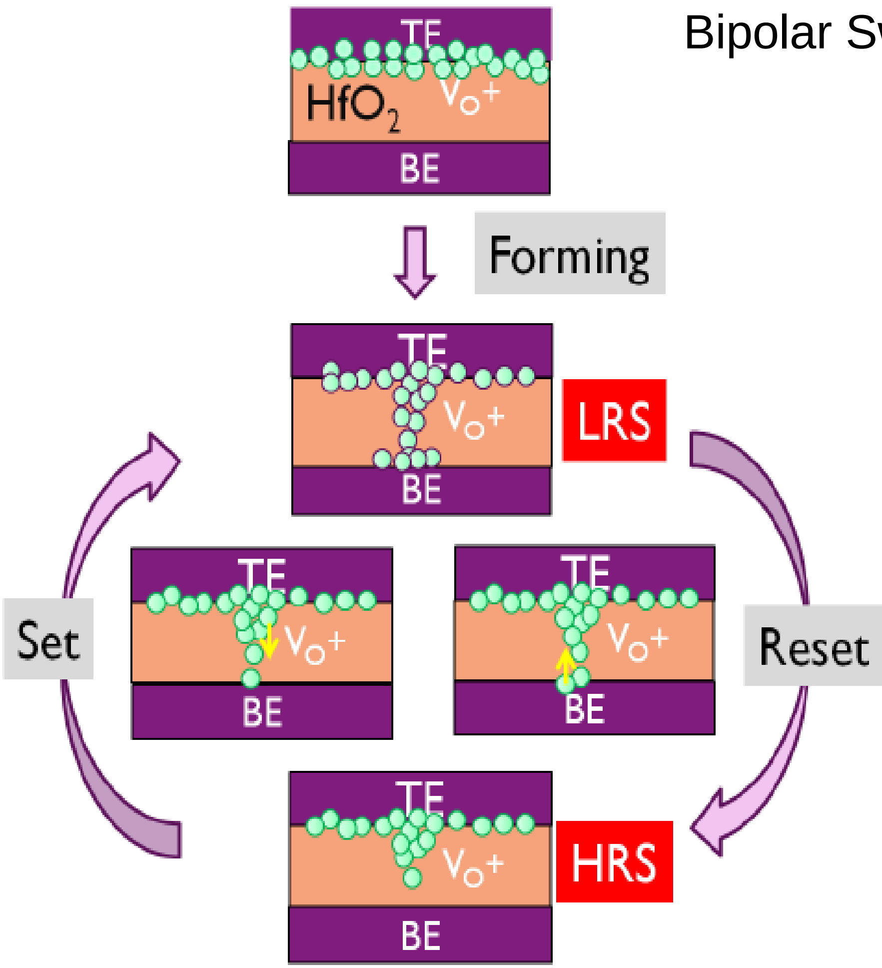
Development and design of a radiation hard non-volatile memory technology by using standard CMOS silicon processing.

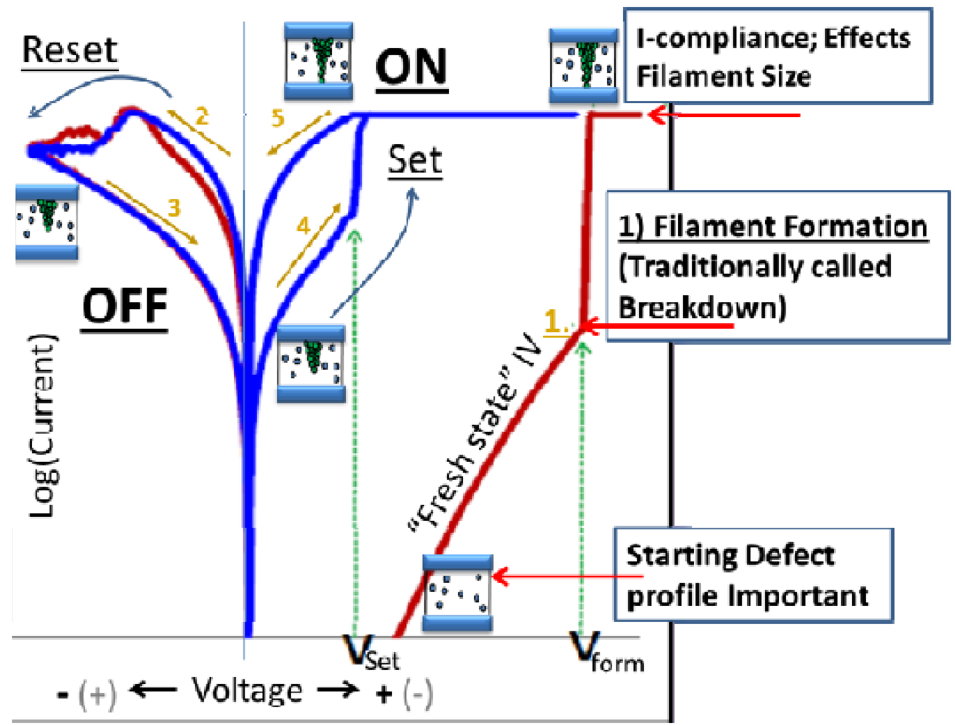
New R^{2}RAM approach:
Using the Resistive random-access memory (RRAM) technology

www.r2ram.eu

R2RAM Technology

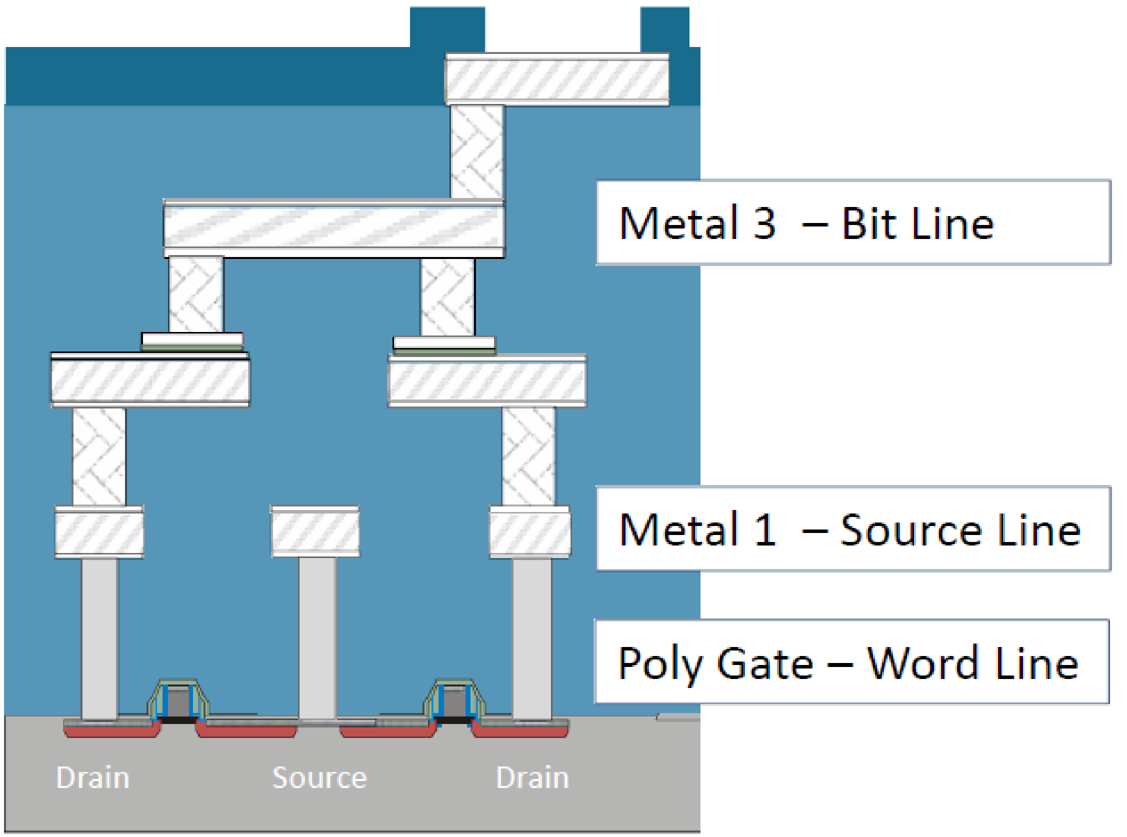
Bipolar Switching effect in Ti/HfO_2 based MIM cells

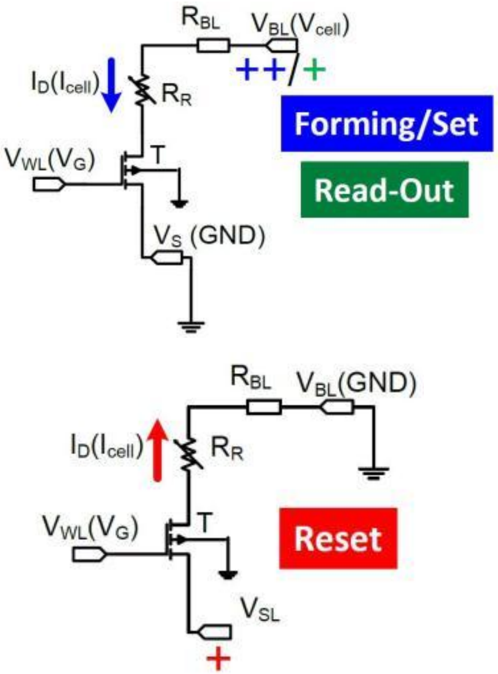




Schematic 1T1R Device

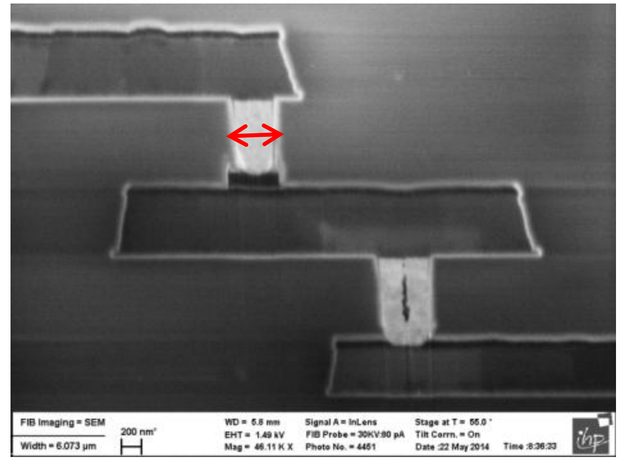
TiN/HfO$_2$/Ti/TiN 1T1R Devices:



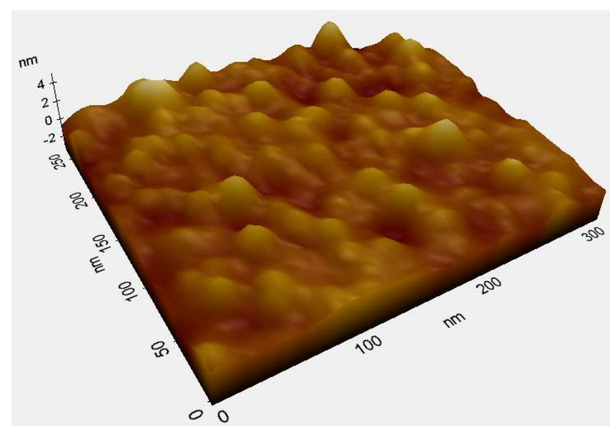


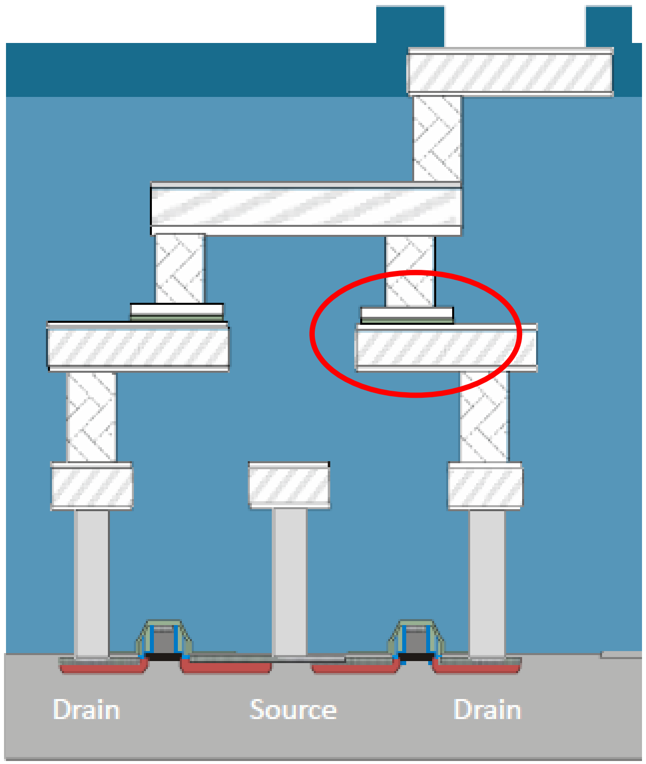
Schematic 1T1R Device (Integration Issues)

1. Cell size: > 500 nm



2. Surface roughness of Met 2: > 2 nm

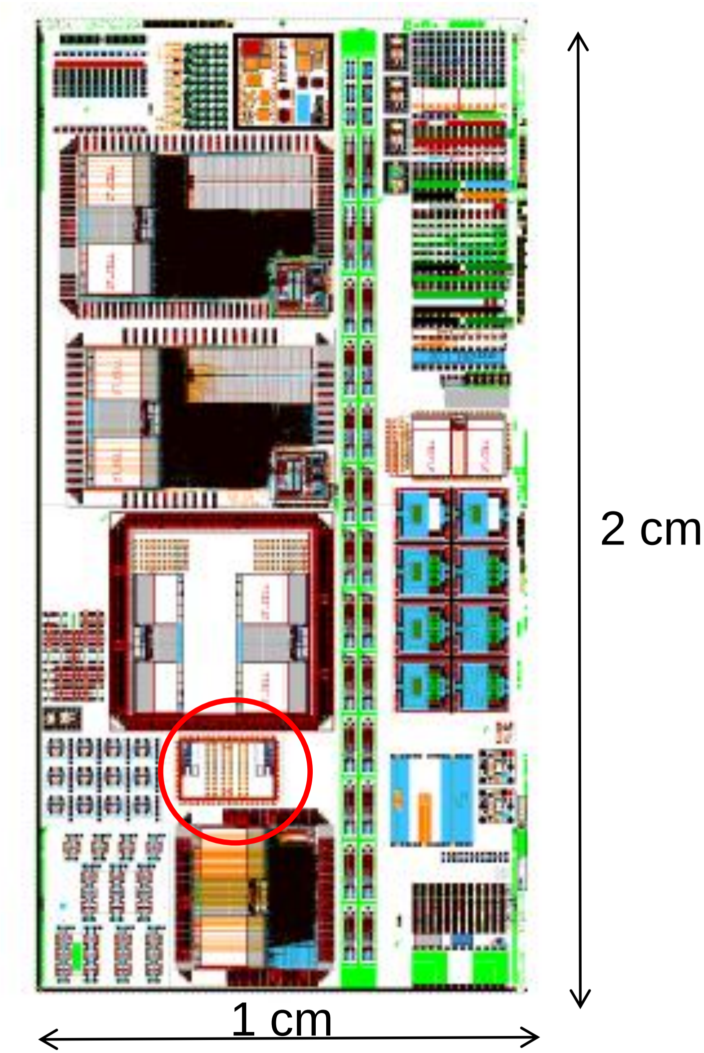




3. Final anneal at 400 °C for 30 min

MPW Approach

Testfield 284



Cost sharing (Multi Project Wafer):

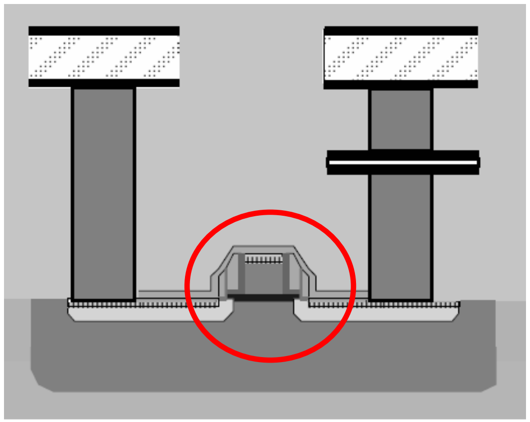
Every circuit designer is using the same design kit

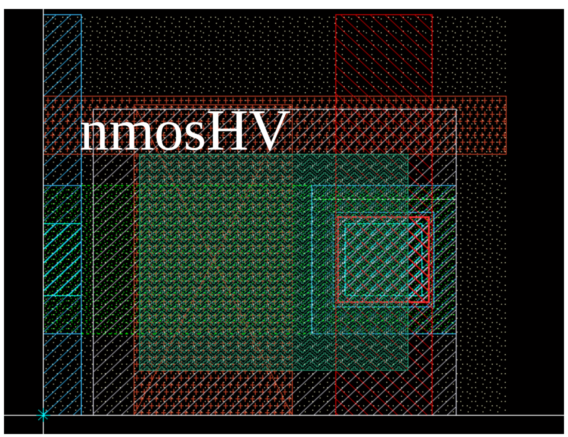
Process flow is equal until finalized Metal 2, split of RRAM wafers

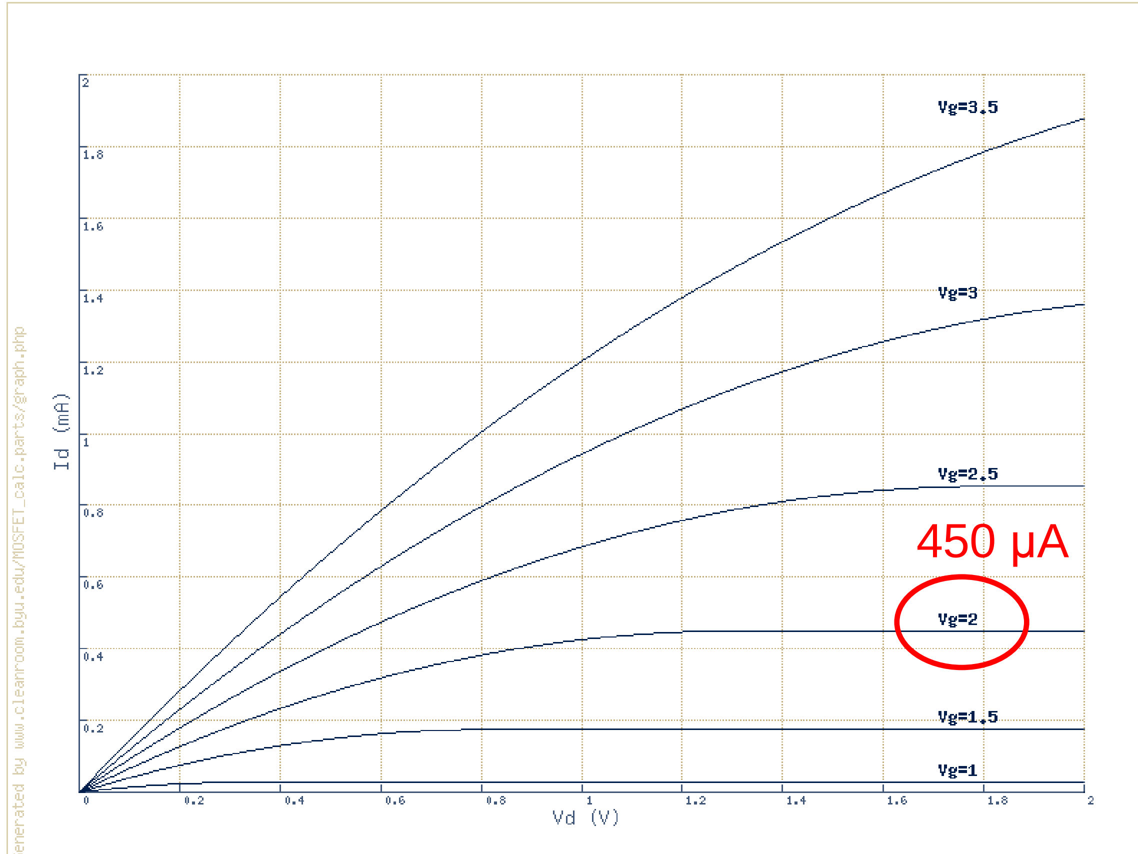
Required additional process steps:

- HfO_2 deposition by CVD or ALD
- Ti/TiN deposition by PVD
- $TiN/Ti/HfO_2$ etching by RIE

Choice of NMOS Select Transistor



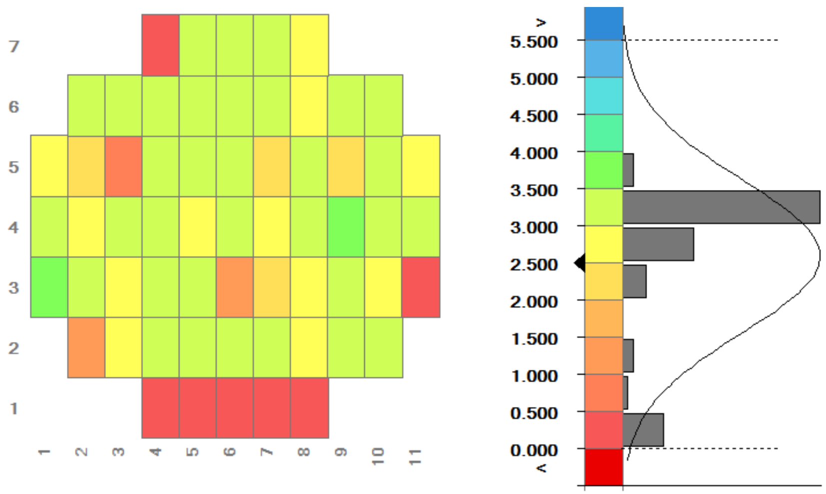




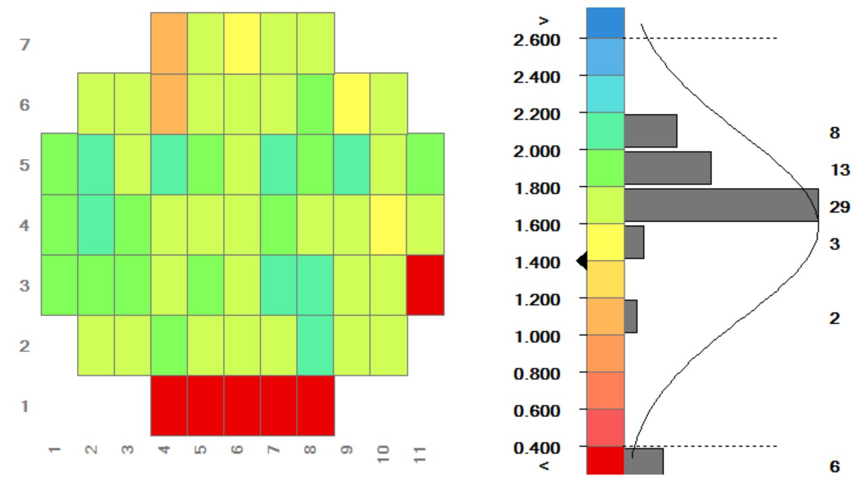
Lenght: 0.3 µm
Width: 0.3 µm
Oxide: 5.0 nm

Yield poly-christalline HfO_2

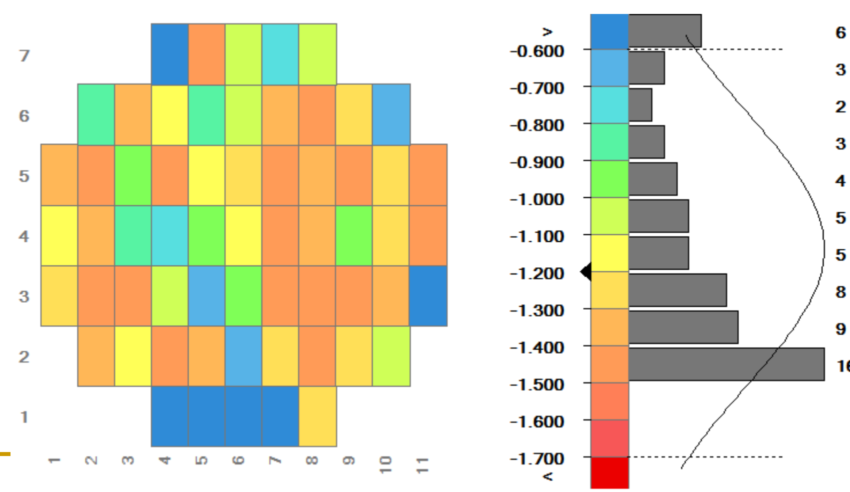
Forming



Set



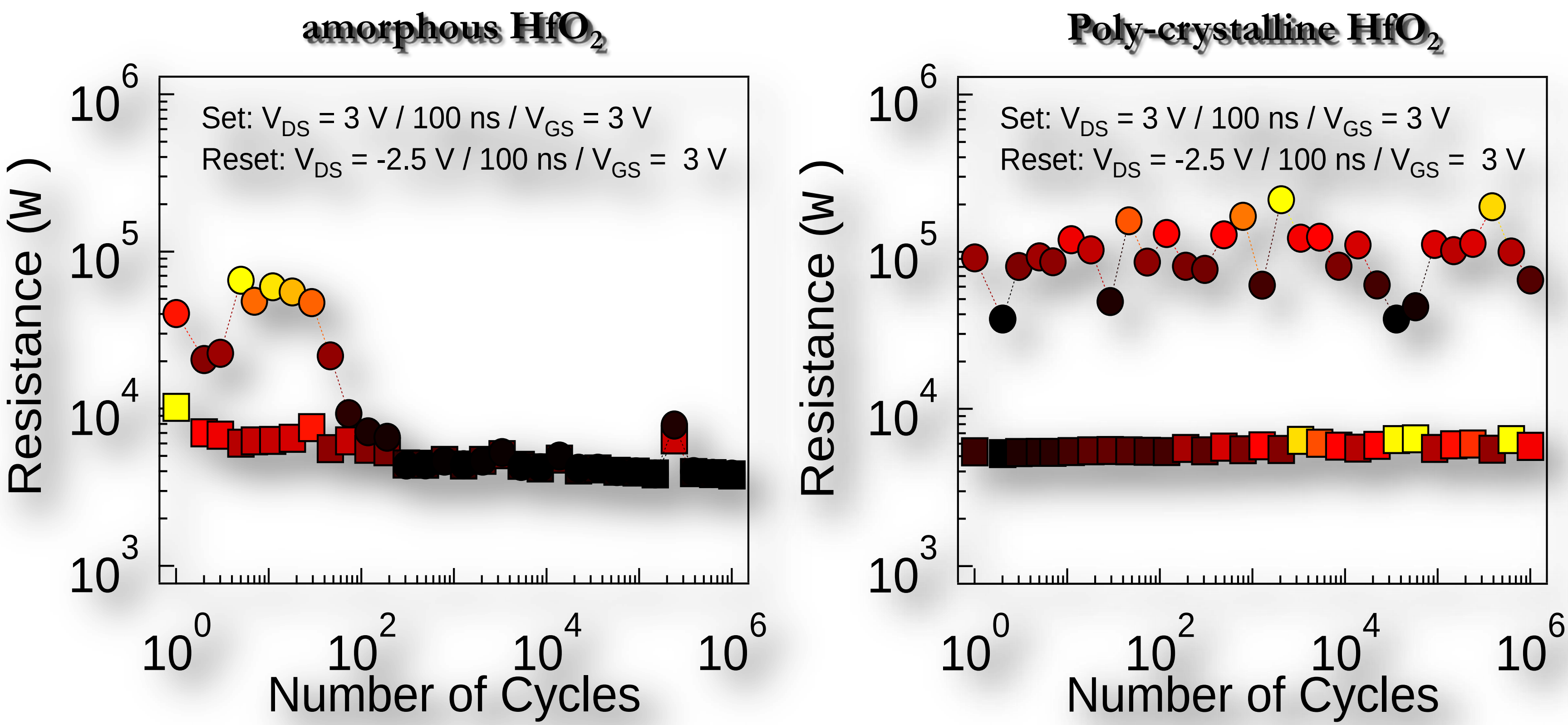
Reset



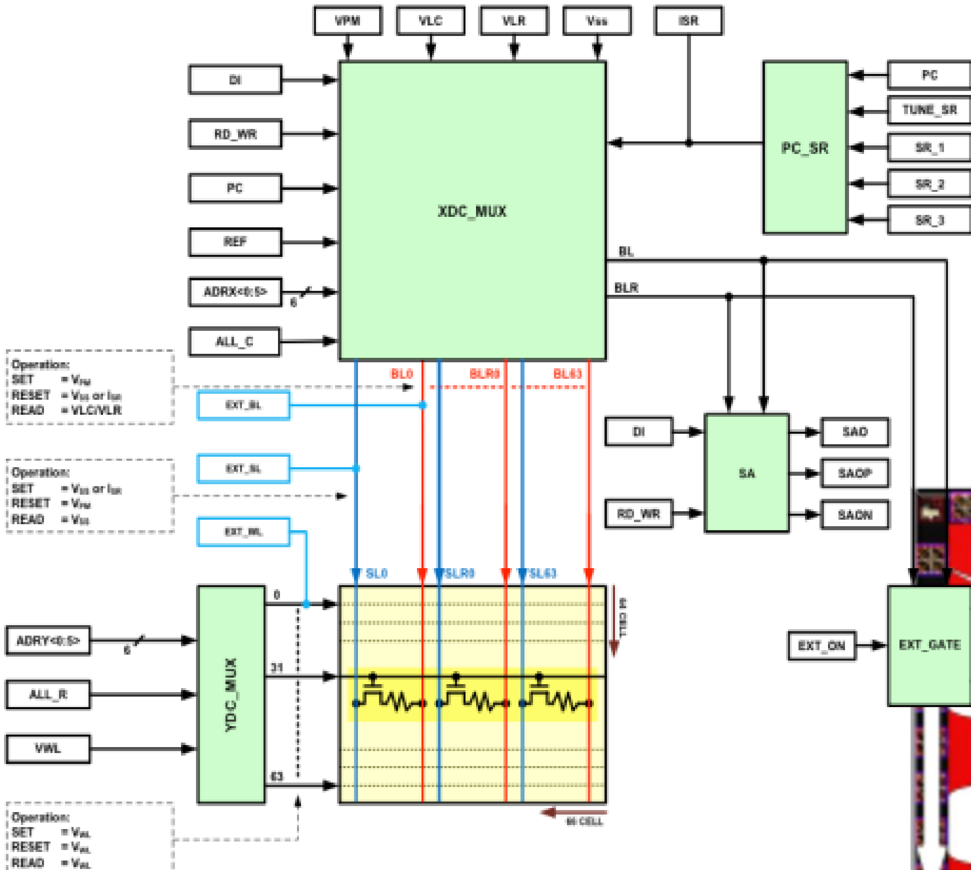
V_{read}=0.2 V, $V_{set,WL}$=2 V, $V_{set,BL}$=2 V,
$V_{reset,WL}$=3 V, $V_{reset,SL}$=1.5 V

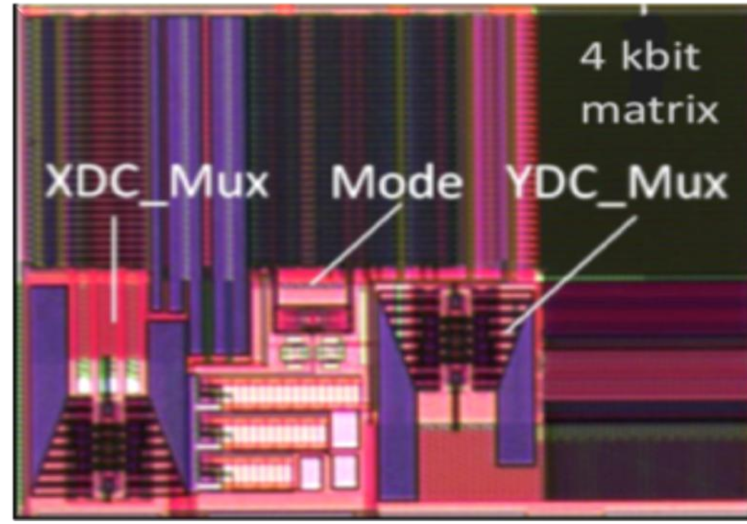
Endurance of single 1T1R device

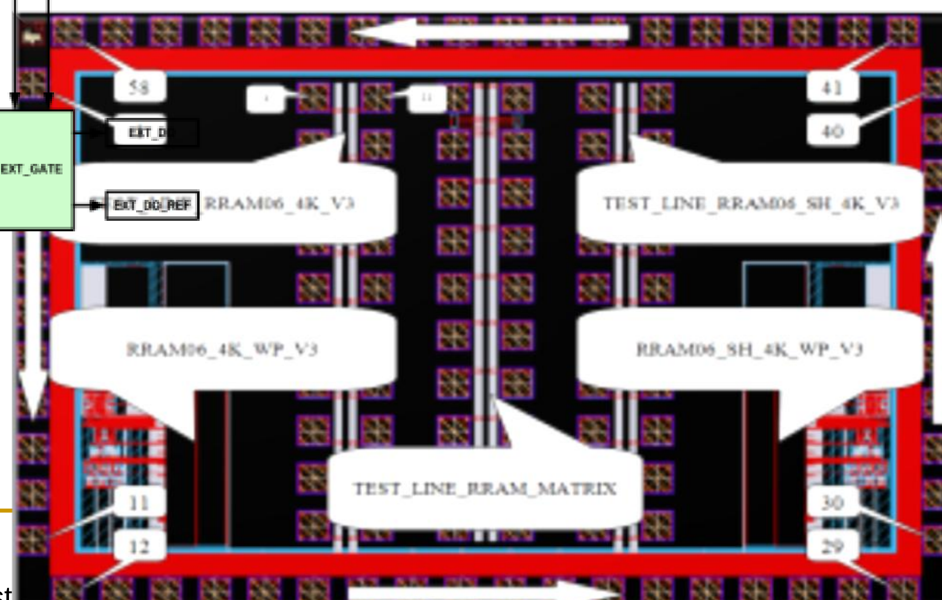
Stable endurance for poly HfO_2



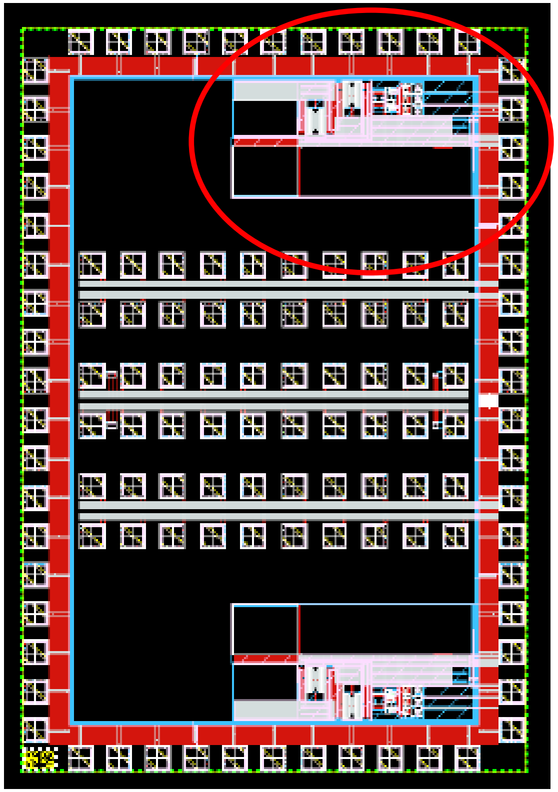
4Kbit Test Vehicle (200mm wafer, 0,25 µm)



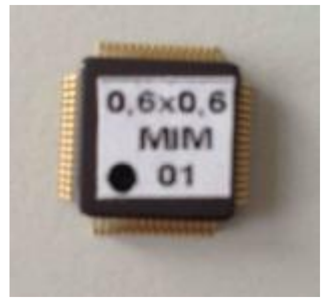




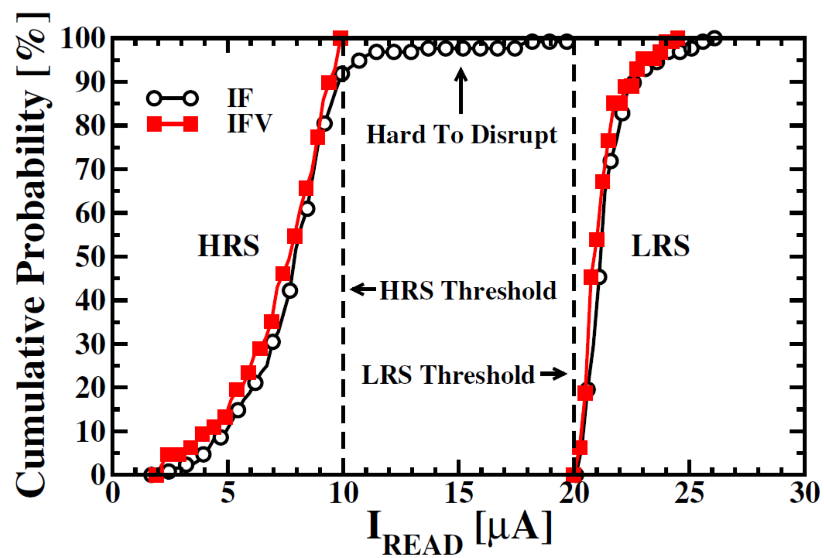
4Kbit Test Vehicle (Test at Univ. Ferrara)



4kbit array

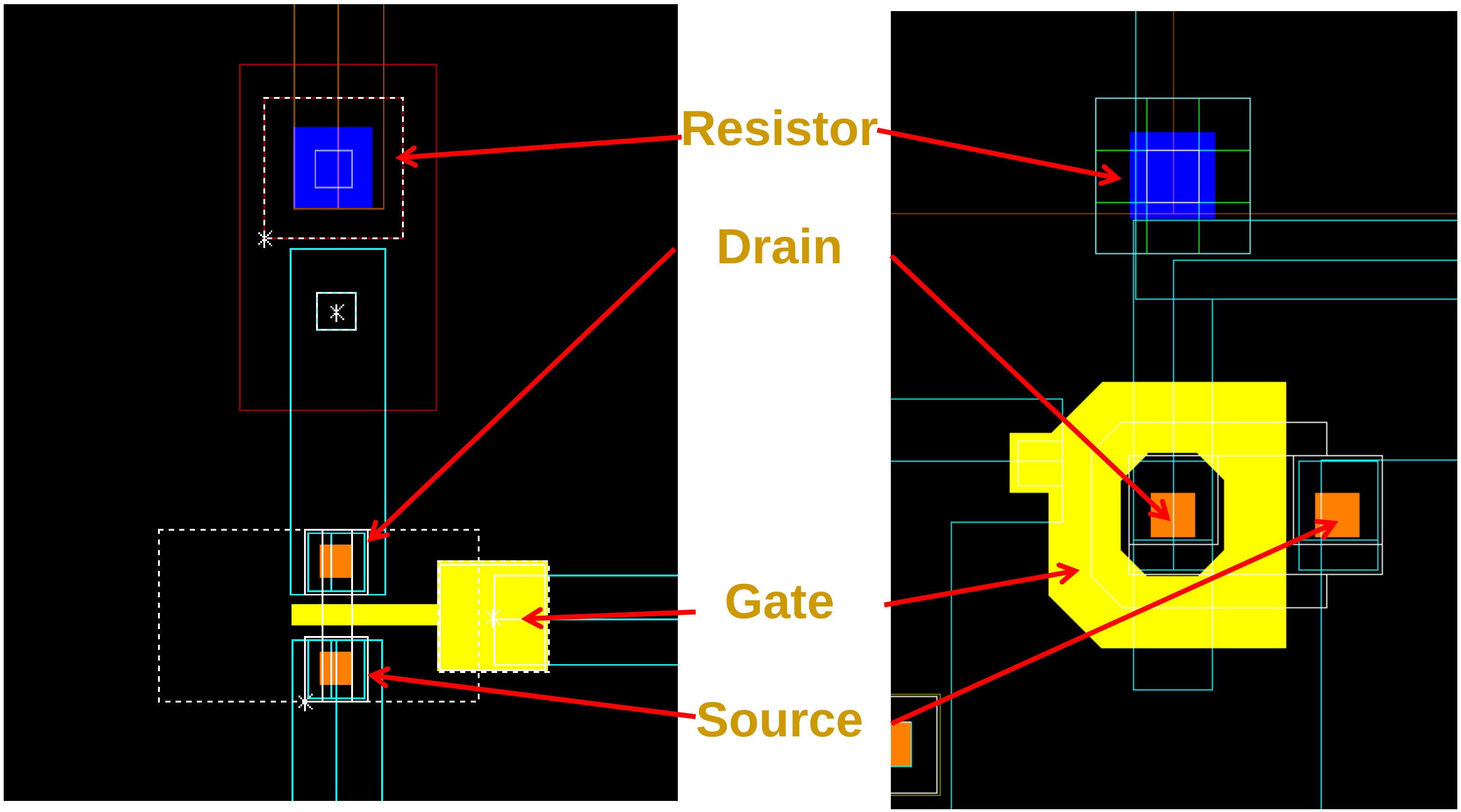


Incremental Form and Verify (IFV):



New rad-hard 1T1R design

Standard cell: Rad-hard cell:

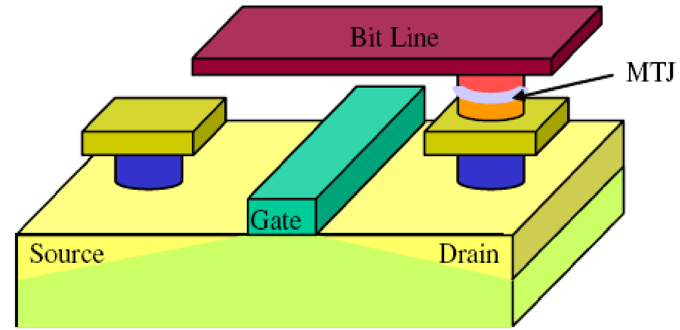


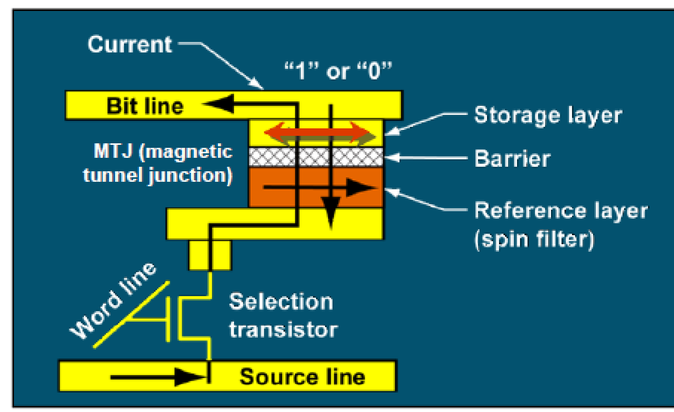
R2RAM Test Vehicle (The SkyFlash heritage)

• SkyFlash has been focused on Nitride Flash cells but many blocks are in common with others NVM technologies.

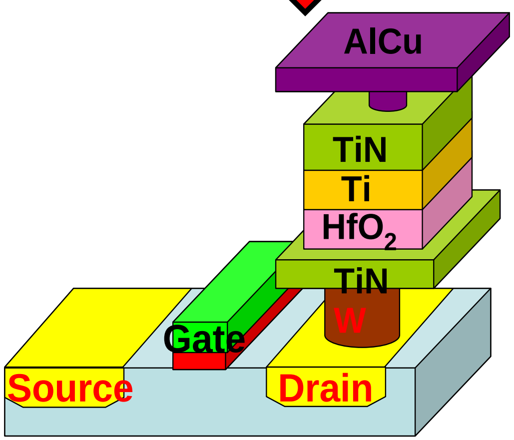
SkyFlash Roadmap
decoders, sense amplifiers, memory architecture, double cell, charge pumps, bandgap references, I/O pads, HV distribution, level shifters, S-Flash, CEONOS, final stages, ATDs, etc…

MTJ

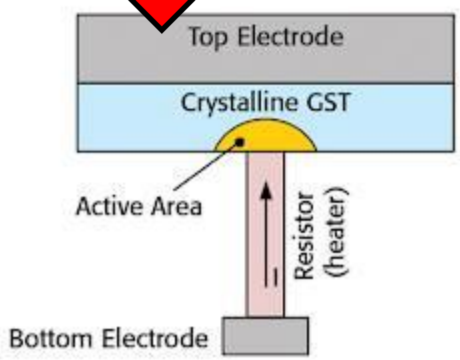


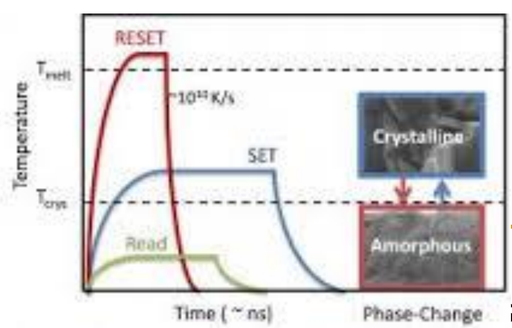


RRAM



PCM

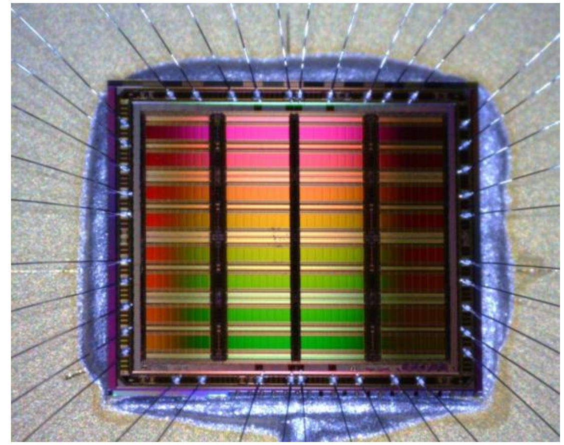


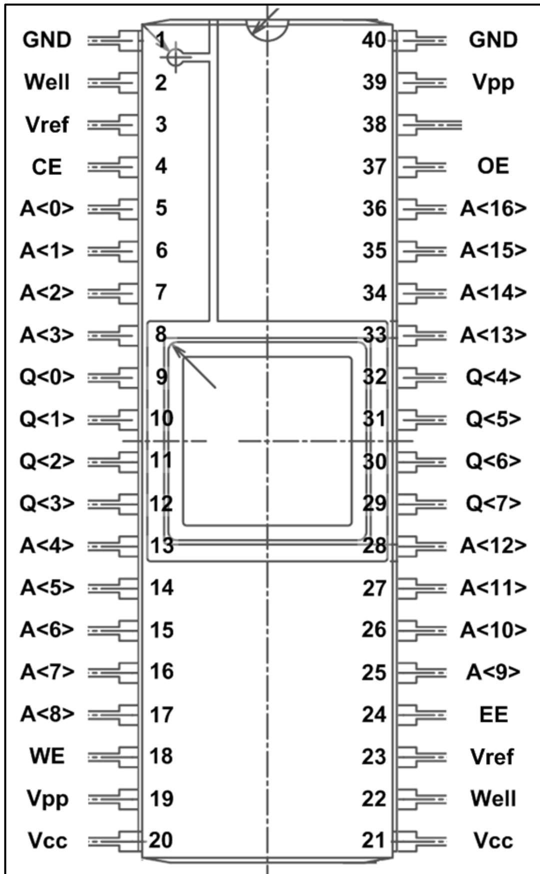


RedCat Devices

SkyFlash Test Vehicles

1Mbit (128kbit x8)



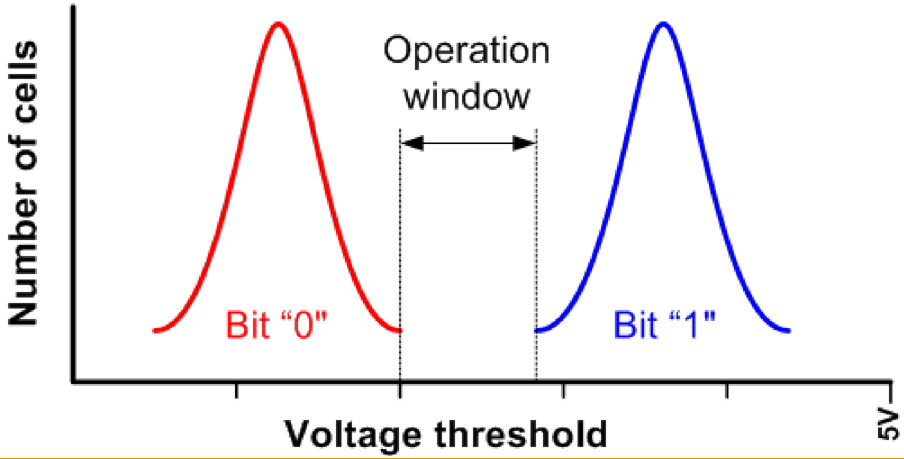


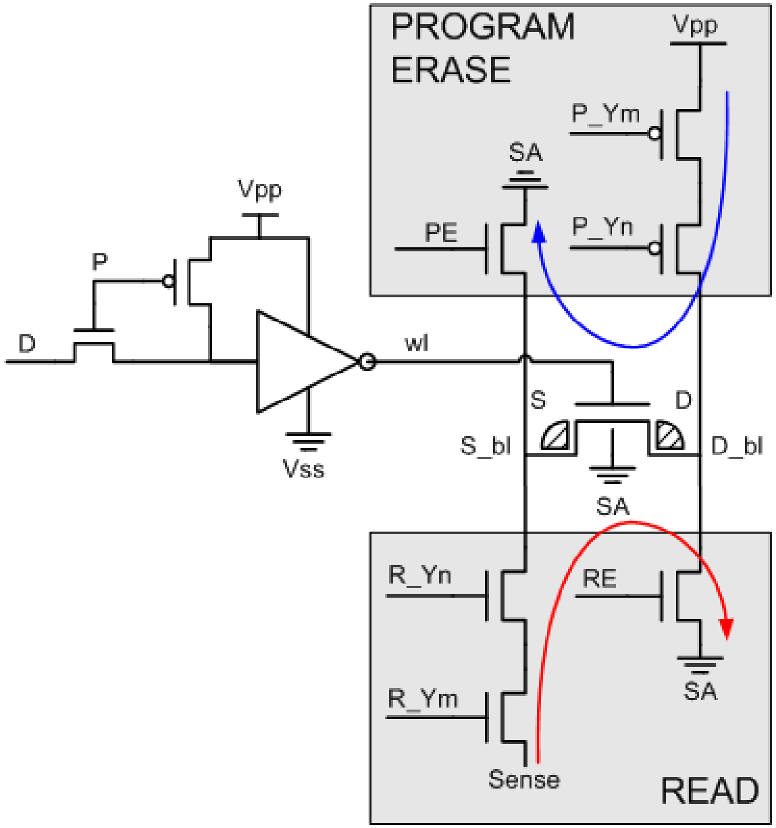
Prototype Code	Description
RC27F1024SKY1	1Mbit OTP with external HV
RC27F1024SKY2	1Mbit OTP with internal charge pump
RC27F1024SKY3	1Mbit OTP with internal charge pump and reference array
RC27F1024SKY4	1Mbit OTP with internal charge pump and bgref
RC27F1024SKY5	1Mbit OTP with charge pump for erasing
RC27F1024SKY6	1Mbit OTP refinement of SKY5
RC28F1024SKY1	1Mbit NVM based on SKY4 (CEONOS replacement)

From NROM to ReRAM 1/2

Cell program and erase is based on hot carrier mechanism (CHE) and hot holes generated by band-to-band (BTB) tunneling. The injection of charge in the nitride produces a shift on the threshold voltage. The programming is done from the drain side with voltages of 5-6V using 3.3V transistors.

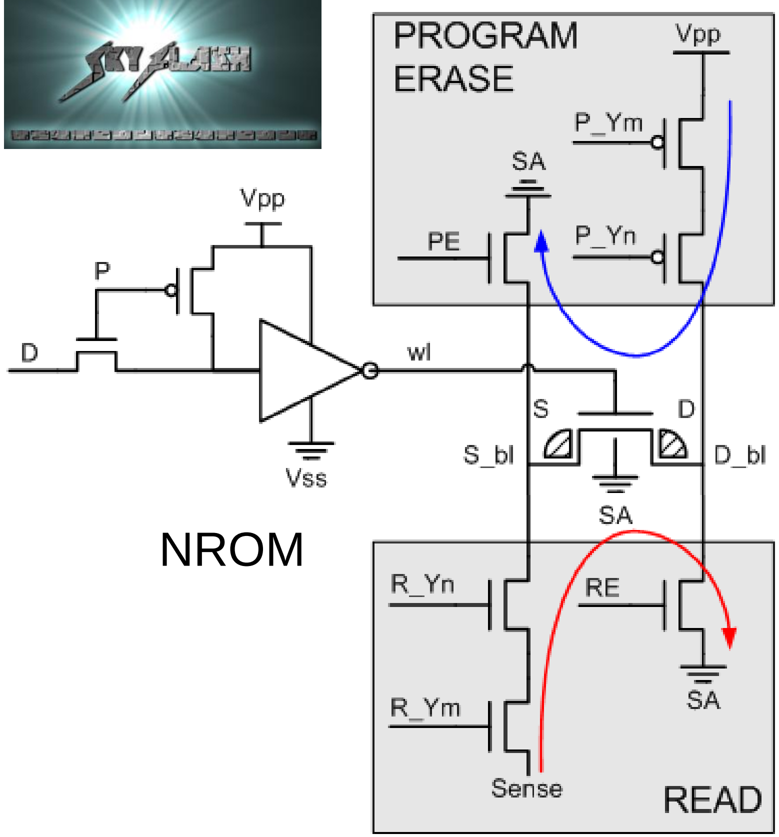
Each bit is represented with different V_{th} and the distance between them is the operation window. Reading is done on the reverse direction of programming (source), allowing to separate high voltage circuitry from the reading stage.

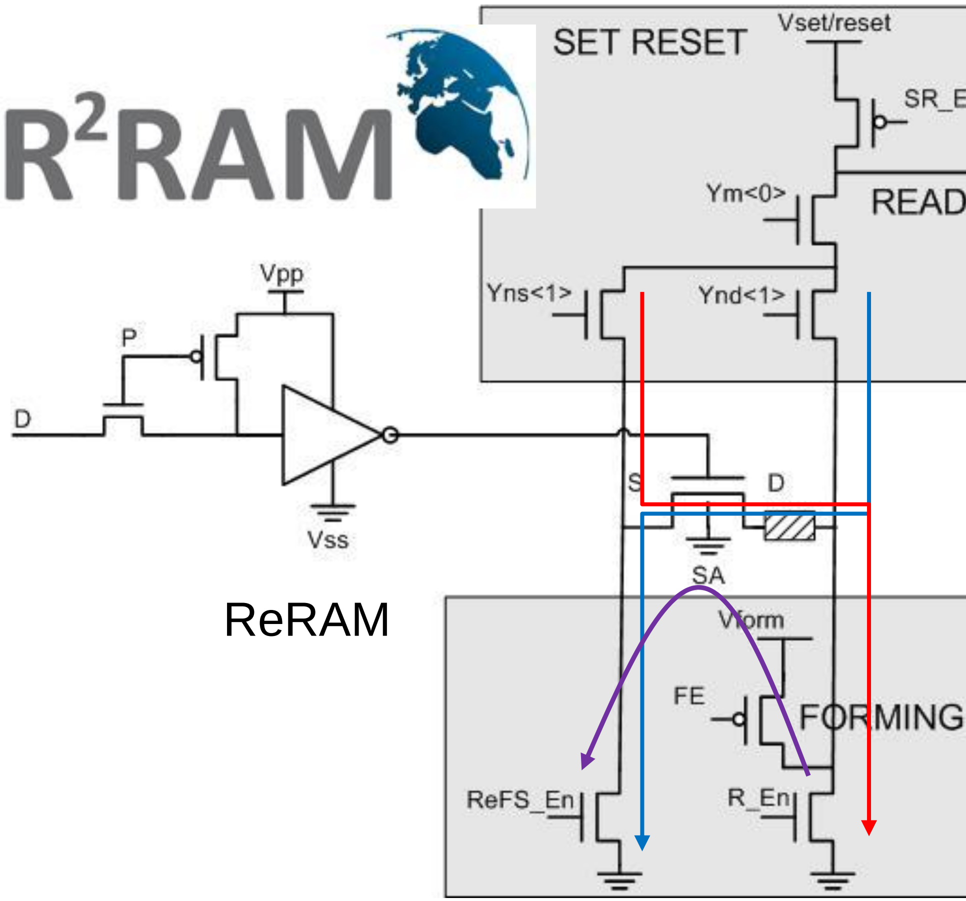




From NROM to ReRAM 2/2

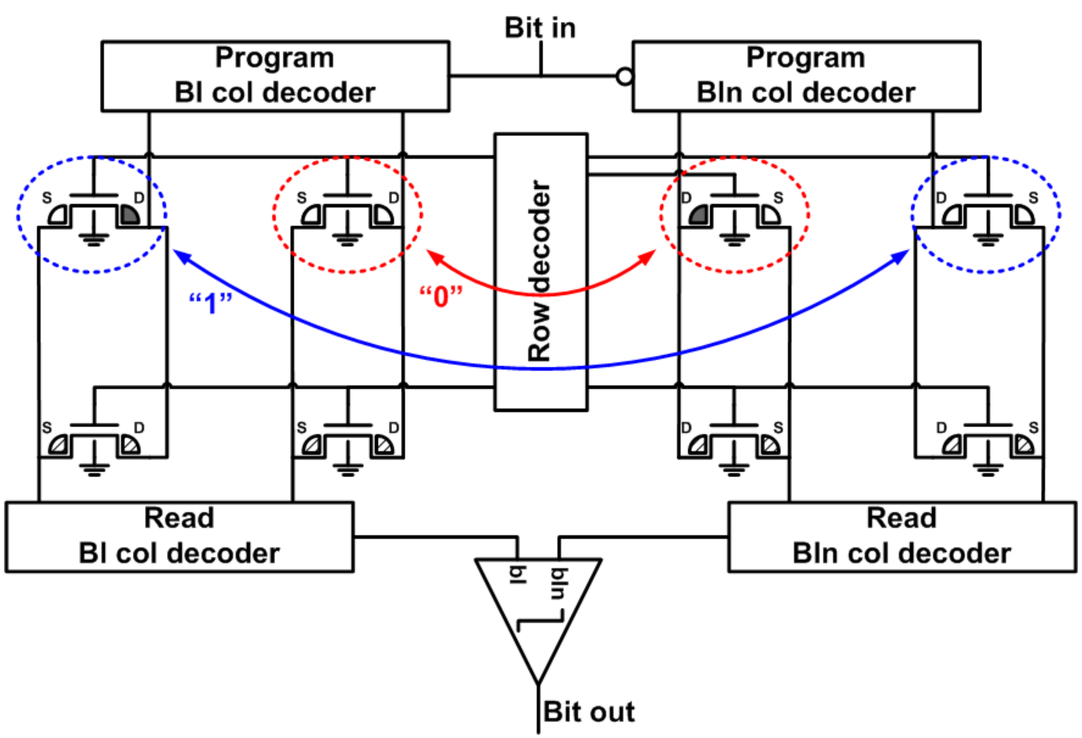
Despite the differences between the two cells, the main goal is to maintain the same architectural approach in the test vehicle

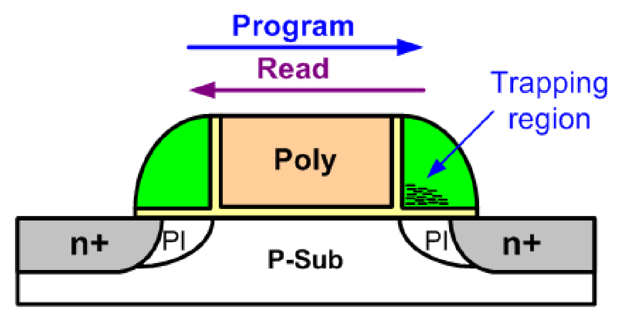


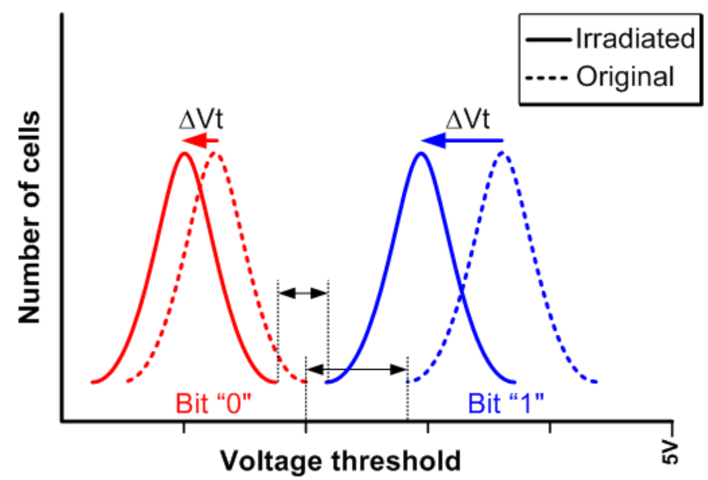


Differential Cell Approach (2 cells for 1 bit)

Two cells corresponding to the single bit are placed in two independent arrays. The minimum distance between the two cells of the bit is 70µm (length of row decoding scheme).



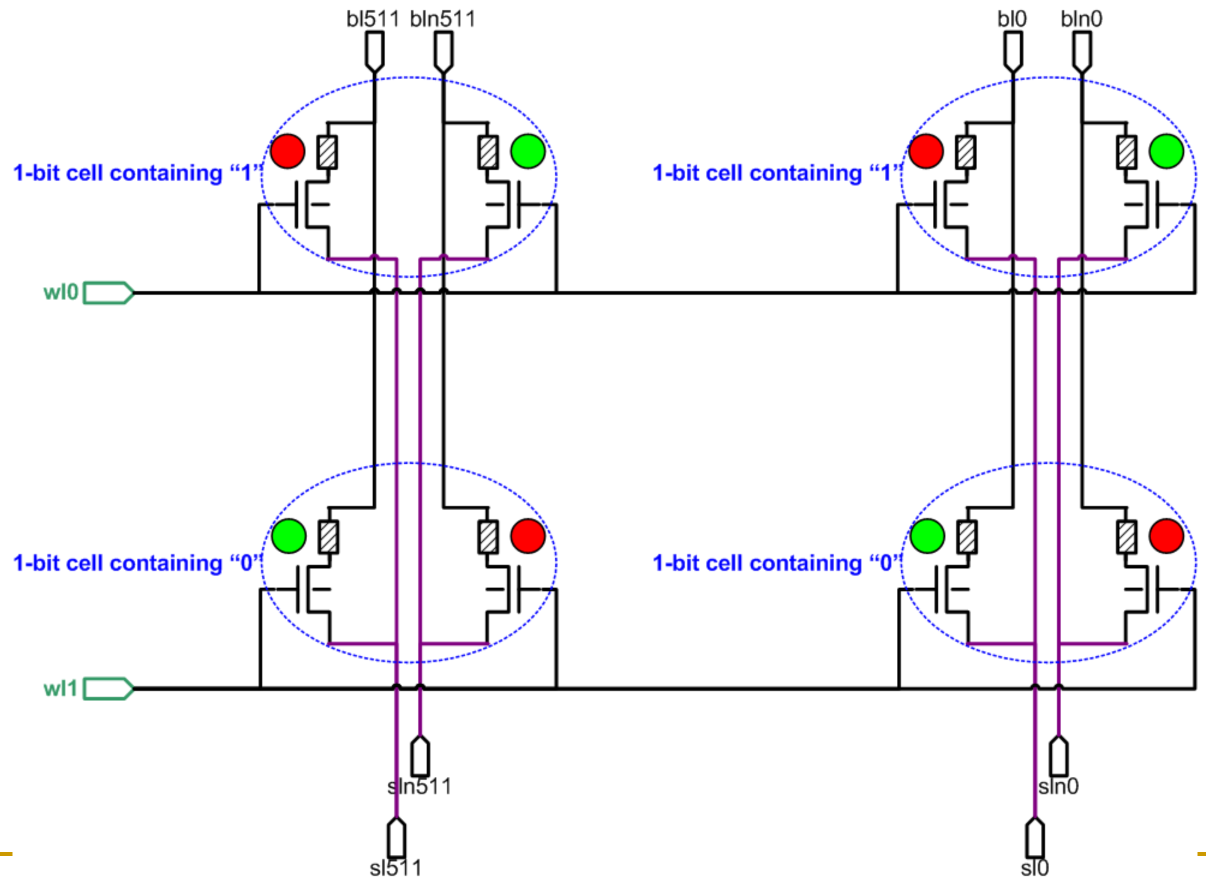




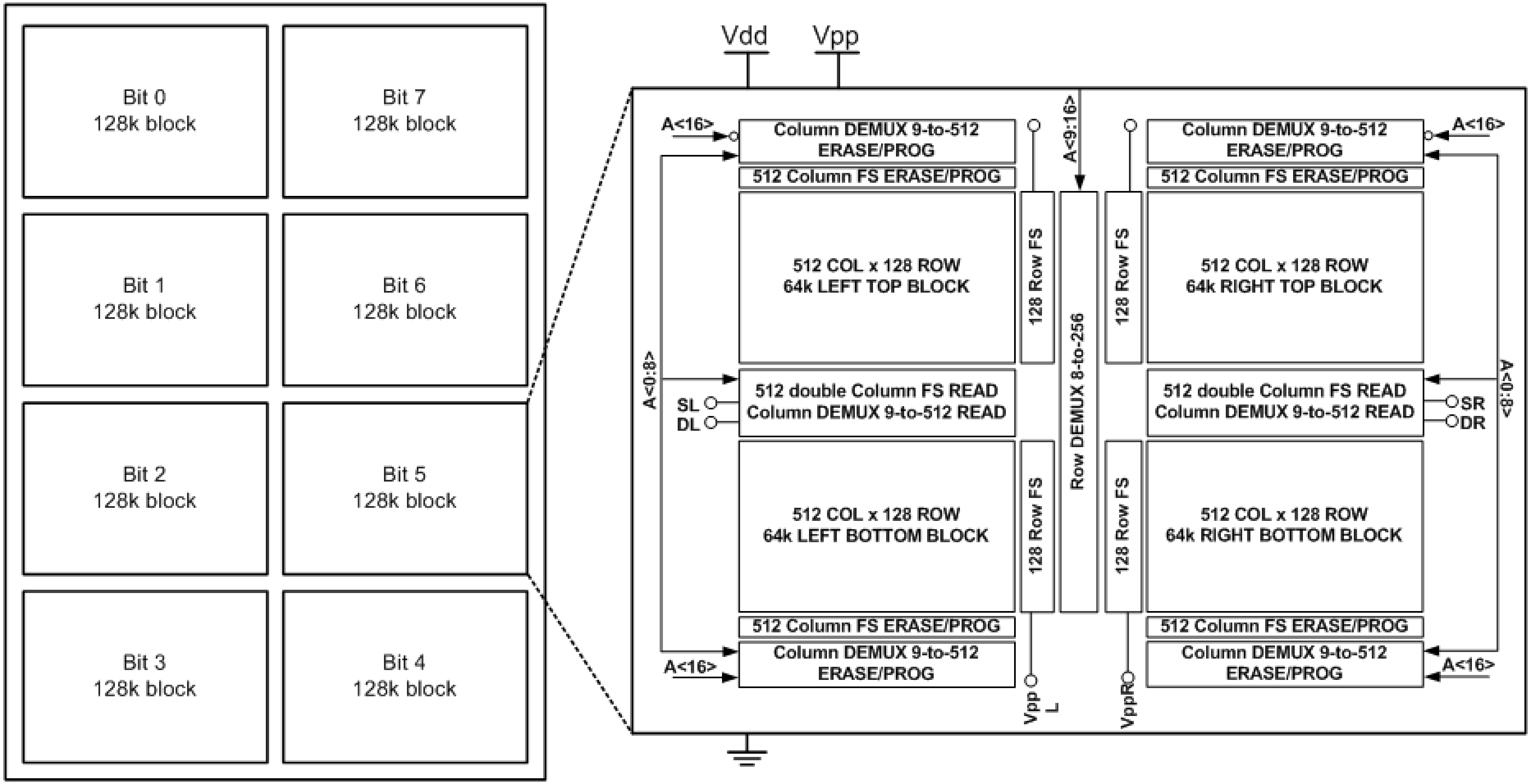
Differential Cell in R2RAM

RedCat Devices

The differential approach in memory array foresees a low resistance cell on the left and a high resistance cell on the right. We call this status “1”. Vice-versa for “0”. This architectural approach does not require ANY reference cell.

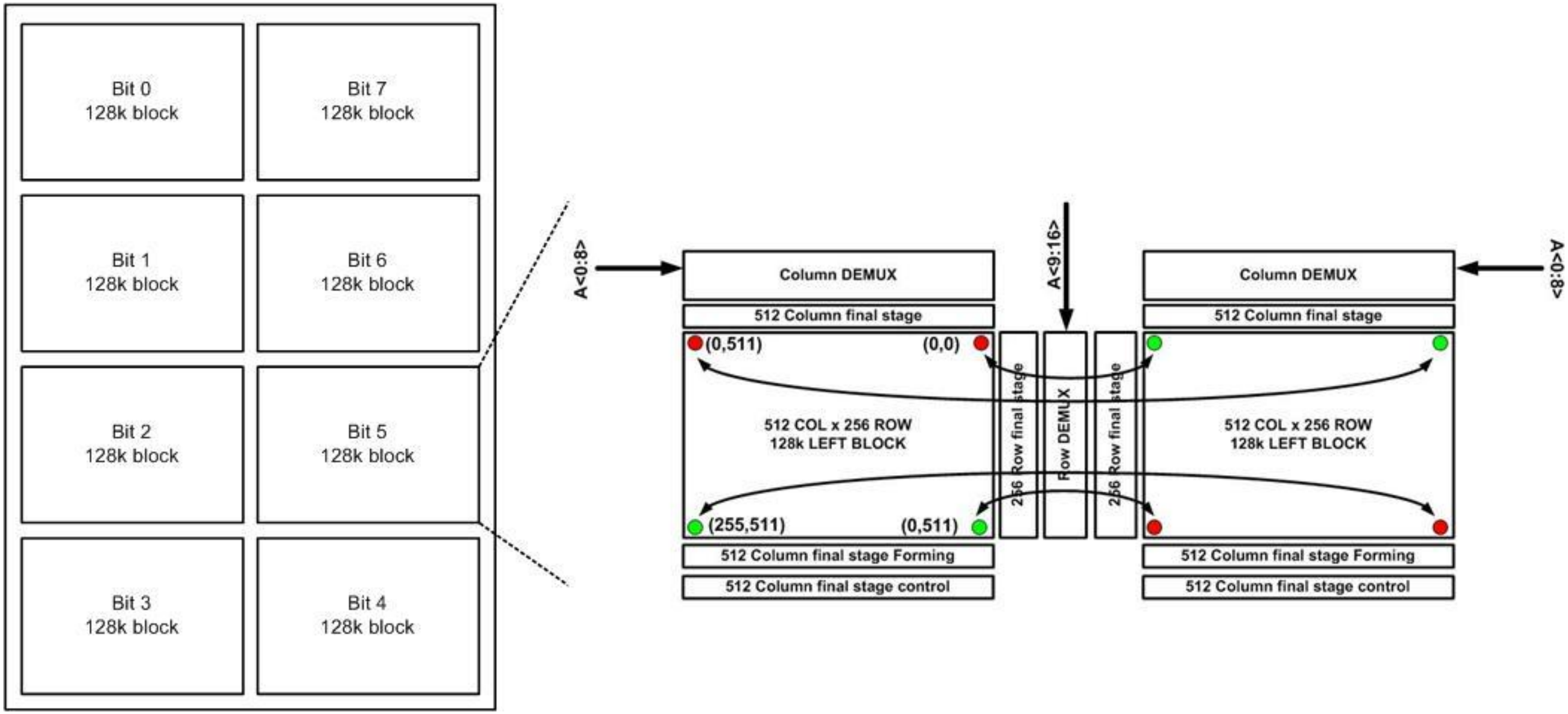


SkyFlash 1Mbit (RC27F1024SKYn)

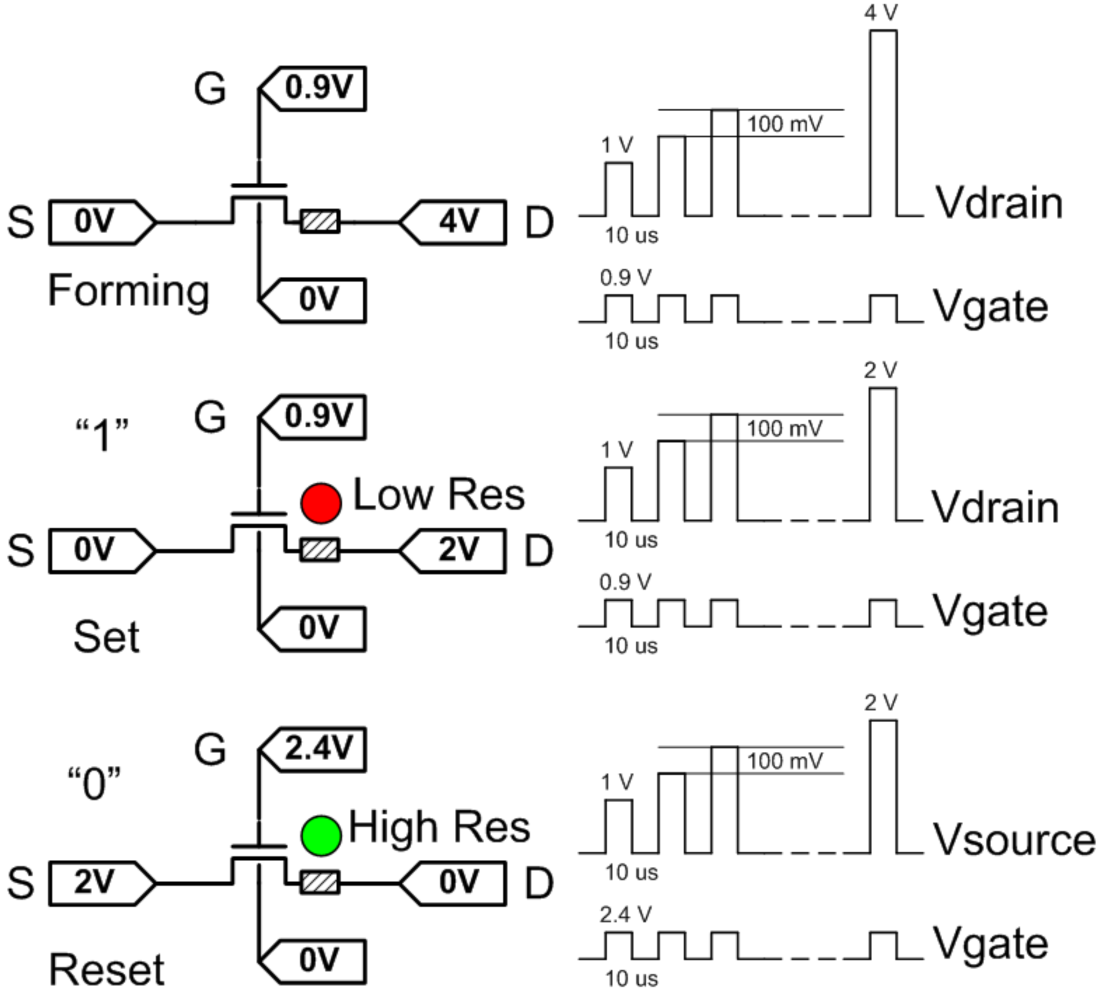


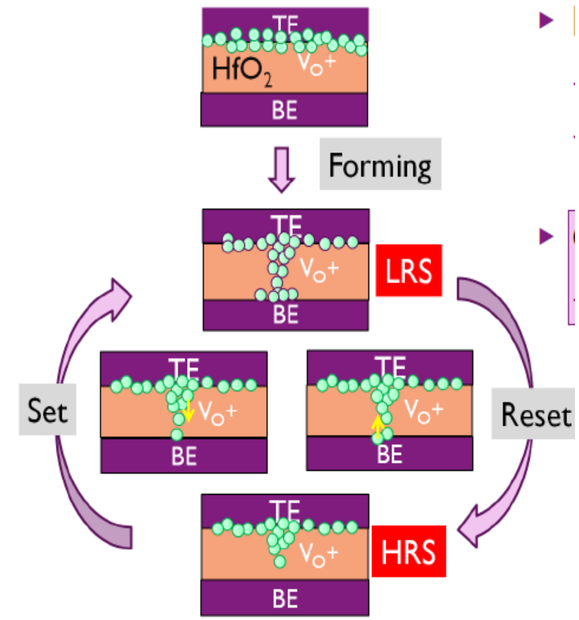
R2RAM 1Mbit (RC28F1024R2RAMn)

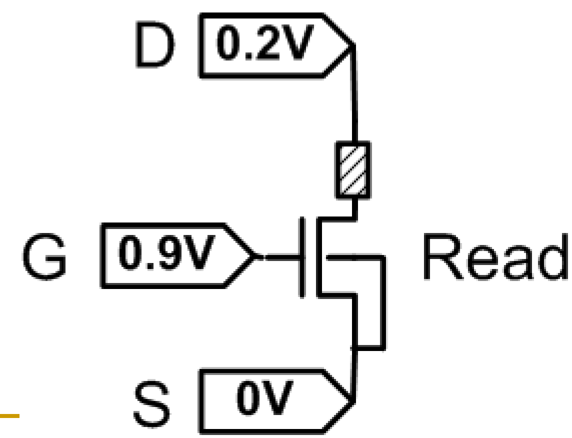
The independence of each bit (independent final stages, ATDs, etc…) guarantees resistance to MBUs.



ReRAM Cell Working Conditions







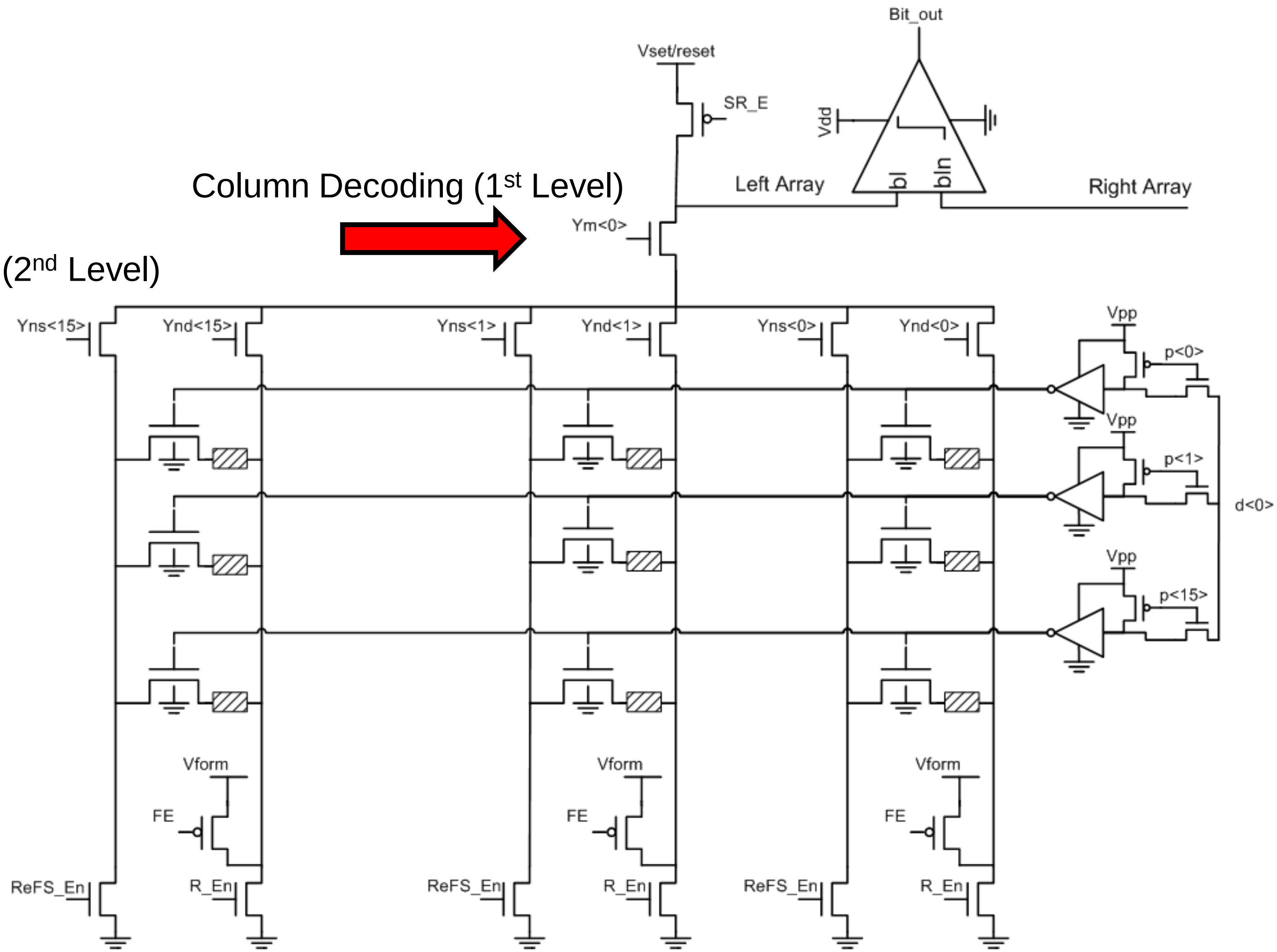
Architectual Approach (16 x 16 Bank)

RedCat Devices

Column Decoding (1st Level)

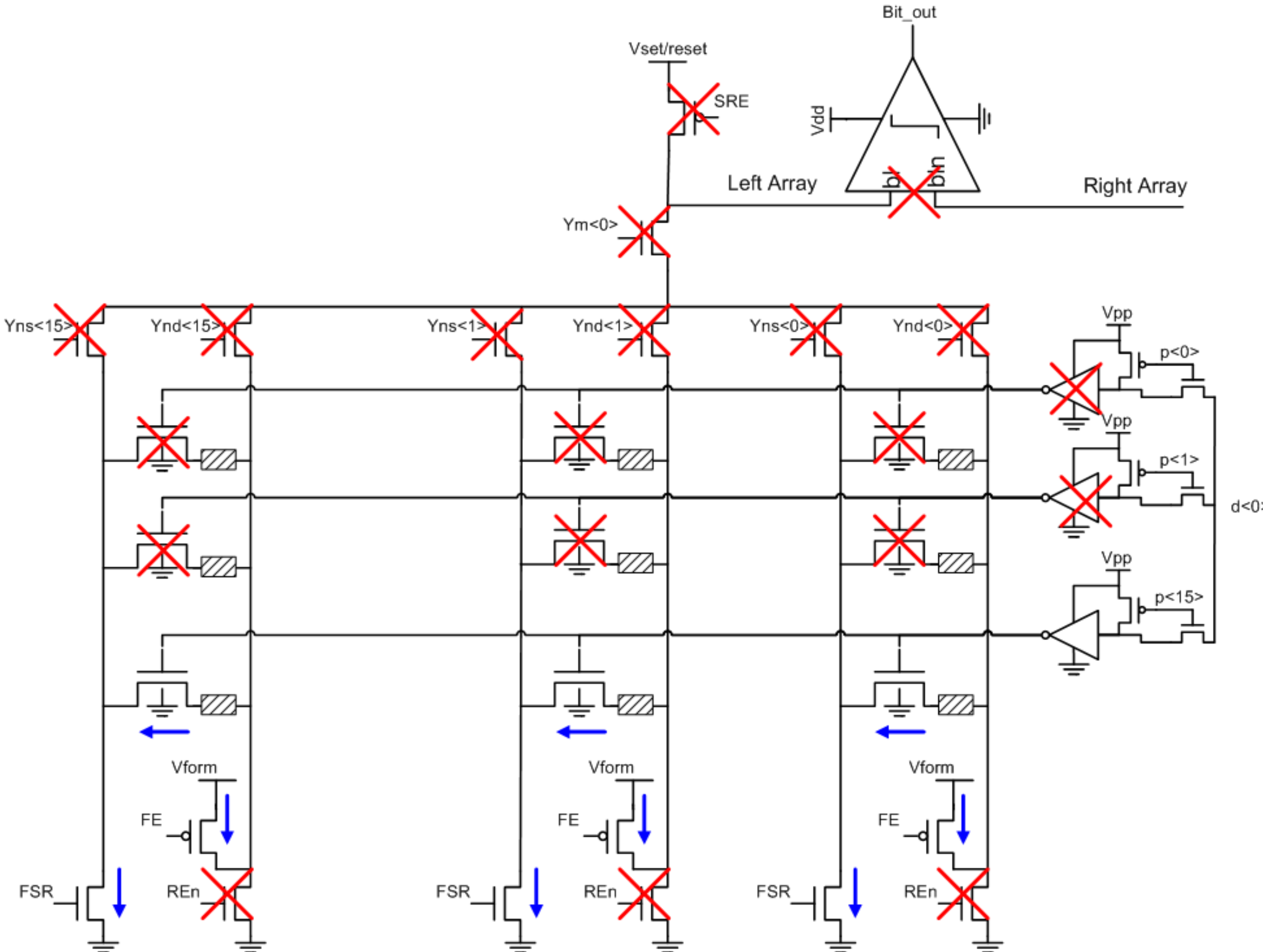
Column Decoding (2nd Level)

Column Control



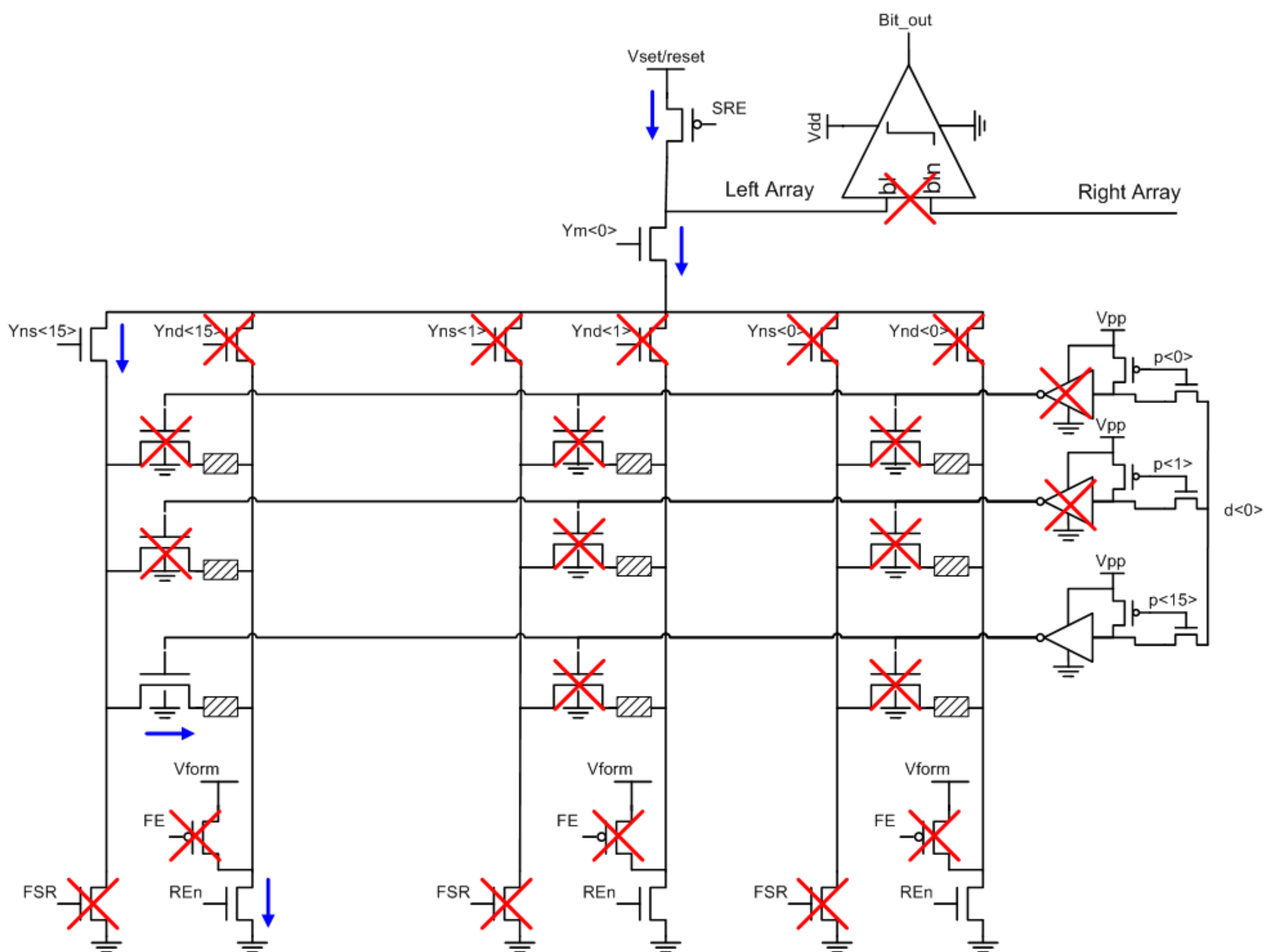
Forming Mode (row by row)

Vset = 0 V
Vdd = 2.5 V
Vpp = 0.9 V
Vforming = 4 V



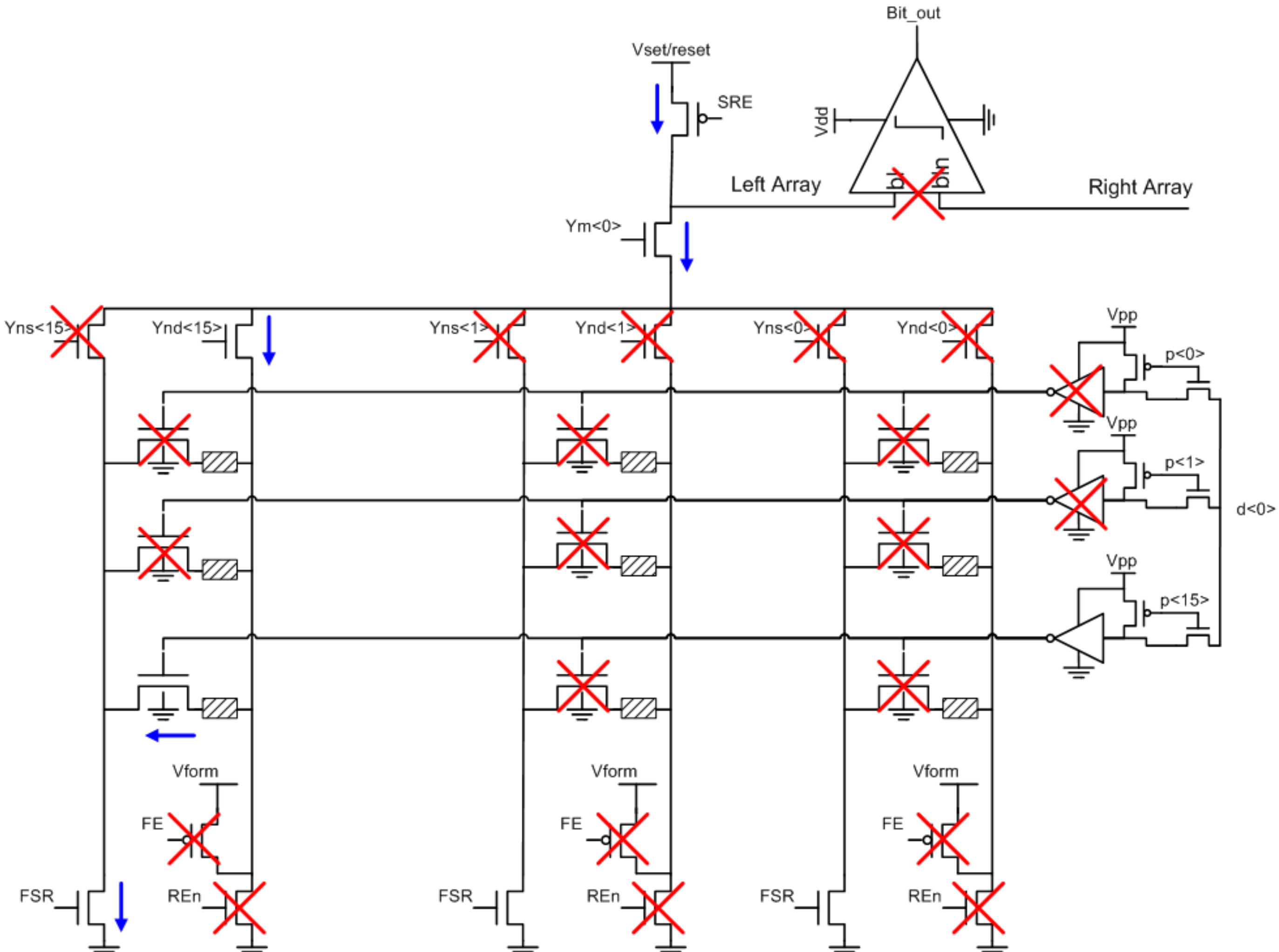
Reset Mode

Vreset = 2 V
Vdd = 2.5 V
Vpp = 2.4 V



Set Mode

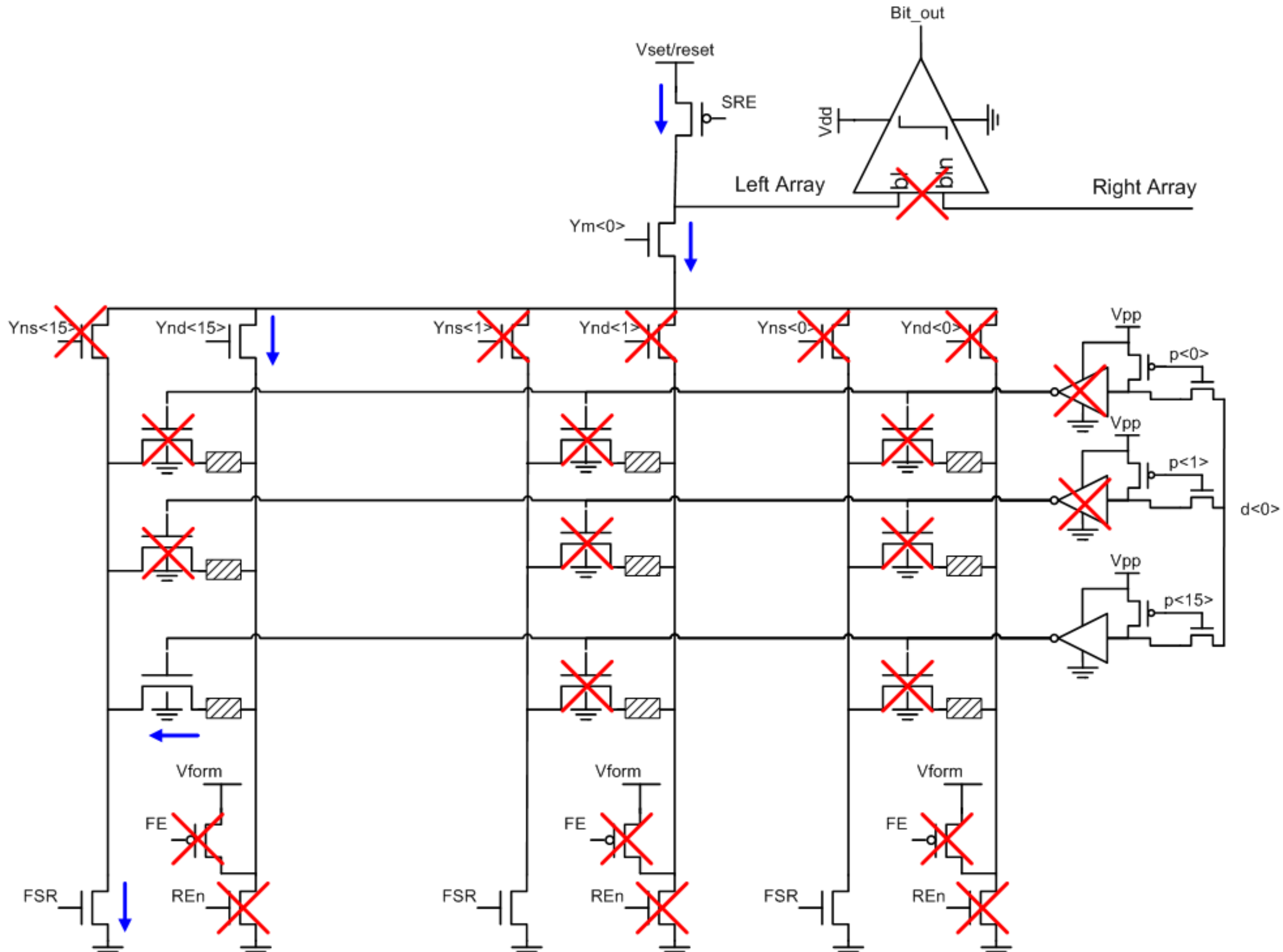
Vset = 2 V
Vdd = 2.5 V
Vpp = 0.9 V



Forming Mode (cell by cell)

RedCat Devices

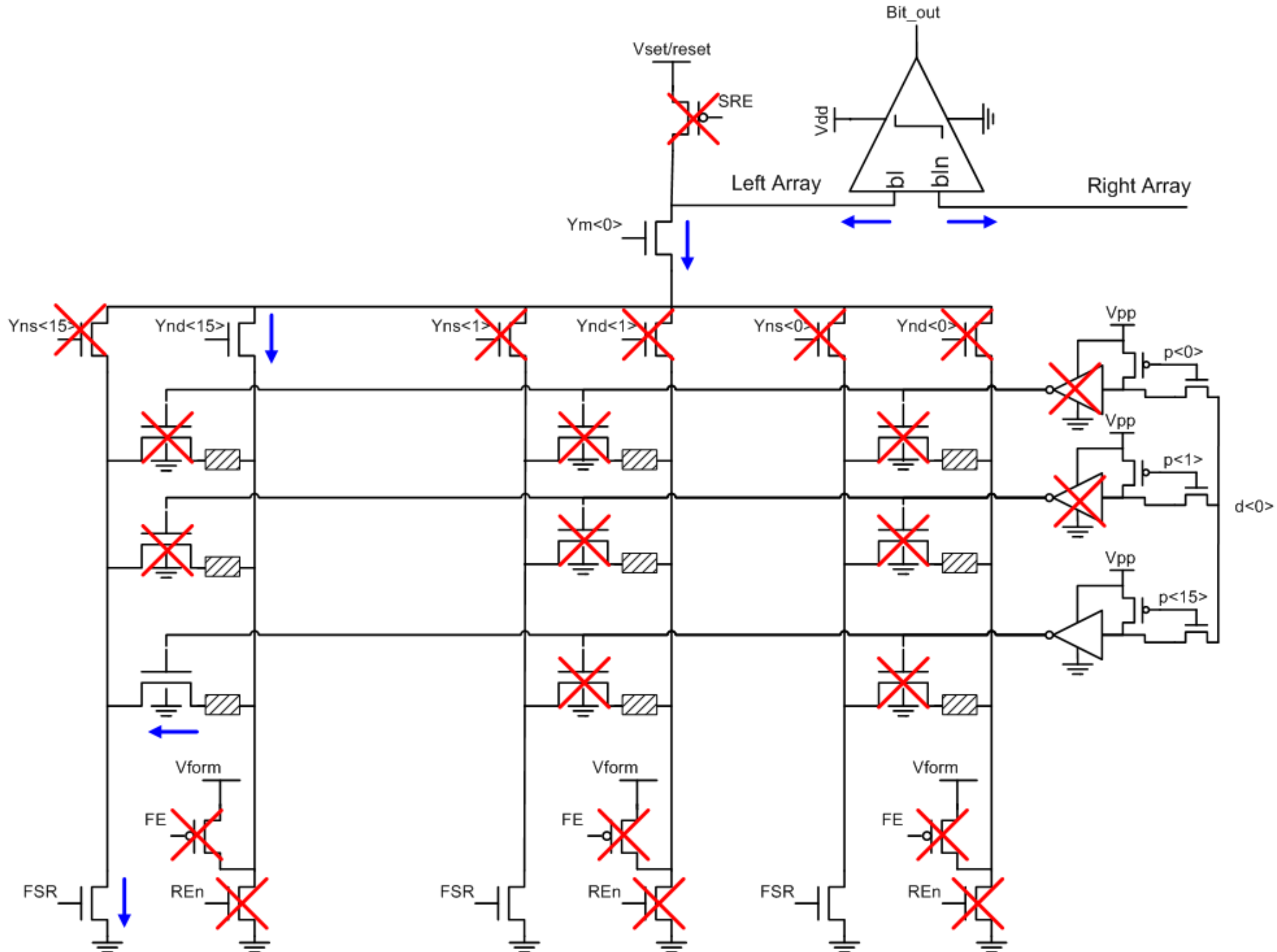
Vset = 3 V
Vdd = 3V
Vpp = 0.9 V



Read Mode

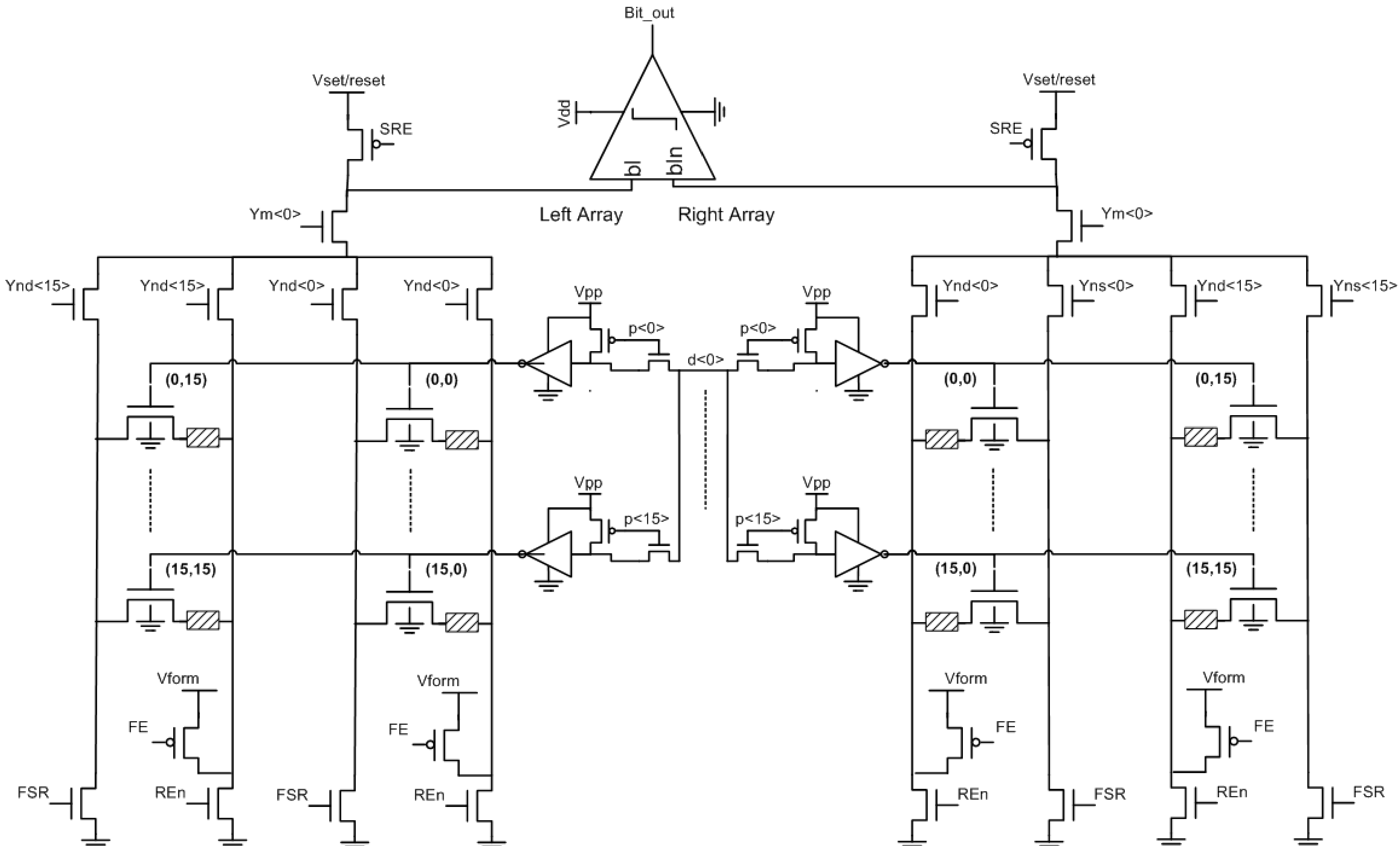
RedCat Devices

Vset = 0 V
Vdd = 2.5 V
Vpp = 0.9 V

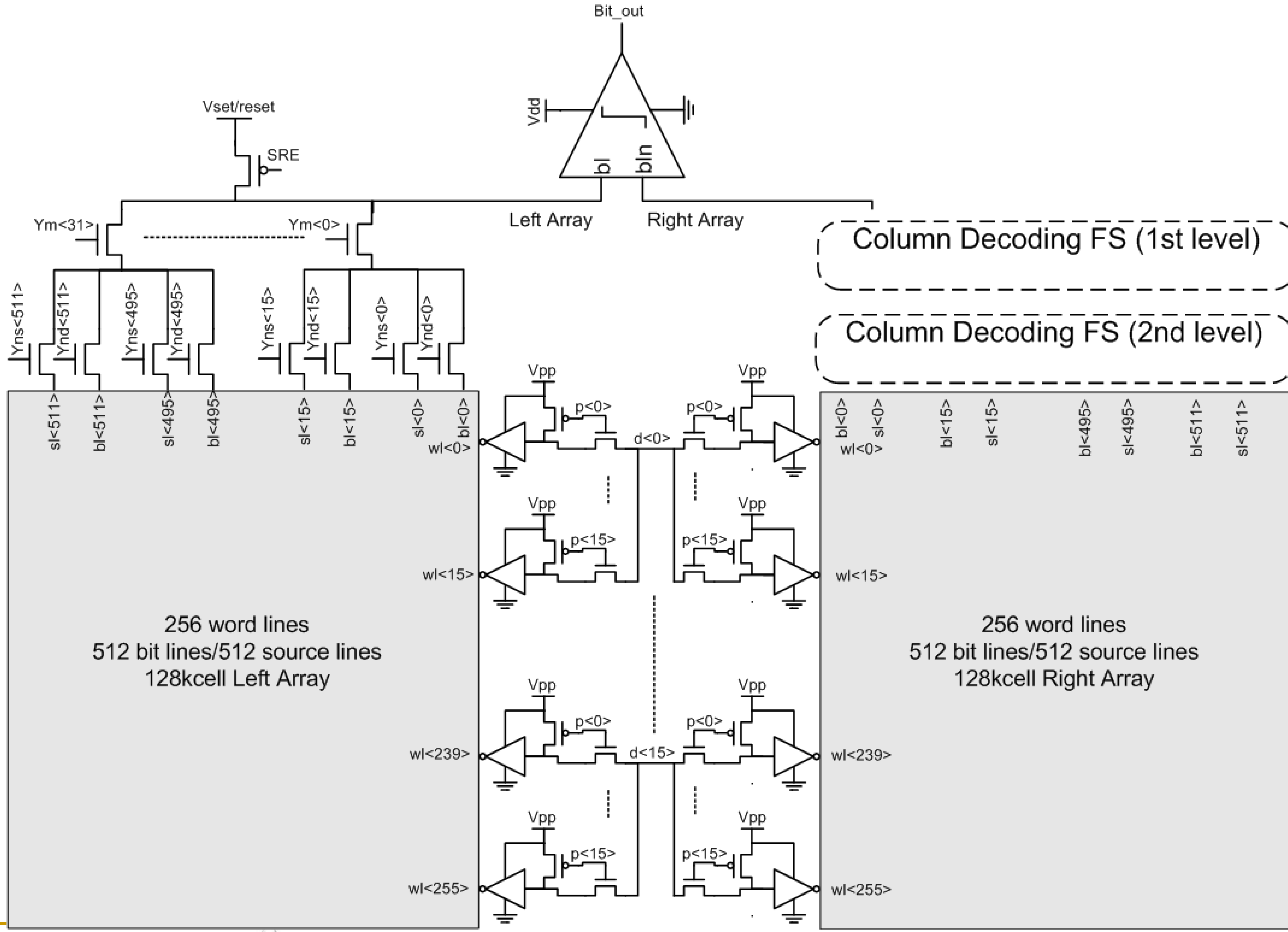


16 x 16 Differential Bank

RedCat Devices



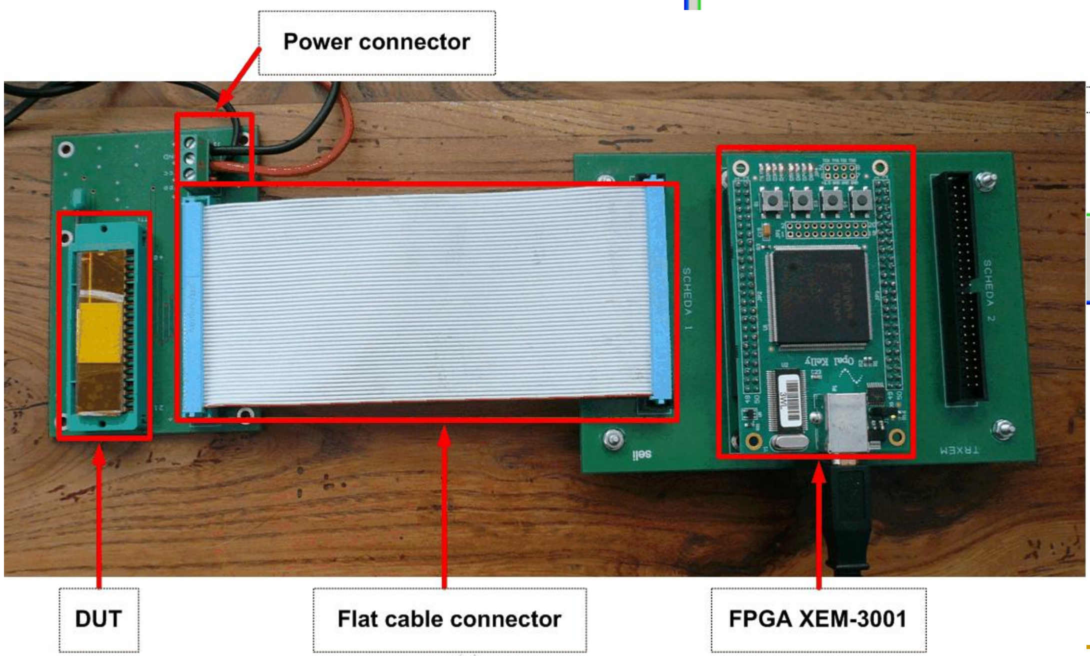
128kbit Differential Block

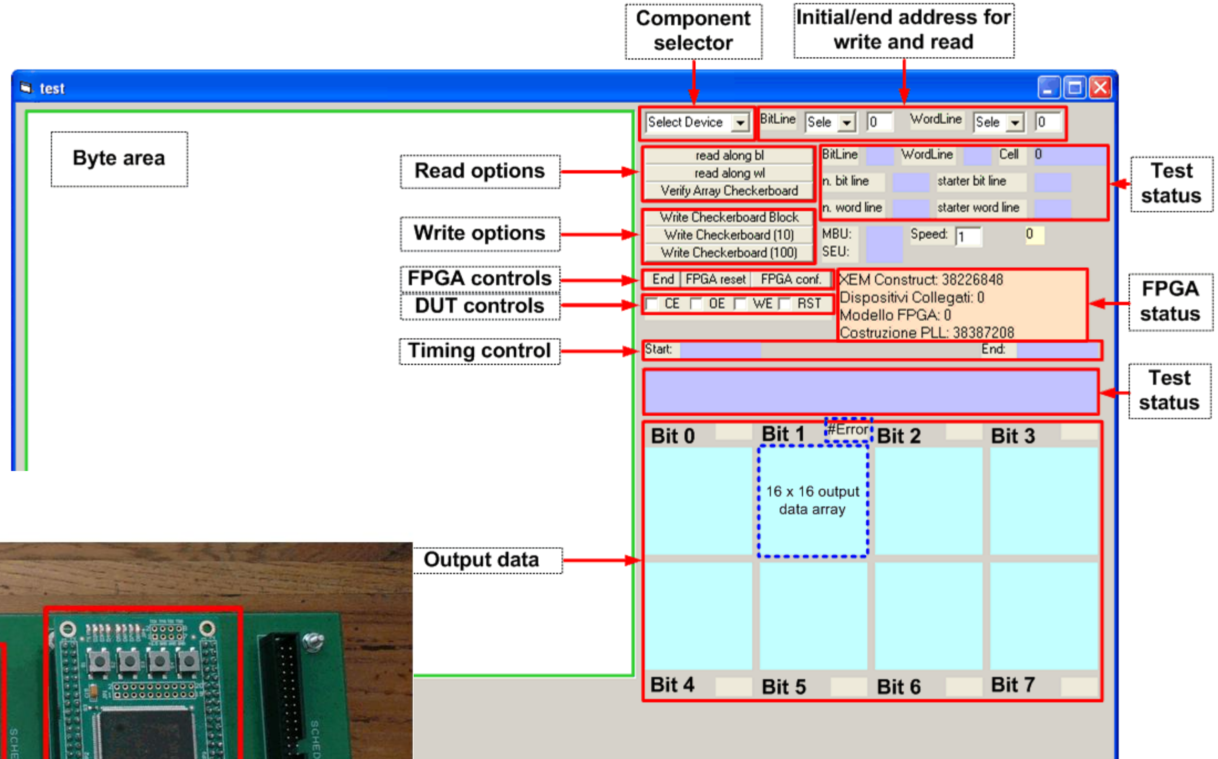


Testing Equipment

RedCat Devices

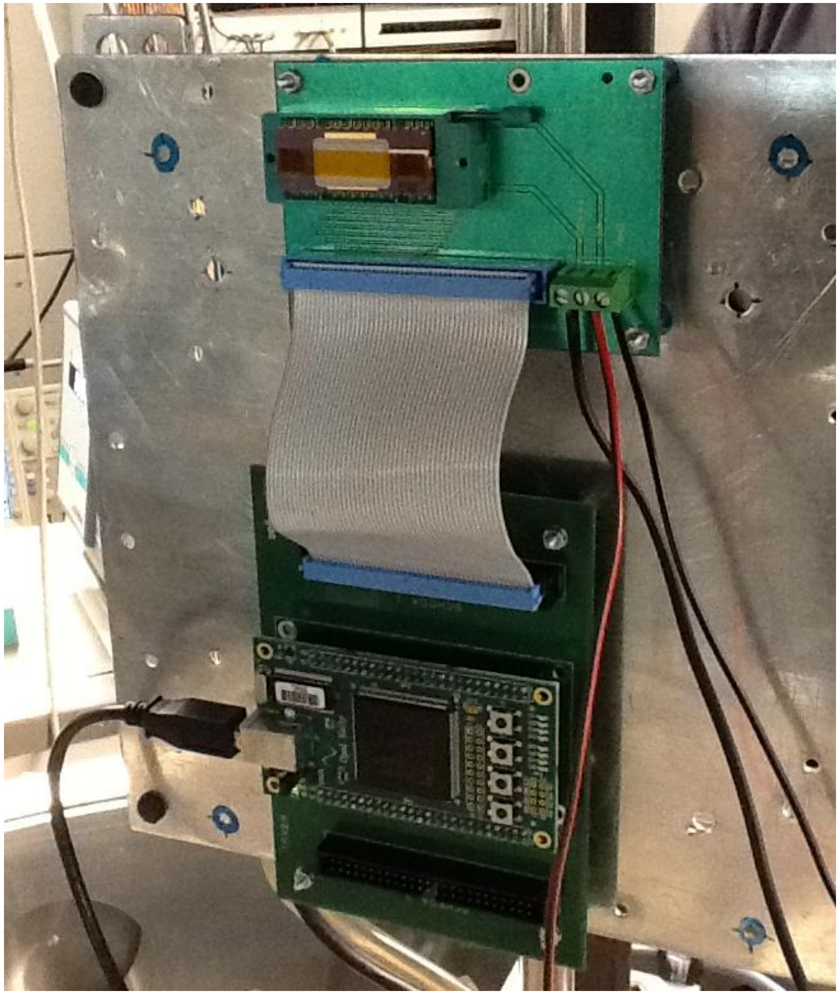
Hardware Based on Xilinx Spartan FPGAs

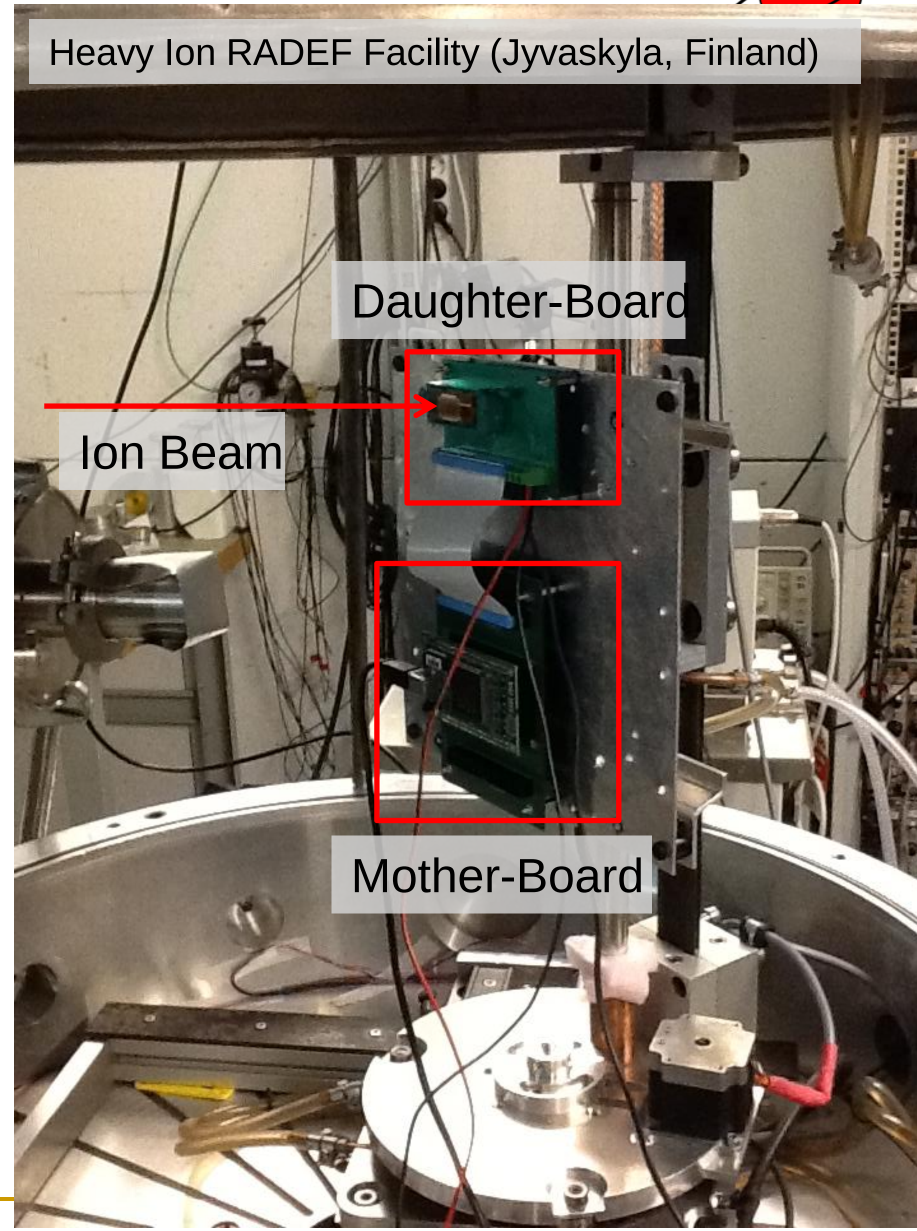




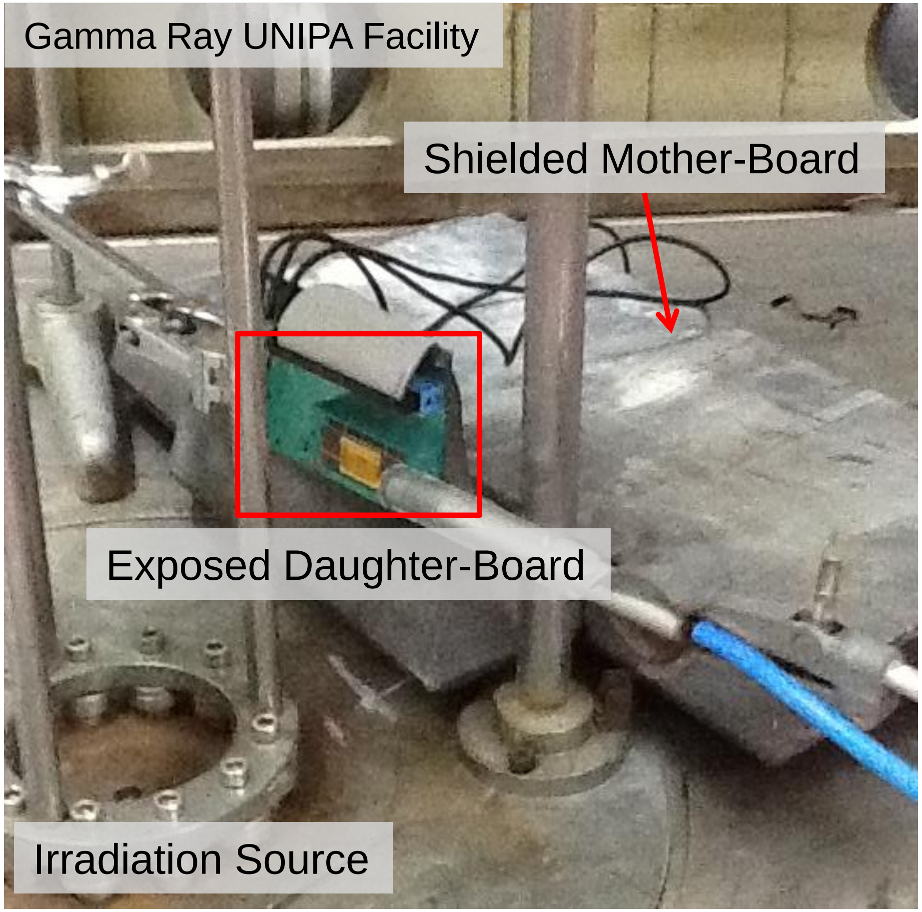
Software Based on Verilog and VB

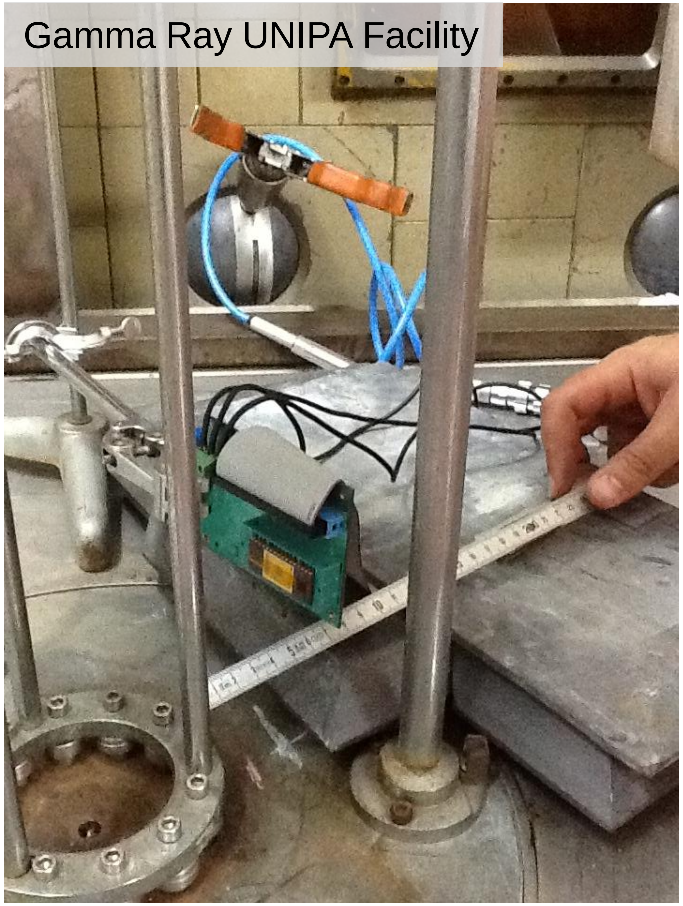
Testing Equipment (SEE)





Testing Equipment (TID)

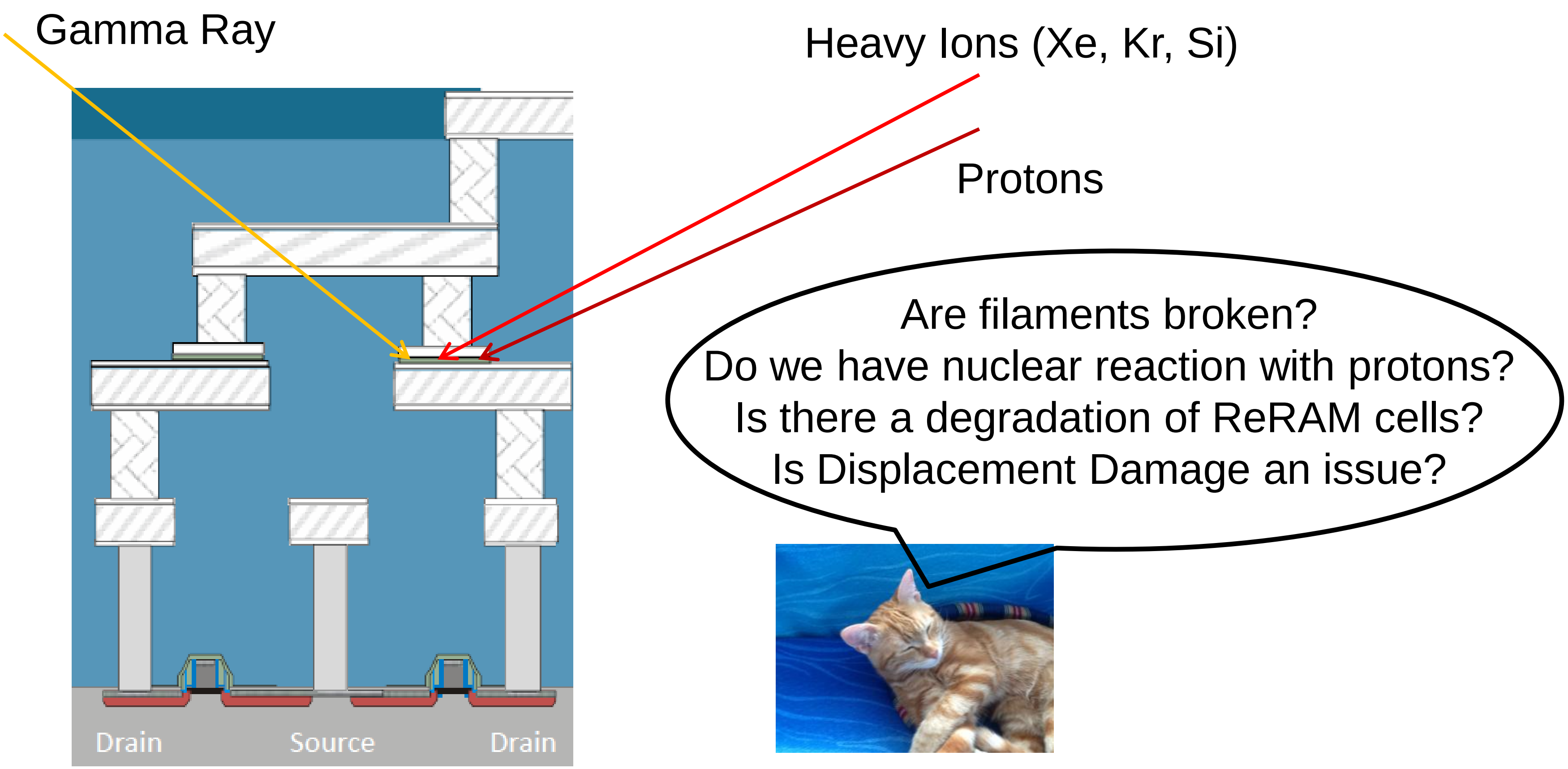




Some questions looking for an answer

RedCat Devices

Problem N° 1: Effect of heavy ions on ReRAM!
Problem N° 2: Effect of protons on ReRAM!
Problem N° 3: Effect of gamma on ReRAM!



Thanks for your Attention!!