The development of EGSE COTS products for high-speed O/B interfaces for advanced spacecraft and instruments

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ABSTRACT

In this paper a flexible and reconfigurable approach in the development of EGSE Front-Ends for high-speed O/B spacecraft and instrument interfaces is presented. These Front-End platforms can easily be adapted to different electrical interfaces (like Wizardlink, SERDES and LVDS), but they can also be tailored to different industry standard and customer specific protocols. This approach is described in detail based on use cases of our Wizardlink-based EGSE Front-Ends. These have been in operation at many European system integrators and instrument developers, for example in the Sentionel-1 programme where SSBV developed and delivered the SAR Data Simulator (SDS) and Mass Memory Storage Unit (MMSU) Simulator based on Wizardlink. Finally, the migration of our Front-End platforms towards likely future industry standards such as SpaceFibre is addressed.

INTRODUCTION

With the increase of bandwidths within satellite payload systems, there is a demand for high-speed data interfaces on-board satellites. Where in the past a SpaceWire, PacketWire or even ML16/DS16 interface provided sufficient bandwidth to transport data across from a payload to subsequent data processing units or on-board memory, the threshold has been pushed for data rates reaching up to 2Gbps and beyond. In order to meet these high bandwidths, on-board equipment designers now incorporate high bandwidth interfaces such as parallel LVDS, SERDES and Wizardlink into their subsystems.

Over the last 2-3 years SSBV has extended its wide range of EGSE/SCOE equipment to support these types of high-speed interfaces as standard products. The existing SSBV range of high-speed front-end acquisition systems now include support for Parallel LVDS, SERDES and Wizardlink as part of their standard portfolio, with the option to expand to new standards like SpaceFibre. These products have been designed to provide a flexible solution that can be rapidly adapted such that the front-ends can support customer specific protocol layers as nominally implemented on SERDES and Wizardlink interfaces. In addition to their core functionality, SSBV have specifically designed these products to support the low level AIT needs of both instrumenters and spacecraft integrators for example the retention of lower layer protocol levels such as Wizardlink data (D-Code) and special characters (K-Code).

In this paper the two generations of EGSE front-ends that provide Wizardlink as protocol interface are described. Additionally the linkage into other on-board high speed interfaces such as Parallel LVDS, SERDES, Spacewire and the future SpaceFibre is discussed.

FIRST GENERATION WIZARDLINK FRONT-END

Wizardlink is a multi-gigabit transceiver family from Texas Instruments that provides a high-speed bi-directional point-to-point baseband data transmission interface between systems on a controlled impedance media of 50Ω. From this family the TLK2711 [1] is used on-board in various spacecraft's. The TLK2711 provides the physical interface and performs parallel-to-serial and serial-to-parallel conversion. The parallel interface is a 16-bit wide bus that is internally encoded into 20bits using 8b/10b coding. The resulting 20-bit data is transmitted (or received) differentially at 20 times the reference clock rate using Voltage Mode Logic (VML) as electrical interface standard.

The first generation of the Wizardlink Front-End was developed by SSBV in 2008 and has been used on the Sentinel-1 programme. This programme used various EGSE systems, under which the SAR Electronics Subsystem (SES) EGSE to Astrium Portsmouth, the Data Storage & Handling Assembly (DSHA) EGSE to TAS-I Milan and the Payload Data Handling and Transmission (PDHT) EGSE to TAS-I Rome.

In Sentinel-1 Wizardlink (1.6Gbps link rate) is used to interface between the SAR instrument, providing the horizontal polarisation and vertical polarisation outputs (payload data) from the radar, and the MMSU (Mass Memory Storage Unit). The payload data from the SAR instrument are CCSDS packets transmitted over two independent Wizardlink interfaces, one for each polarisation. The MMSU is a sub-unit in the DSHA, where the DSHA together with the X-Band Transmission Assembly makes the PHDT.

For SES the MMSU Simulator was defined, capable of receiving, processing and storing the two Wizardlink data streams as output by the SAR instrument. For DSHA and PDHT the SAR Data Simulator was developed, capable in the transmission of two Wizardlink data streams. These two simulators were developed using a single hardware platform which later became the first generation Wizardlink Front-End.

The development of the Wizardlink hardware platform was driven by two major requirements:

- The physical distance between the UUT (on-board equipment/sub-systems) and the overall EGSE should be at least 30 meters
- The coaxial cable used should be commercially available

In order to guarantee the required minimum signal eye-opening by a Wizardlink receiver the choice was made to use fibre optics to bridge the required physical distance between the EGSE equipment rack and the UUT. Choosing fibre optics will require the signal to be converted back to Voltage-Mode Logic (VML) [2] as used by Wizardlink. A significant benefit of using fibre optics is that it allows galvanic isolation between the spacecraft high speed interfaces and the remainder of the EGSE.

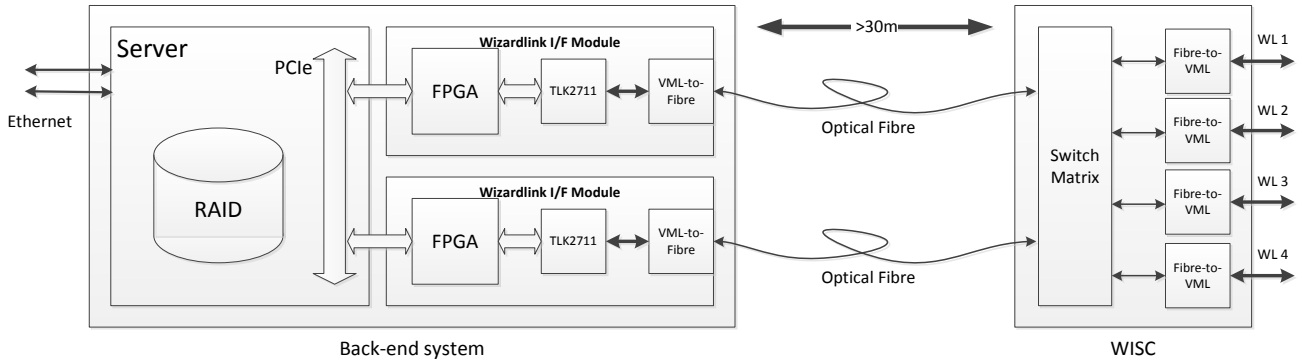

Fig. 1. Wizardlink Front-End Hardware Platform (First Generation)

The architecture of the Wizardlink FE platform is shown in Fig. 1. The Wizardlink I/F Module (WIM) is an in-house developed PCI express card (Fig.2). It is plugged in a commercially available server (i.e. the back-end system). Two WIMs are fitted in the server to support two independent Wizardlink interfaces for the various Sentinel-1 EGSEs. The data to and from the UUT are transferred from and to a RAID through the server's PCIe bus.

The WIM features a Wizardlink Chipset (based on TLK2711), an FPGA for pre and post processing the data, supporting the protocol levels as used by Sentinel-1. Additionally received data can be accurately time stamped and data to be transmitted can be accurately released on a packet to packet base. The time as internally kept in the hardware is in CUC (CCSDS Unsegmented Code) format, synchronised by an externally provided PPS. The VML in- and output of the Wizardlink chipset is converted to fibre using commercially available fibre optic transceivers.

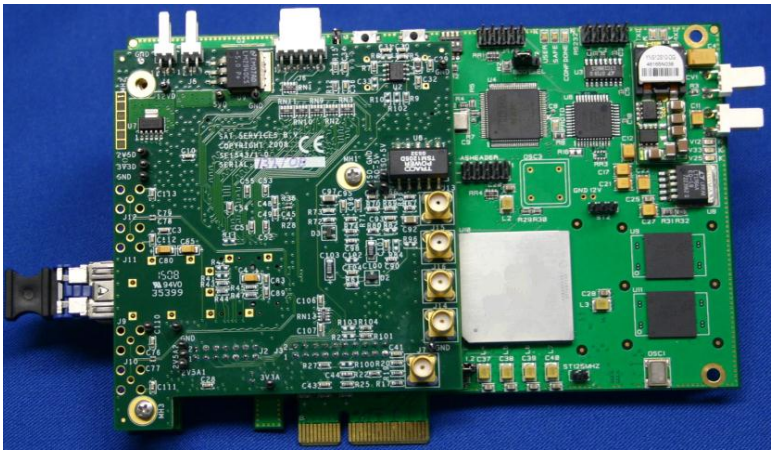

Fig. 2. Wizardlink Interface Module

A separate unit, the Wizard Interface Selection & Conversion (WISC) unit has been developed (Fig. 3) to convert the optical data back to VML, which is the Wizardlink electrical interface used in the Sentinel-1 subsystems. Next to signal conversion the WISC also provides a switch matrix to switch between different VML input and outputs to and from the UUT.

The Wizardlink Front-End is controlled and monitored through a Graphical User Interface offered by the joint SSBV/TERMA product for low-latency instrument- and payload checkout: the Control, Monitoring, Data-processing & Visualisation Software (CMDVS).

The platform as provided by the first generation Wizardlink Front-End allowed easy adaption to support customer specific higher level Wizardlink protocol handling directly in hardware (firmware) without an impact on hardware architecture.

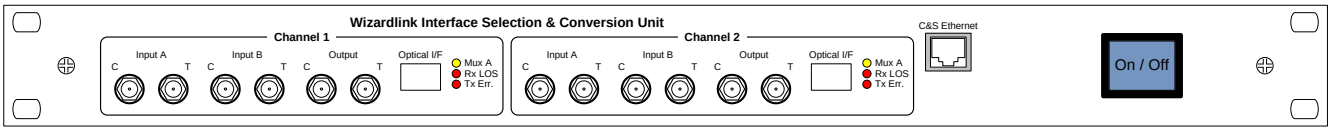

Fig. 3. Wizardlink Interface and Selection Unit

SECOND GENERATION WIZARDLINK FRONT-END

With the success of the first generation Wizardlink Front-End hardware platform in the Sentinel-1 program, in 2011 SSBV decided to evolve the platform that became the second generation Wizardlink Front-End. From the experiences gained during the development and operational phases of the first generation Wizardlink Interface Front-End a list of improvements have been defined:

- Provide failure mode protection of the Wizardlink interface (due to a flaw at the input stage of the TLK2711)..
- Support RAW link acquisition of the Wizardlink Interface (i.e. the retention of D- and K-codes).
- Include the possibility of "link teaming" of high-speed data transfers over multiple Wizardlinks.
- Allow for different electrical interfaces instead of fibre optics only.

- Design a generic and flexible hardware platform that would allow easy extension to other high-speed on-board interface standards like Parallel LVDS, SERDES, SpaceWire and the future SpaceFibre.

With the above in mind a new architecture was specified that maintained the split between front-end (the electrical/physical interface to the UUT, previously the WISC) and back-end. However all data processing, protocol handling, time stamping and formatting would be moved to the front-end side. This meant that the back-end would only function as a data ingestion/transmission platform (with large storage capabilities in the form of RAID arrays). This architecture would of course allow offline (post) processing after ingestion to disk.

The front-end side provides the electrical interface to the UUT, but also perform all pre and post data processing functions on the data stream in FPGA. This would provide the means to easily adapt data processing, protocol handling, time stamping and formatting according to customer requirements without a hardware re-design.

Further, it would be preferable to have a flexible design which can easily be adapted to other electrical interfaces without having to re-design the complete front-end.

The second generation Wizardlink Front-End platform is implemented in a High-Speed Baseband (HSBB) module, a double Eurocard module which fits in a 2U 19" rack mountable unit. This HSBB implements all interface, control/status, data routing/formatting and baseband processing functions. For physical/electrical interfacing, mezzanine modules can be fitted on top of the HSBB that provides the actual I/O interfaces to the UUT.

A second generation Wizardlink Front-End EGSE has been deployed with three Wizardlink interfaces. For flow control purposes, each Wizardlink interface is equipped with two optional 3.3V compliant LVDS flow control input and output signals. Each Wizardlink interface can operate in single or bidirectional mode. The Wizardlinks can be clocked synchronously or independently. The data processing, time stamping, buffering, alignment, packing, etc. is executed on incoming and outgoing data streams in FPGA on the HSBB. As all three Wizardlink are interfacing to a single FPGA this provides the means of link teaming (i.e. multiple lanes).

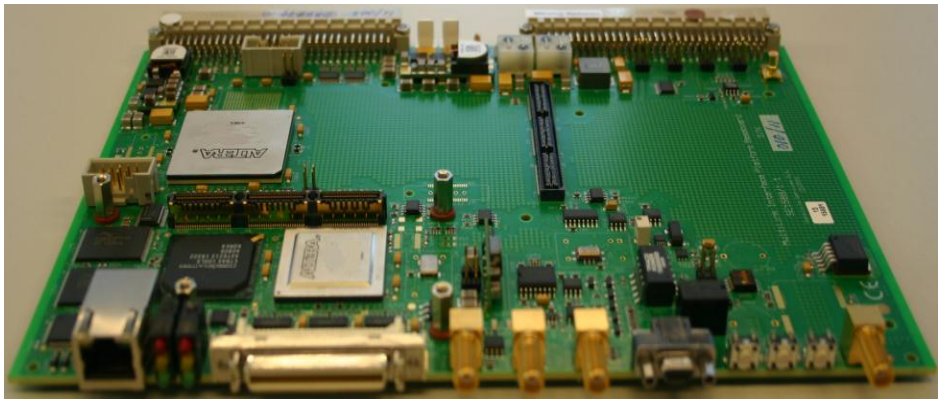

Fig. 4. High-Speed Baseband Module

Along with the development of the second generation Wizardlink Front-End, in 2012 SSBV upgraded also the performance of data ingestion and processing hardware to be able to cope with the data rates and amount of data to be acquired and processed. As standard interface between the HBSS and the back-end data ingestion platform a dedicated Gigabit Ethernet Interface optimized for data streaming

has been specified. The HBBS can stream the data to and from the back-end server through up to three Gigabit Ethernet ports, each capable of streaming data out up to 800Mbps sustained (bi-directional).

Fig. 5 shows the block diagram of a second generation Wizardlink Front-End as it is currently being deployed, and Fig. 6 shows a picture of the system, including data ingestion platform.

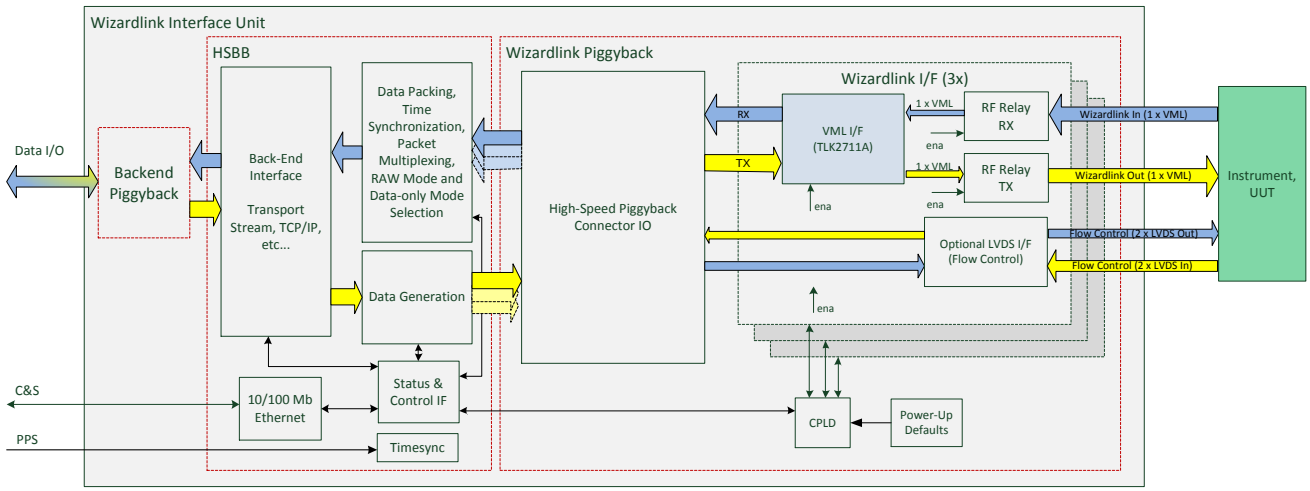

Fig. 5. Wizardlink Interface Module Block Diagram

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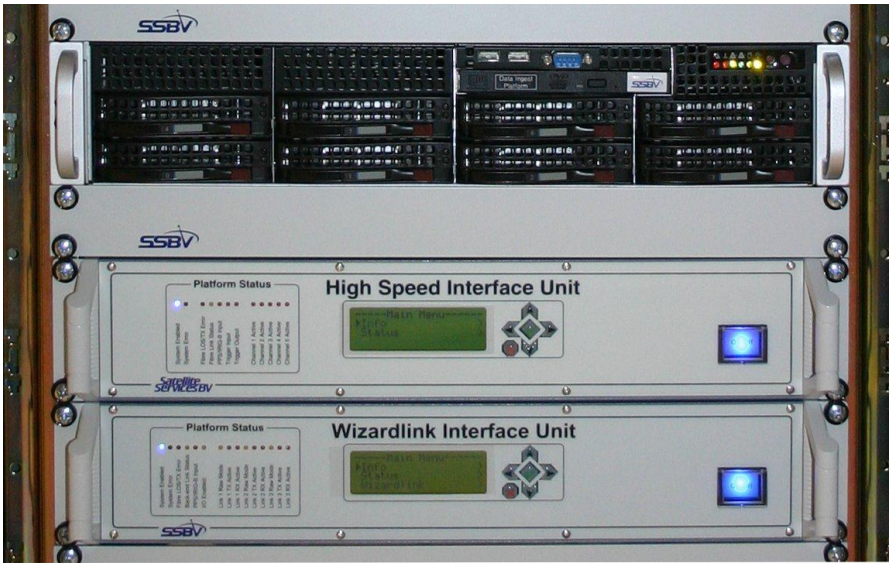


Fig. 6. Picture of a deployed second generation Wizardlink Front-End.

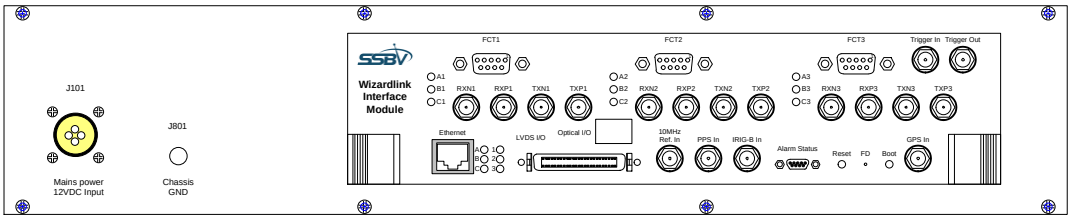
OTHER HIGH-SPEED FRONT-ENDS

As described in the previous section, the development of the second generation Wizardlink Front-End provided a hardware platform that allows relatively easy expansion to other high-speed front-ends using different electrical interfaces by replacing the interface mezzanines as fitted in the HSBB.

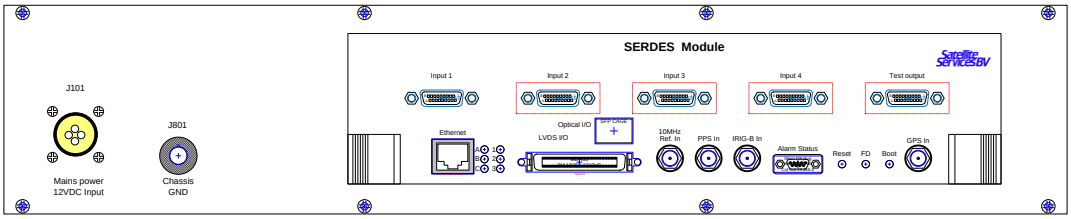
In order to support a large amount of other satellite programmes using high-speed interfaces (for example AS250, Sentinel-2, EarthCARE, SeoSAT, GAIA, etc…) for which SSBV has provided EGSE, the current portfolio of high-speed front-ends using the same hardware platform are:

- Wizardlink Interface Unit (Texas Instruments TLK2711)
- SERDES Interface Unit (Aeroflex UT54LVDS217)
- High-Speed Interface Unit (Parallel LVDS)
- Spacewire Monitor Interface Unit (Serial LVDS)

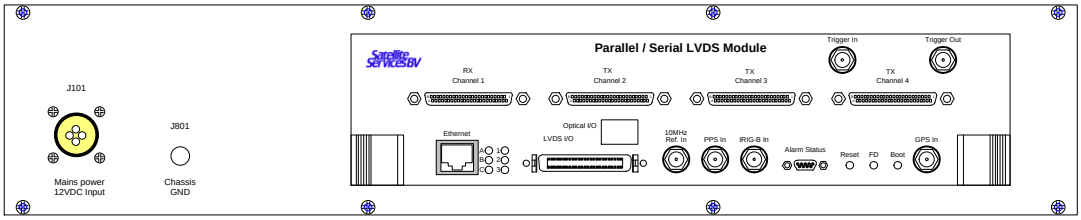
Fig. 7 shows the rear-panel view of the interface units listed above.



(a)



(b)



(c)

Fig. 7 Rear panels of Wizardlink Interface Unit (a), SERDES Interface Unit (b) and Parallel LVDS / Spacewire Monitor Interface Unit (c).

FUTURE HIGH-SPEED FRONT-ENDS

As indicated in this paper, the second generation Wizardlink Front-End platform has been based on a generic and modular approach within SSBV of developing commercial-off-the-shelf high-speed O/B front-end platforms. These high-speed front-ends platforms can easily be adapted to different electrical interfaces (like Wizardlink, SERDES and LVDS) by adding mezzanine interface modules, but they can also be tailored to different industry standard and customer specific protocols. An example is the SpaceWire Front-End platform which uses the same electrical interfaces as the LVDS Front-End platform. Similarly, the Wizardlink platform has been configured by SSBV for user and instrument specific protocols.

This allows an easy expansion of these high-speed O/B front-ends with new industry standards. For example, a currently activity of ESA is the specification SpaceFibre, a new high-speed O/B interface standard for data rates beyond 2Gbps as a successor of the successful SpaceWire standard [3]. SpaceFibre carries SpaceWire packets over virtual channels and provides a broadcast capability similar to SpaceWire time-codes but offering much more capability. SpaceFibre can run over fibre optic or copper media. The aim of SpaceFibre is to provide point-to-point and networked interconnections for very high data-rate instruments, mass-memory units, processors and other equipment, on board a spacecraft.

One of the recommended implementations of serialisation and physical layer of a SpaceFibre single-lane over copper is the TLK2711 Wizardlink. Higher layers of the SpaceFibre protocol allow the usage of multiple lanes ("link teaming") to increase the data speed. Using the Wizardlink electrical interfaces in our Wizardlink Front-Ends and implementing the SpaceFibre protocol (CODEC) in the FPGA, allows for a seamless migration to a SpaceFibre over Wizardlink Front-End. Replacing the Wizardlink mezzanine interface module with an appropriate optical mezzanine interface module results with a limited effort and low risk in a SpaceFibre over Fibre Optic Front-End.

This shows the benefit of our approach in designing a flexible platform that can be rapidly adapted such that the front-ends can support industry standard and customer specific protocol layers as well as different electrical and physical layers.

References

[1] Texas Instruments, "*TLK2711-SP 1.6-Gbps to 2.5-Gbps Class V Transceiver,*" Texas Instruments, Datasheet SGLS307E, July 2006 – Revised November 2011.

[2] N. Holland, "*Interfacing Between LVPECL, VML, CML, and LVDS Levels,*" Texas Instruments, Application Report SLLA120, December 2002.

[3] SpaceFibre Standard Draft D, ECSS-E-ST-50-XXX, 29th February 2012