AMICSA & DSP 2016

ESA Round Table on DSP and FPGA

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Synthesis

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Purpose of the Document

The purpose of this document is to present a synthesis of the discussions that took place during the ESA Round Table on DSP and FPGA as part of the 2016 ESA DSP Day that was organized in conjunction with AMICSA.

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1 Background

The ESA Round Table 2016 on "DSP and FPGA" was held at the Radisson Blue Hotel in Gothenburg, Sweden in the frame of the AMICSA & DSP 2016 event on June 16th, 2016. The purpose of the Round Table was to

i) Organize a discussion and receive feedback from European industry and academia on their view on the future need for DSP ASICs versus need for FPGAs in support of future space applications

ii) Organize a discussion and receive feedback from European industry and academia on their view on the need for the integration of FPGA fabric in future data processors (in particular DSPs, but also General Purpose Processors or GPPs)

iii) Invite participants from European industry and academia to state their views, ideas and concerns with respect to other topics related to space based digital signal processing

For stimulating the discussion, the following materials were presented:

- Paper and presentation on: "DSP and FPGA: Competition, Synergy, and Future Integration in Space ASICs" [1]
- Presentation of the current status of relevant R&D activities at ESA (DSP IP cores, NoC developments, DSP ASIC and related software, FPGA developments)
- A set of questions to trigger and focus the discussion and expression of opinions from participants

All presented materials can be downloaded from the "timetable" section of the AMICSA / DSP 2016 website [2].

ESA was very pleased to welcome 53 attendants to that Round Table which were representing the European space community (industry, space agencies and academia) as well as one company from Israel.

2 DSP and FPGA: Motivation for the DSP Day Round Table Discussion

After the ESA Round Table on "Next Generation Processor for On-board Payload Data Processing Applications" in October 2007 [3], ESA has pursued several development routes in parallel. For DSP ASICs, several developments were followed in parallel:

- Next Generation DSP (NGDSP) development based on ADI's 21469 commercial DSP design (abandoned due to lack of funds)
- Massively Parallel Processor Technology, resulting in the Scalable Sensor Data Processor ASIC development (ongoing, EMs expected in 2017, and FMs expected in 2018)
- High Performance Data Processor, an array processor ASIC aiming at telecom applications (prototype development ongoing, first chips expected 2017)

In addition to data processor ASIC developments, the utilization of reconfigurable FPGAs for high performance data processing was also investigated via the following activities:

- DRPM (Dynamically Reconfigurable Processing Module), and effort aiming at the evaluation of reconfigurable FPGA technology for data processing applications via 2 parallel contracts

Since then, reconfigurable FPGAs have become available and popular for space applications, many of the associated problems have been addressed, and FPGAs have therefore become a viable competitor to processor ASICs in many areas. Also in Europe, significant investments are being made in reconfigurable FPGA technology, and first prototypes are already being tested.

From an R&D management point of view, including but not limited to budget considerations, the question arises whether DSP ASICs and reconfigurable FPGA development lines should both be maintained in parallel, or whether one technology provides superior performances in a sufficient number of application cases to justify prioritizing the technology over the other. On the other hand, commercial trends to combine hard-wired ASIC technology with FPGA fabric on the same chip also exist, and the integration of both technologies into a DSP / FPGA 'Hybrid' may allow to combine the strengths of both technologies, a point of view advocated in the ESA introduction paper [1].

Given the constraints in ESA R&D funding, and the importance of making the right decisions today in order to deliver the right chips 10 years from now, the ESA DSP Day 2016 round table was organized to collect the views of industrial and academic representatives related to the topic of DSP ASIC vs. FPGA.

The following chapter describes the presentations and discussions that took place at the ESA DSP Day 2016 Round Table.

3 Round Table Discussions: DSP and FPGA

The discussion was preceded by the presentation of a paper ("DSP and FPGA: Competition, Synergy, and Future Integration in Space ASICs", [1]) authored by ESA stakeholders which summarizes advantages and disadvantages of traditional DSP ASICs and re-configurable FPGAs, and illustrates possibilities for synergies in future SoC designs via an example many-core DSP design that integrates on-chip FPGA fabric. The presentation as well as a dedicated viewgraph on related ESA technology developments (in the areas of DSP cores, NoC IP, FPGA IP, and software) illustrated the available technology background in Europe. The audience was then presented with the following questions for seeding the Round Table discussion:

1. How do you see the future shares of rad-hard (DSP) ASICs and (rad-hard / rad-tolerant) FPGAs in payload data processing ?
2. How attractive would you consider a high performance payload processor chip that combines GPP/DSP cores with on-chip FPGA(s) ?
3. What are your expectations for the utilization of COTS DSPs and COTS FPGAs in future space data processing applications ?

Additional questions from the audience were invited as well. Speakers were encouraged to address any or all of the proposed questions, ask any of their own, and state opinions on relevant related topics. The following paragraphs summarize the essence of discussions and opinions grouped into topics; they do therefore not reflect the temporal sequence of discussions. Table 1 shows the acronyms used to indicate the company affiliation of discussion contributors.

EI	Enterprise Ireland, Ireland
TAS	Thales Alenia Space (several locations)
AB	Airbus Space & Defence (several locations)
SSC	Swedish Space Corporation, Sweden
A/M	Atmel / Microchip, France
RC	Ramon Chips, Israel
CBK	Centrum Badan Kosmicznych PAN, Poland
DCU	Dublin City University, Ireland
CG	Cobham Gaisler, Sweden
UoD	University of Dundee, UK
SY	Syderal, Switzerland

Table 1: Acronyms used for company affiliations of DSP Round Table participants

Discussion Topic: ASIC vs FPGA

TAS: ASIC and FPGA solutions are not mutually exclusive and there is a need and room for both. For the future we expect a combination of both in many application cases. A combination will allow to achieve high performance, but also standalone FPGA solutions are attractive and provide flexibility.
RC: Our investigations indicated that the companies - including primes, both inside and outside Europe, want to move away from hard-wired ASICs and FPGAs, towards powerful re-programmable DSP architectures. This is why we went into that direction with RC64.
AB: For very high performance data processing our European FPGAs are not sufficient and we need to consider DSP ASICs / massively parallel architectures in Europe, unless we go for COTS FPGAs.

Discussion Topic: FPGA integration in Processor ASICs

UoD: Flexibility for I/Os is very important and desirable, and FPGA fabric as part of devices could provide this functionality. For the architecture concept shown on the slides [1], a patent search might be advisable to identify potential IP constraints.
SSC: Addition of a small FPGA into a processor device is a good idea. Sometimes designers find that they need a small addition to the design and with today's fixed-functionality ASICs this leads to the addition of an external FPGA device.
CG: There is always a need to add an FPGA to a board design to implement interfaces etc. not present on the chosen ASICs. On-chip FPGA fabric on DSPs and GPPs would be useful to tailor the interfaces to application needs (without adding external FPGAs).
A/M: We have been studying and developing / selling DSP and FPGA in the past. When comparing digital signal processing in DSP/ASIC and FPGA, for similar performances an FPGA needs to use higher integration (FPGA in 28nm is required to match an ASIC in 65nm). When combining hardwired functions and eFPGA on the same chip, the eFPGA fabric will be comparatively slow and not very suitable for high speed data processing. A better combination can be achieved via a Multi-Chip Module (MCM), where the best processor / FPGA combination can be paired. If eFPGA fabric is added on the same chip (with GPP or DSP) it is useful for added logic, to customise processor interfaces. For high speed data processing algorithms you also may need a different (DSP-oriented) FPGA technology.
CBK: Basically every instrument we developed contains a CPU either within an FPGA or as a separate CPU with an associated FPGA. A combined device would be very beneficial for us.
SSC: Other than for COTS components, for rad-hard components the choice in ASICs is quite limited. The more flexibility is available in a rad-hard chip, the more it will be used, and allow larger production volumes.
AB: We agree that on-chip FPGA for enabling configurable interfaces in processors would be useful.
TAS: Integration of FPGA in DSP is considered an attractive feature / solution.

Discussion Topic: FPGAs for Digital Signal Processing

SY: We use FPGAs as a processing resource, and are looking forward to the upcoming European FPGAs. We would like to see partial re-configurability in future European FPGAs.
TAS: For both combined (ASIC and FPGA) and standalone solutions, we are waiting to see the performance of the new European FPGA. For applications that can accept lower reliability we may be able to use COTS FPGAs.
AB: High performance data processing cannot be done with current European FPGAs alone. BRAVE is seen as an option to RTAX FPGAs, with NG-LARGE we can move into medium performance data processing. For high performance re-programmable data processing we need DSPs. Current European FPGA developments may not provide sufficiently high performance.
EI: Mixed signal elements in FPGA may be attractive and should be researched, to complement the usual digital functionality.

Discussion Topic: Requirements Definition and Architectures

DCU: For R&D planning we need to understand the problem domain. What will be the challenges in the future to which we need to respond ? For making technology choices one needs to predict the future application's technology needs in 5/10/15 years time. This may be challenging.
RC: Discussions on required performances are often focused on target performances of single processor chips. However, one should also analyse the performance needs on payload level. On large payloads you may need / use more devices; scalability requirements (possibility of efficient interconnection of multiple chips) then become important. When developing an integrated DSP / FPGA device, it is important to find the right combination as chip development is expensive and European industry cannot afford too different chip developments.
TAS: There is a clear need in space applications for COTS FPGAs and COTS DSPs.

4 Summary and Next Steps

The round table discussions have provided important insights into the current thinking, needs and expectations of European Industry and Academia on the topics discussed. Overall the stated opinions are quite well in line, and can be summarized as follows:

- For digital signal processing in space applications, both DSP ASICs and FPGAs will be needed in future. ESA's R&D should therefore support both development lines.

- For new developments, the correct anticipation of the needs in 5/10/15 years time is essential, as resulting ASIC developments are expensive and only a limited number of different ASIC developments can be afforded. The requirements analysis should include performance needs on system level, and derive scalability requirements for the chip level.

- There is a strong consensus in European industry and academia on the expected benefits of integrating on-chip FPGA fabric on future processor ASICs (both DSP and GPP). Advantages are expected especially for flexible interfacing, but less so for on-chip FPGA based high performance data processing. For the latter case the use of separate DSP and FPGA in MCMs is suggested.

- COTS components (both DSPs and GPP) are expected to play an important role in future space based digital signal processing, in parallel to rad-hard high reliability solutions.

- For European rad-hard FPGAs, industry hopes for good performances achievable with the upcoming BRAVE devices but does not expect them to provide a single solution for payload data processing. For follow-up developments, partial re-configurability is desired.

Based on these consolidated opinions, the following actions / next steps for ESA in the area of DSPs are proposed:

- **A requirements consolidation and technology study should be performed to support the optimal technology choice and architectural design of New Digital Signal Processor ASICs for space applications.**

- **A study on the integration of FPGA / eFPGA with DSP and GPP should be performed with high priority, in order to have the results available as an input to the ESA 2018/2019 TRP cycle.**

- **The development line of COTS based DPUs for space based data processing shall receive continued support via ESA R&D.**

These will be injected into ESA's internal decision / planning processes.

5 Reference Documents

[1] R. Trautner, J. Both, D. Merodio, R. Jansen, R. Weigand, DSP and FPGA: Synergy, Competition, and Future Integration in Space ASICs, Proceedings of AMICSA & DSP 2016, Gothenburg, 2016.

[2] AMICSA & DSP 2016 conference website, https://indico.esa.int/indico/event/102/

[3] Next Generation Processor for On-board Payload Data Processing Application, ESA Round Table, TEC-EDP/2007.35/RT, October 2007.

6 Glossary of Acronyms

Acronym	Explanation
ADI	Analog Devices Inc., United States
ASIC	Application specific Integrated Circuit
AB or AIRBUS	Short form for Airbus Defence & Space, France / Germany / UK
MICROCHIP Atmel	European Semiconductor Manufacturer, France (former ATMEL)
CBK	Centrum Badan Kosmicznych PAN, Poland
COTS	Commercial Off The Shelf
CPU	Central Processing Unit
DCU	Dublin City University, Ireland
DMA	Direct Memory Access
DSP	Digital Signal Processor
EI	Enterprise Ireland
ESA	European Space Agency
ESTEC	European Space Technology Centre, NL
FLOPS	Floating Point Operations Per Second
FPGA	Field Programmable Array
GFLOPS	Giga (10^9) Floating Point Operations Per Second
GOPS	Giga (10^9) Operations Per Second
GPP	General Purpose Processor
CG	Cobham Gaisler, Sweden
I/F	Interface
I/O	Input/Output
IP	Intellectual Property
ITAR	International Traffic in Arms Regulation (US)
LEON	A SPARC compatible processor IP core
MFLOPS	Mega (10^6) Floating Point Operations Per Second
MCM	Multi-Chip Module
MIPS	Million (10^6) Instruction Per Second
NGDSP	Next Generation DSP (synonym for previous effort to port the ADI 21469)
RAM	Random Access Memory
RC	Ramon Chips, Israel
R&D	Research and Development
ROM	Read Only Memory
SpFi	SpaceFibre
SpW	SpaceWire
SRAM	Static RAM
ST	ST Microelectronics, France
SSC	Swedish Space Corporation, Sweden
TAS	Thales Alenia Space, France / Italy / Spain
UoD	University of Dundee, UK
Syderal	Syderal S.A., Switzerland